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Highly robust wideband rectangular waveguide-to-substrate-integrated-waveguide transition leveraging a dielectric superstrate

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Research Paper

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Abstract

This work presents a comprehensive analysis of a superstrate-based air-filled rectangular waveguide (RWG) to substrate-integrated waveguide (SIW) transition that spans the entire D-band (110–170 GHz). The transition architecture exploits a resonant slot together with an aperture-coupled resonant patch, jointly optimized with a dielectric-loading superstrate. Its operation is examined in detail through an equivalent circuit model to analyze its key operating mechanisms. The robustness of the proposed superstrate-based concept is then further evaluated and compared with alternative topologies through full-wave electromagnetic simulations. Particular emphasis is placed on realizing the design within a standard Any-Layer High-Density Interconnect printed circuit board (PCB) process, by ensuring its tolerance to manufacturing variations. Measurements of multiple RWG-to-SIW transition prototypes show a 46% fractional bandwidth, covering the entire D-band, and a low insertion loss of 0.95 ± 0.15 dB, confirming the significance of the proposed transition as a reliable component for D-band RWG-to-PCB interfacing.

Introduction

Achieving the high data rates and low latency targets of next-generation communication and sensing systems calls for large-scale D-band (110–170 GHz) antenna arrays featuring highly directive beams and wide bandwidths [4]. Such D-band arrays generally exploit either printed circuit board (PCB)-based technologies [1–3] or low-loss waveguide-based approaches such as rectangular waveguide (RWG), commonly fabricated through CNC milling [5], 3D printing [6], or silicon micromachining [7]. While PCB-based implementations offer a compact and integration-friendly solution, their higher intrinsic losses limit the achievable efficiency for large, high-gain arrays. In contrast, RWG-based implementations provide superior efficiency, but are less suited for compact integration with active circuitry. As a result, hybrid configurations are often preferred for such applications [8], in which integrated circuits (ICs) are mounted on a PCB platform through flip-chip or wirebond interconnections. Consequently, efficient and broadband transition structures become essential to interconnect the PCB-mounted components with the RWG-based antenna arrays.

Such PCBs must accommodate numerous control and power interconnects required for operating the associated electronics, resulting in carrier architectures composed of multiple thin substrate layers [9]. End-launch PCB-to-RWG transitions [10, 11] offering a broad impedance bandwidth can be realized on these multilayer carriers, while utilizing only a limited number of layers. However, these transitions inherently occupy a large lateral area, leading to bulky assemblies and often necessitating a split-block configuration [10, 12] or augmentation of the waveguide implementation through adaptations such as stepped impedance structures [13]. As an alternative, vertical-launch transition topologies [14–18, 20–22] enable more compact integration, though none currently achieve full D-band coverage. To realize a high-performance and versatile D-band interface between RWG and PCB in heterogeneous integration platforms, a transition design that combines compactness, broad bandwidth, and robustness is critical.

We propose a superstrate-based RWG-to-substrate-integrated-waveguide (SIW) transition, which is the first to cover the entire D-band. This is achieved by co-optimizing two resonators, a slot and a patch, with a dielectric-loading superstrate, resulting in a measured -10dB-impedance bandwidth of 108–173GHz (a fractional bandwidth (FBW) of 46%) and an insertion loss (IL) of only (0.95±0.15) dB, which is the lowest currently found at D-band. The presented transition was initially reported in [25], where the superstrate-based concept and corresponding measurement results were first introduced. However, that work was limited to demonstrating the concept and did not provide a detailed analysis of the underlying operating mechanisms nor a systematic investigation of the design parameters. An earlier version of this paper was presented at EuMW 2025 and was published in its proceedings [23]. Yet, in this contribution, we provide a

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Table 1. Performance of state-of-the-art millimeter-wave RWG-to-PCB transitions

ref	f_0 [GHz]	Topology	Size [$\lambda_0 \times \lambda_0$]	# Metal Layers	IL [dB]	FBW [%]
[10]	100	Finline, EL	2.3×0.42	2	0.9	**46**
[12]	92.5	Split-block, EL	8.64×2.78	2	<2	38
[13]	92.5	Stepped waveguide, EL	0.78×1.83	2	1.1*	38*
[14]	**140**	Back Cavity, **VL**	1.18×0.53	2	1.1	10.1
[15]	60	Inductive Vias, **VL**	0.89×0.6	2	0.5	**45.5**
[16]	90	Stepped Impedance†, **VL**	0.83×0.76	3	0.6	37.8
[17]	**140**	RWG irises, **VL**	n/a	2	2.5	35
[18]	52	Wedge Waveguide Aperture, **VL**	0.27×0.77	3	1.1	**44**
[19]	**140**	Stepped Waveguide†, **VL**	1.26×0.77	3	0.6	**44**
T.W. [23]	**140**	Superstrate, **VL**	0.93×0.51	4	0.95	**46**

[†] indicates depth routing, EL = End-Launch, VL = Vertical-Launch, * indicates simulation

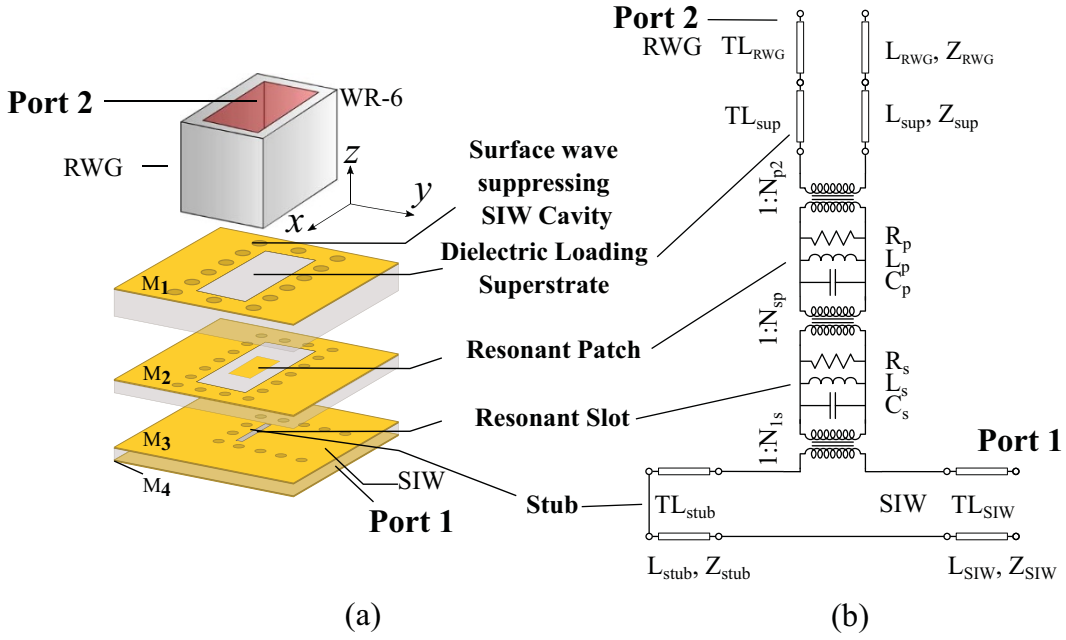


Figure 1. (a) Proposed topology in [23] and (b) Equivalent circuit model containing the coupling mechanisms discussed in [23, 25], which influence the resonances associated with the slot and patch resonators. The equivalent circuit parameters are given as follows: $L_{SIW} = 1\,mm$, $Z_{SIW} = 265\,\Omega$, $L_{RWG} = 1\,mm$, $Z_{RWG} = 495\,\Omega$, $L_{sup} = 0.147\,mm$, $Z_{Sup} = 230\,\Omega$, $L_{stub} = 0.1625\,mm$, $Z_{stub} = 263\,\Omega$, $N_{1s} = 1.29$, $N_{sp} = 0.98$, $N_{p2} = 0.83$, $R_s = 5\,k\Omega$, $L_s = 0.39\,nH$, $C_s = 0.11\,fF$, $R_p = 100\,k\Omega$, $L_p = 0.98\,nH$ and $C_p = 2.8\,fF$.

deeper analysis of the previously proposed transition by introducing an equivalent circuit model that not only explains its underlying operating mechanisms, but also provides a means to estimate the optimal resonance frequencies of the patch and slot, as well as the optimal superstrate height. Next, we examine the robustness achieved by the superstrate-based approach to account for the tight design tolerances inherent to standard multi-layer high-density interconnect (HDI) PCB fabrication at D-band. In addition, the proposed transition does not require depth routing, ensuring compatibility with standard PCB manufacturing processes. Variations in other relevant design parameters are also investigated, demonstrating the topology's resilience to the full range of expected tolerances. Furthermore, several prototypes have been measured, providing experimental evidence of the robustness of the proposed superstrate-based transition.

In the literature, several wideband vertical-launch RWG-to-planar-waveguide transitions have been reported. These approaches also employ aperture coupling: the on-PCB SIW [15, 16] or microstrip [14, 17, 18] feed structure excites a resonant patch, which then couples to the RWG to realize wideband interfacing. However, achieving an impedance match across the full D-band (FBW≥43%) requires additional matching elements in such configurations. In [15], inductive via posts are introduced to control the matching bandwidth. However, relying on the precise placement of a single via makes the transition sensitive to fabrication tolerances at D-band. In [16], broadband performance

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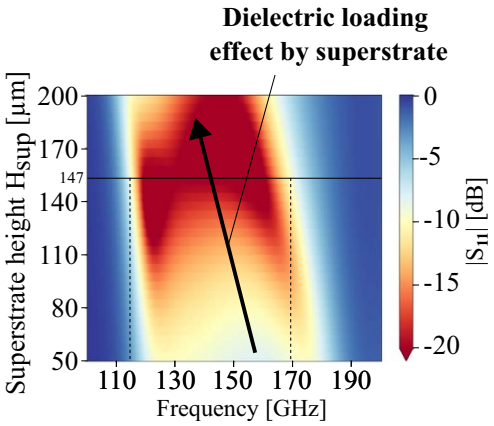


Figure 2. Magnitude of the reflection coefficient in dB, as a function of frequency and superstrate height, based on the proposed equivalent circuit. Increasing the superstrate height shifts the operating band downward. An optimal superstrate height of $H_{sup} = 147\ \mu$m is selected to maximize D-band coverage.

is obtained using depth routing to form a stepped-impedance SIW section, which enhances bandwidth but adds design complexity due to the need for accurate depth control. Similarly, [19] deploys depth routing to create a stepped impedance waveguide, along with an additional substrate taper to create a RWG-to-differential microstrip transition that covers the full D-band. The D-band transition in [14] relies on an aperture and a back cavity. Measurements align well with simulations, indicating good tolerance robustness, though the structure still falls short of full D-band coverage. In [17], a microstrip-to-RWG transition achieves an FBW of 35% by incorporating irises into the RWG. This approach reduces on-PCB complexity, requires custom RWG sections, and results in higher IL. [18] implements a microstrip-to-RWG structure based on a probe and resonant patch to achieve an FBW of 44% at an operating frequency of 52GHz. The design counters RWG-to-PCB misalignment and improves matching through a wedge-shaped waveguide. Although its IL is higher than that of the solution presented here, which enhances robustness using only a standard WR-06 waveguide, the wedge-shaped approach is compatible with this work, and combining both strategies can be considered. These works are summarized in Table 1.

In the "Transition operation and modeling" section, we analyze the operation of the transition component provided previously in [23, 25] by means of an equivalent circuit model. In the "Robust full D-band superstrate-based RWG-to-SIW transition" section, our proposed superstrate-based approach is compared to an alternative structure that omits the superstrate, underpinning its superior robustness against fabrication tolerances. The "Experimental validation" section explains the validation approach, including the measurement setup and S-parameter measurements of several fabricated prototypes, which are compared to the simulation results. Finally, the "Conclusion section" concludes the paper.

Transition operation and modeling

To realize an interfacing component that enables efficient RWG-to-PCB interconnection for next-generation communication and sensing systems operating across the entire D-band, a wideband and low-loss design is essential. In this work, we introduce an RWG-to-SIW transition that exploits a resonant slot–patch configuration, further enhanced by incorporating a dielectric-loading

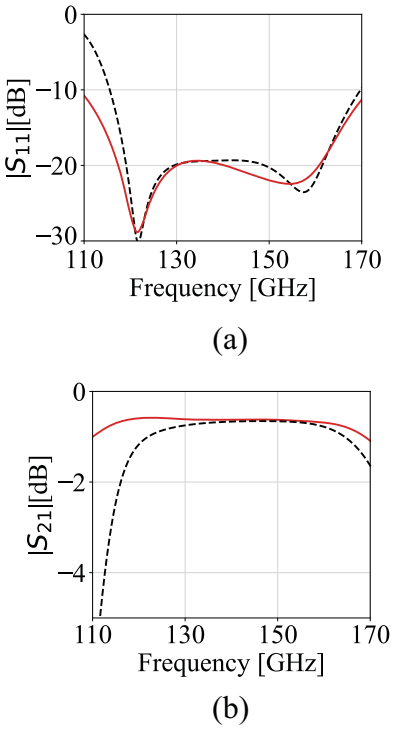


Figure 3. (a) Reflection coefficient and (b) insertion loss of the simple equivalent circuit from Figure 1(b) (black dashed curve) and full-wave simulation (red curve). The existence of the in-band resonances is correctly predicted. However, the model is less accurate at the lower end of the band due to missing additional coupling mechanisms not modeled by the initially proposed equivalent circuit.

superstrate, consisting of Megtron 7 R-5680(N) [26] dielectric material, to achieve the target performance [23]. The combined slot and patch resonances provide the required wideband characteristics, while the dielectric superstrate ensures that these resonances fall within the D-band. Crucially, the superstrate significantly enhances the structure's resilience to PCB fabrication tolerances. The proposed component is depicted in Fig. 1(a).

The proposed RWG-to-SIW transition exploits three main components: a resonant slot (M_3), a resonant patch (M_2), and a dielectric superstrate, whose behavior can be directly mapped to the equivalent circuit model depicted in Fig. 1(b). In this model, the slot and patch are represented by RLC resonators, while the superstrate is modeled as a short RWG section. The coupling mechanisms responsible for the transition operation (SIW-slot coupling, slot–patch coupling, and patch–RWG coupling) are explicitly included as transformer components. Physically, the slot couples the TE_{10} mode of the SIW section, dimensioned for a cut-off frequency $f_c = 85$GHz to ensure in-band linear-phase behavior [24], to the TM_{100} resonant mode below the patch, which then interfaces with the RWG's TE_{10} mode.

The superstrate is tuned using the equivalent circuit model to optimally position both resonances within the D-band. This step is essential, as the slot alone cannot be made sufficiently long inside the SIW to achieve an in-band resonance without dielectric loading, as shown previously in [25]. The effects of varying the superstrate height, thus affecting the dielectric loading, are illustrated in Fig. 2. Increasing the superstrate height shifts the band of operation downward in frequency, allowing for D-band coverage with the resonant slot-patch pair. From this simulation, a superstrate height $H_{sup} = 147\ \mu m$ is selected.

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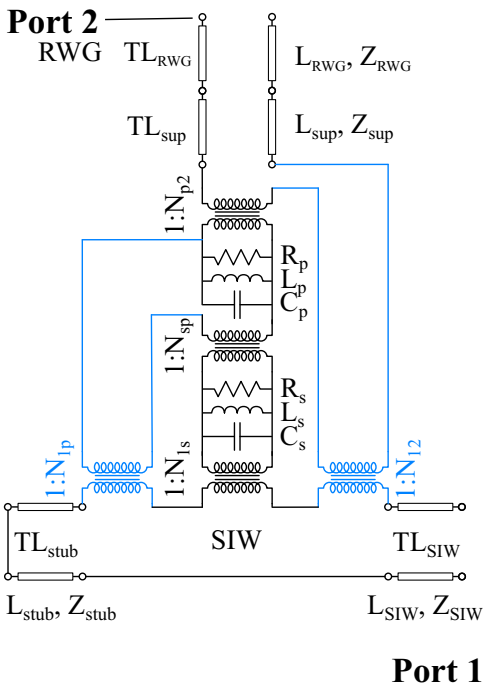


Figure 4. Advanced equivalent circuit modeling additional parasitic coupling mechanisms representing direct coupling between the SIW and the patch, and between the SIW and the RWG. These additional elements are indicated in blue. The updated circuit parameters are given by: $L_{SIW} = 1\,mm$, $Z_{SIW} = 265\,\Omega$, $L_{RWG} = 1\,mm$, $Z_{RWG} = 495\,\Omega$, $L_{sup} = 0.147\,mm$, $Z_{Sup} = 230\,\Omega$, $L_{stub} = 0.1625\,mm$, $Z_{stub} = 263\,\Omega$, $N_{1s} = 1.52$, $N_{sp} = 1.43$, $N_{p2} = 0.73$, $N_{1p} = 0.86$, $N_{12} = 1.85$, $R_s = 5\,k\Omega$, $L_s = 0.46\,nH$, $C_s = 0.11\,fF$, $R_p = 100\,k\Omega$, $L_p = 0.98\,nH$ and $C_p = 2.6\,fF$.

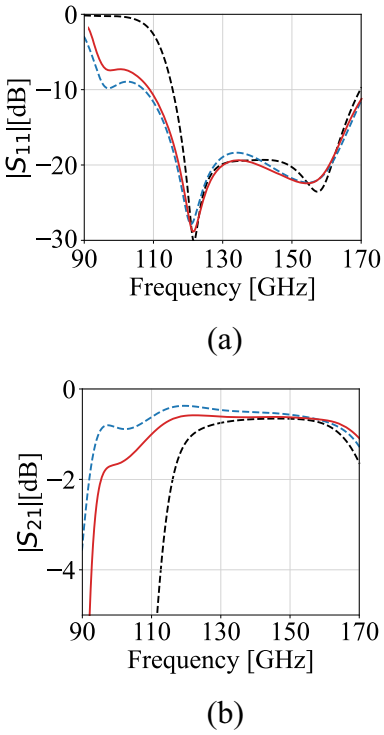


Figure 5. (a) Reflection coefficient and (b) insertion loss of the simple equivalent circuit from Figure 1(b) (black dashed curve), advanced equivalent circuit from Figure 4 (blue dashed curve), and full-wave simulation (red curve). The [90–110 GHz] range is included to highlight the additional out-of-band resonance introduced by parasitic coupling mechanisms, which is captured only by the advanced circuit model.

After establishing in-band operation, the resonance frequencies, the lower one governed by the patch width (W_p) and the upper one by the slot length (L_s), are distributed over the D-band to maximize the bandwidth, with optimal resonance placements at 120 GHz and 157 GHz.

The reflection coefficient and insertion loss of the equivalent circuit are shown in Fig. 3. They are compared to a full-wave electromagnetic (EM) model, with the previously obtained $H_{sup} = 147\,\mu m$, in the band of interest (110–170 GHz). Note that the aforementioned slot and patch resonances are indeed present in the equivalent circuit model as well as in the full-wave Em simulation. However, given that its results deviate from the EM simulation at the lower end of the band, the equivalent circuit model no longer captures the detailed behavior of the transition in this frequency range. Despite this, the model provides valuable insight into the operation of the RWG-to-SIW transition. Moreover, it has proven highly effective for obtaining an initial parameter estimation, specifically the aforementioned superstrate height. To obtain more accurate predictions across the full 110–170 GHz band, a more comprehensive equivalent circuit is required.

Using the parameters obtained from the simplified model as a starting point, we introduce the advanced equivalent circuit shown in Fig. 4, which incorporates additional parasitic coupling paths that influence the bandwidth of the insertion loss. These added elements represent direct coupling between the SIW and the patch, and between the SIW and the RWG (both occurring via the slot). These effects were not included in the simpler model. By accounting for these mechanisms through curve fitting of the advanced model to the full-wave EM results, the behavior shown in Fig. 5 is obtained. An additional resonance, absent in the initial equivalent circuit model, is now accurately captured, resulting in excellent agreement with the full-wave EM simulation. The insertion loss predicted by the advanced equivalent circuit model also closely follows the EM results, providing nearly identical in-band performance over 110–170 GHz.

Note that, while the coupling level between the resonators needed to be tuned to match the response of the advanced equivalent circuit, the parameters of the slot, patch, stub, and superstrate remain effectively unchanged. In particular, the superstrate height and the stub length retain the same values in both the physical implementation (EM-model) and the equivalent circuit representations, thereby showcasing physical significance and simplifying the curve-fitting procedure.

In summary, the simplified equivalent circuit serves as an efficient tool for conceptualizing the transition operation and for rapidly estimating key design parameters such as the in-band resonance frequencies and the required superstrate height. Building on this foundation, the advanced equivalent circuit offers a higher level of accuracy by incorporating additional coupling mechanisms. While being more intricate and therefore less suited for initial optimization, this advanced model reliably reproduces the full-wave EM behavior across the entire D-band. It is thus well-suited for providing a more detailed understanding of the operating mechanisms of the proposed component.

Robust full D-band superstrate-based RWG-to-SIW transition

We now compare the proposed transition with an alternative approach for achieving in-band operation through dielectric

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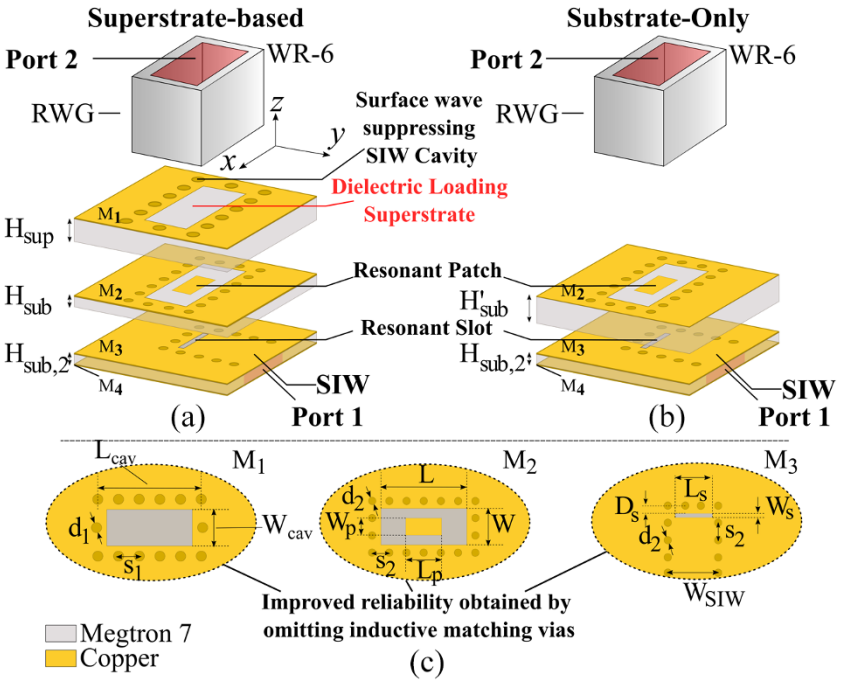


Figure 6. Geometry of the proposed RWG-to-SIW transition employing a resonant patch and slot, co-optimized with (a) a thin dielectric substrate layer (H_{sub}) with additional superstrate layer (H_{sup}) and (b) a thick dielectric substrate layer (H'_{sub}) without additional superstrate layer to place both resonances within the D-band and ensure full D-band operation. An SIW cavity is included to suppress surface wave propagation. (c) includes the remaining transition parameters. Final dimensions of the superstrate-based/substrate-only design: L_{cav} = 2 mm/2 mm, W_{cav} = 1.1 mm/0.93 mm, L = 1.65 mm/1.65 mm, W = 0.7 mm/0.525 mm, L_p = 0.7 mm/0.65 mm, W_p = 0.32 mm/0.25 mm, d_1 = 0.2 mm/0.2 mm, s_1 = 0.4 mm/0.4 mm, d_2 = 0.15 mm/0.15 mm, s_2 = 0.3 mm/0.3 mm, L_s = 0.725 mm/0.735 mm, W_s = 0.075 mm/0.075 mm, W_{SIW} = 1.05 mm/1.05 mm, D_s = 0.125 mm/0.125 mm, H_{sup} = 147 μm/-, H_{sub} = 102 μm/150 μm, $H_{sub,2}$ = 102 μm/102 μm. Megtron 7 substrate: ϵ_r = 3.2, tan δ = 0.005, copper surface roughness: R_a = 300 nm.

loading. The benchmark topology, shown in Fig. 6(b), implements this by increasing the substrate height H'_{sub} rather than by introducing the superstrate layer (similar to, e.g., [21]) as in the proposed design. Functionally, this alternative component behaves similarly to the structure analyzed in the previous section, but with dielectric loading governed by the thicker substrate instead of the superstrate height H_{sup}. Fig. 6 summarizes both configurations: in-band operation is achieved either using the superstrate-based solution (H_{sup}, Fig. 6(a)) or by relying on a thicker substrate (H'_{sub}, Fig. 6(b)).

When comparing both options, the substrate-only design offers a slight cost advantage, since it requires only three metal layers instead of the four needed for the superstrate-based approach. Meanwhile, both options result in a comparable bandwidth and IL. However, we now show that, once robustness, previously identified as a critical design criterion, is taken into account, the superstrate-based solution clearly outperforms its substrate-only counterpart.

Fig. 7 presents an extensive variation analysis of the substrate and superstrate height parameters for both configurations, showing how these variations affect the transition's frequency-dependent reflection coefficient. The results indicate that the superstrate-based design can accommodate variations up to ±20 μm (20%) in substrate height and ±28 μm (18%) in superstrate height before losing full D-band coverage. In contrast, the substrate-only design already experiences bandwidth degradation for substrate height deviations as small as ±7.5 μm (5%).

Note that H'_{sub} not only controls the dielectric load on the slot and patch resonators, but also directly determines their physical separation. Because the coupling level between these resonators depends on this separation, variations in H'_{sub} introduce an additional bifurcation effect affecting the resonance frequencies, ultimately reducing robustness. When a superstrate is used, however, these mechanisms, dielectric loading and mode bifurcation, remain decoupled, as illustrated in Fig. 7(b) and 7(c), respectively. An analogous result is obtained when varying the dielectric constants of the respective dielectrics; the superstrate-based structure shows superior tolerance against variations in dielectric constant.

This is further supported by the equivalent circuit model, where the aforementioned effects are modeled through variations in the L_{sup} and N_{sp} parameters that affect the dielectric loading and mode bifurcation, respectively. If no superstrate is included in the model, these effects cannot be decoupled.

The insertion loss is virtually the same for both topologies, with simulations showing an in-band value of approximately 0.65 dB, when considering an average copper surface roughness R_a = 300 nm. This confirms that adding a superstrate layer does not introduce any meaningful loss. Additionally, the bandwidth of the superstrate-based design is slightly higher, covering the entire D-band (110–170 GHz). Meanwhile, the substrate-based alternative achieves a slightly lower bandwidth of 120–170 GHz. As a result, despite requiring one extra layer, the superstrate-based design is chosen as the preferred RWG-to-SIW topology for PCB implementation, especially given that substrate height tolerances of about 10 %, corresponding to variations of roughly 15 μm, are typically encountered in practice.

To further assess the robustness of the superstrate-based design with respect to fabrication tolerances in the remaining design parameters, Fig. 8(a) and 8(b) present a cornerstone analysis alongside the nominal reflection coefficient and insertion loss. The results confirm that the design maintains robust full D-band coverage, achieving a nominal FBW of 46 % with a simulated insertion loss of 0.65 dB. Based on manufacturer data [27], variations of up to 50 μm in the slot, patch, and cavity dimensions, as well as 10 % deviations in each substrate height, have been considered. The transition is found to be resilient to variations of this scale. The largest deviations in behavior are found to be caused by the slot length L_s and patch length L_p, which control the resonances of the design. Particularly, a decrease in L_p exceeding 50 μm is most critical, as it may occur due to overetching and leads to mismatch within the D-band. Meanwhile, slot length variations of up

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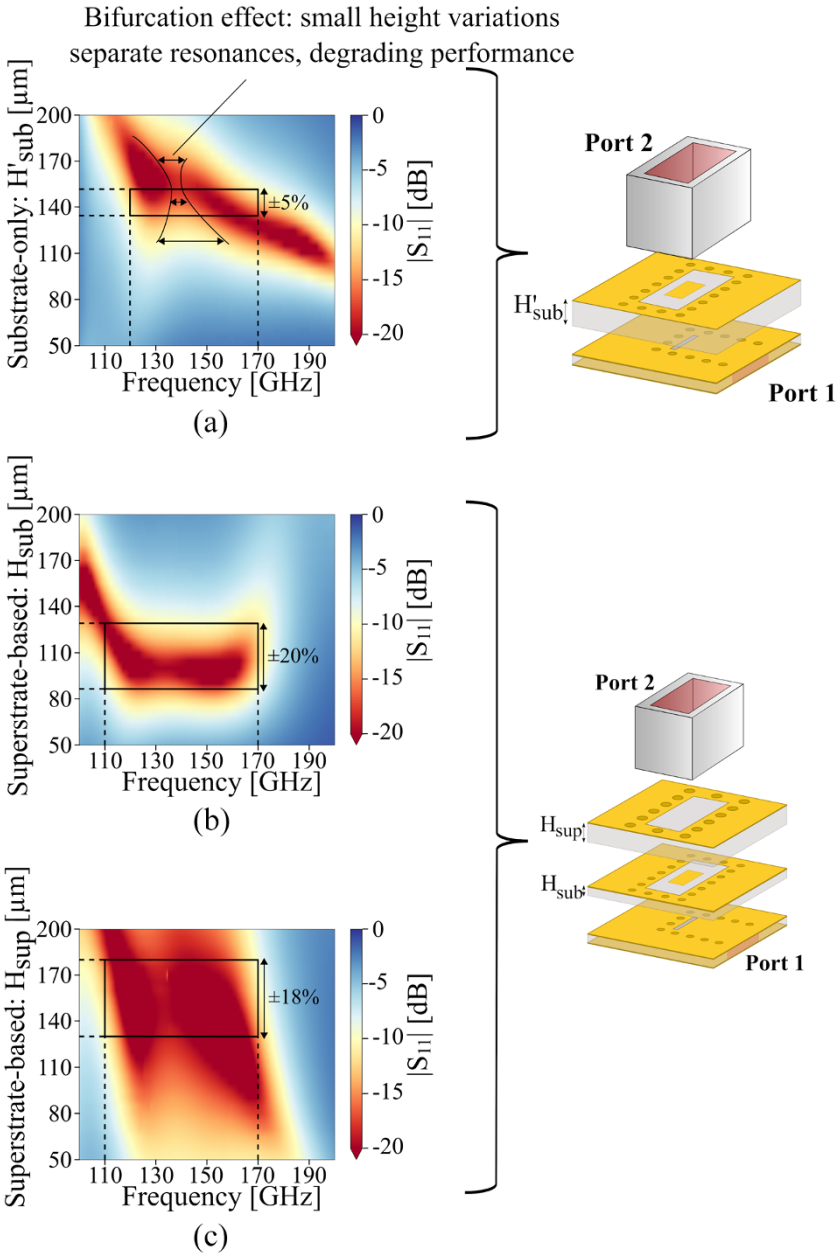


Figure 7. Magnitude of the reflection coefficient, in dB, as a function of frequency and of (a) the substrate height in the nominal substrate-only design, (b) the substrate height in the nominal superstrate-based design, and (c) the superstrate height in the nominal superstrate-based design. The region where the operating bandwidth is still covered, is indicated by the black boxes. The analysis demonstrates that the superstrate-based design is four times more robust against height variations of both substrate and superstrate.

to 75 µm can be tolerated. Moreover, the simulations show that the structure exhibits linear phase behavior within the entire -10 dB impedance bandwidth.

Experimental validation

To validate its performance, a back-to-back configuration of the superstrate-based RWG-to-SIW transition component is manufactured using a standard HDI PCB fabrication process. To accommodate the range-extender waveguide flanges, an SIW section of at least 11 mm in length (L_{SIW}) is required between the two transitions. To keep this length as short as possible, the transitions are placed on opposite sides of the PCB within the resulting eight-layer stack-up. Additional slot-coupled SIW layer transitions are introduced in metal layers M_4 and M_5 to connect the two transitions with minimal influence on the overall back-to-back behavior (Fig. 9). To estimate the extra insertion loss contributed by the SIW sections, prototypes with different SIW lengths (LSIW = 11.35 mm and 13.75 mm) are included on the fabricated panels, enabling the extraction of the line-length-dependent losses from the measurement data [28].

The S-parameters are measured with a Keysight N5242B PNA-X microwave network analyzer in combination with Virginia Diode Incorporated (VDI) D-band VNA extenders [29] and WR-6 RWGs. The measurement setup, including the locations of the thru–reflect–line (TRL) calibration reference planes, is shown in Fig. 10. During the measurements, 3D-printed structures are used as supports to clamp the RWG and PCB together, ensuring alignment and air-gap-free contact. The proposed setup and TRL calibration allow for measurements of four prototypes from two successfully manufactured panels to be measured at the PCB interface, allowing for direct comparison to simulation.

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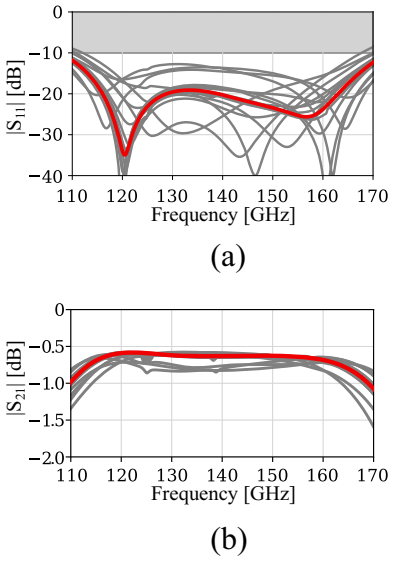


Figure 8. Nominal reflection coefficient (a) and insertion loss (b) of the superstrate-based transition subject to variations of up to 50 μm in slot, patch and cavity dimensions, as well as 10 % variations in each substrate height, indicating full D-band coverage with low insertion loss under all expected parameter variations.

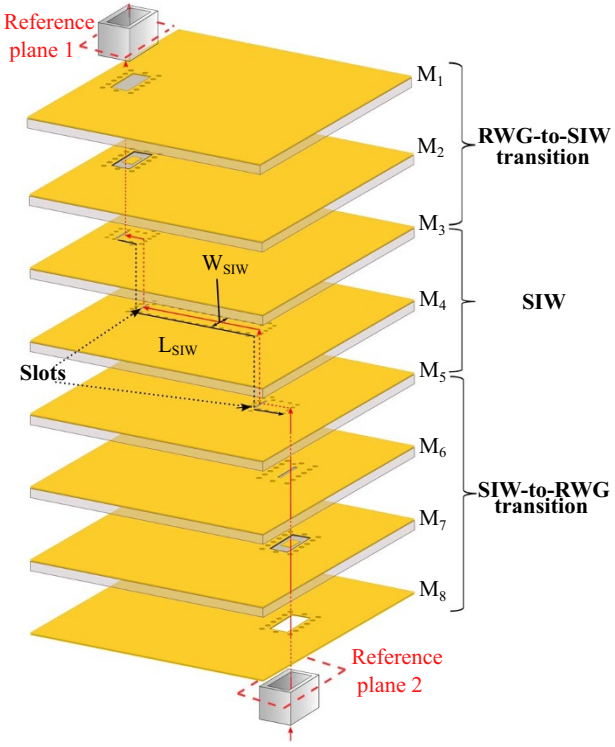


Figure 9. Back-to-back RWG-to-SIW transition connected by an SIW section of length L_{SIW}.

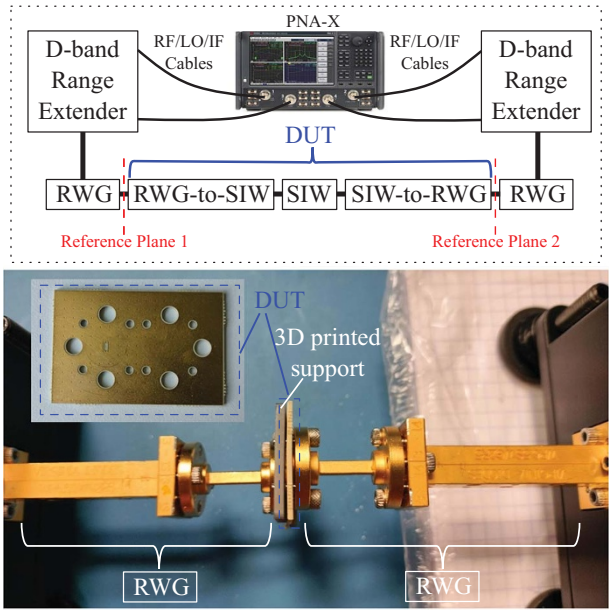


Figure 10. Measurement setup of the back-to-back RWG-to-SIW transition using Virginia Diode Incorporated (VDI)'s D-band range extenders.

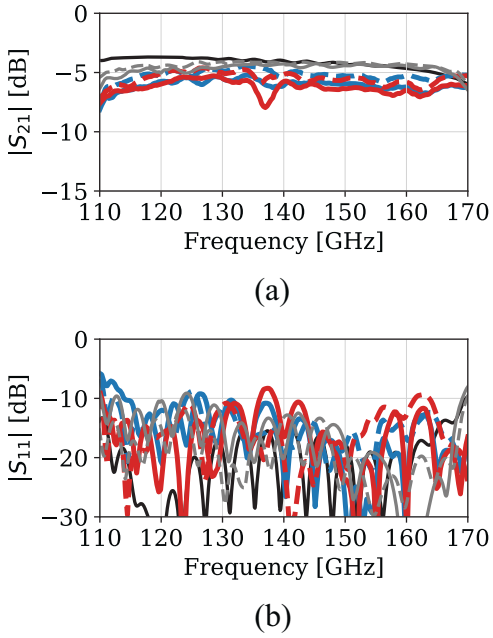


Figure 11. Transmission coefficient (a) and reflection coefficient (b) of the back-to-back transitions of the equivalent circuit (black), EM-simulated (gray), panel 1 (blue), and panel 2 (red) results. The 11.35-mm-long-line is indicated by the dashed lines, and the 13.75-mm-long line with full lines.

Fig. 11 shows the measured S-parameters of the entire back-to-back transition structure for two different line lengths, indicating that the back-to-back reflection coefficients align well with simulation across the entire D-band. All four measured prototypes exhibit good matching throughout the band. The average insertion losses of the 11.35 mm and 13.75 mm SIW lines equal 5.2 dB and 6 dB, respectively, which corresponds to a measured SIW loss of 0.33 dB/mm in the Megtron 7 substrate, compared to 0.28 dB/mm in simulation. From these results, the average single-ended transition insertion loss is determined to be 0.95 dB, slightly higher than the simulated value of 0.65 dB. This difference is attributed to increased substrate, conductor, and surface-roughness losses, consistent with the marginally higher measured SIW loss. Additional simulations indicate that the observed excess loss can be reproduced either by assuming a surface roughness of approximately 2 μm or by increasing the dielectric loss tangent to 0.0125, providing representative upper-bound estimates for these parameters. In practice, the measured loss is expected to result

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from a combination of both effects. The average in-band variation of the insertion loss is 0.15 dB.

Conclusion

A novel broadband RWG-to-SIW transition has been presented that achieves a 46 % bandwidth for $|S_{11}| < -10$ dB, enabling full coverage of the 110–170 GHz D-band. This performance is realized by co-optimizing a resonant slot and an aperture-coupled patch together with a dielectric-loading superstrate. In this contribution, an equivalent circuit model was introduced to analyze the transition's underlying operating mechanisms more thoroughly and to provide practical guidelines for selecting the optimal slot and patch resonance frequencies as well as the optimal superstrate height. Additionally, the superstrate is proven to significantly improve the robustness of the presented component against fabrication tolerances, which are a primary concern at operating frequencies beyond 100 GHz. Comprehensive cornerstone analyses demonstrate that the proposed topology maintains stable performance across the full range of expected HDI PCB tolerances. Measurements performed on multiple fabricated prototypes exhibit good agreement with simulations, with a single-ended insertion loss below 0.95 ± 0.15 dB, while preserving complete D-band coverage.

Overall, the proposed superstrate-based transition achieves wider bandwidth, lower insertion loss, and substantially greater robustness to manufacturing variations than competing approaches reported in the literature. These features make the proposed topology a highly attractive solution for reliable RWG-to-PCB interfacing in next-generation high-frequency communication and sensing systems.

Competing interests. The authors declare none.

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