International Journal of Microwave and Wireless Technologies

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An efficient drain-lag model for microwave GaN HEMTs based on ASM-HEMT

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Research Paper

Cite this article: Beleniotis P, Schnieder F, Krause S, Haque S, Rudolph M (2022). An efficient drain-lag model for microwave GaN HEMTs based on ASM-HEMT. *International Journal of Microwave and Wireless Technologies* **14**, 134–142. https://doi.org/10.1017/S1759078721001483

Received: 10 May 2021
Revised: 20 September 2021
Accepted: 27 September 2021
First published online: 20 October 2021

Keywords:
GaN HEMTs modeling; drain lag; ASM-HEMT; physics-based models; microwave HEMTs; compact models

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Abstract

Large-signal modeling of Gallium Nitride (GaN) based high electron mobility transistors (HEMTs) demands a proper description of trapping effects. In this paper, a new, simplified yet accurate drain-lag description is proposed, enhancing the simulation accuracy and the extraction flow of the physics-based compact model ASM-HEMT. The present study investigates the impact of drain lag on specific physical phenomena, focusing on the relation between trap states, surface-potential calculations, and electron transport properties. It is supplemented with a revised extraction procedure, minimizing the required measurements, thereby the undesired consequences of several passes on the same device, using pulsed I-V and pulsed *S*-parameters only, and approaches for efficient and accurate simulation results. We show that the proposed trap model is a determinative tool for simulating both small and large-signal behavior predicting precisely *S*-parameters and load-pull performance.

Introduction

Gallium Nitride (GaN) high electron mobility transistors (HEMTs) are nowadays considered as the best option for high power and high temperature radio-frequency (RF) and microwave amplifiers. Due to material properties, GaN HEMTs provide higher robustness under tough environmental conditions compared with competitive materials, making them exceptionally suitable for space, broadband communication, and automotive applications [1, 2]. Such applications demand designs with highly accurate as well as highly efficient models.

An important peculiarity of GaN-based HEMTs, which should be sufficiently described by a model, is trapping effects [3]. Trapping effects in GaN and generally in III-Nitride semiconductors are still an unavoidable feature that obstructs real performance capabilities. The consequences of trapping phenomena in GaN-based devices fall into two main categories: gate lag and drain lag. The first term (gate lag) describes trapping effects that assisted by gate voltage variations creating the delayed response of the drain current [4, 5]. Accordingly, drain lag is the delayed response of the drain current during drain voltage variations [6]. Trapping of electrons can happen in several parts of the semiconductor heterostructure. The most predominant locations are the surface and in general the upper parts of the device as well as the channel and buffer layers. Gate lag appears mainly due to trapping at the surface and the upper layers of the semiconductor heterostructure, whereas the region related to drain-lag effect is the GaN channel layer and mainly the buffer. Several techniques, such as surface passivation and treatment or field plates, have achieved a serious reduction of gate lag [7–9]. In a previous study, Luo *et al.* [10] have already observed the negligible gate lag for the device we are going to use in this study. On the other hand, due to native defects in GaN, and the intentional Fe or C doping in order to enhance electron confinement of the 2DEG, drain lag can significantly affect device performance [11, 12].

The proposed model constitutes an enhancement of the physics-based compact model ASM-HEMT [13, 14] in the drain-lag description. ASM-HEMT is based on surface potential calculations providing high flexibility and a better insight into trapping phenomena because of the direct connection of model parameters with physical effects. However, the already built-in trap model lacks an important feature of traps, the difference between time constants of two events, capture and emission of electrons. The closest approach to a trap's behavior is described by the Shockley-Read-Hall (SRH) recombination [15, 16] and therefore some trap models have been developed in order to simulate trapping effects in ASM-HEMT according to physics [17, 18], showing a good agreement with experimental results. However, the employment of the above theory in compact modeling conduces to a complicated extraction procedure due to the introduction of additional parameters that properly manage the feedback from the respective sub-circuit. Also, original trap model's parameters are not always capable to fully describe pulsed I-V measurements. This can play a crucial role in the large-signal model's performance for typical microwave applications, where the large-signal excitation covers an

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extended area of the output characteristic. Recently, Khandelwal *et al.* [19] suggested a new approach for the drain-lag description. This approach provides a sufficient prediction of pulsed output characteristics over a very broad range of quiescent drain voltage V_{dsq}, by introducing a non-linear scaling of model parameters. However, that non-linear model can be simplified and linearized for common microwave applications with GaN HEMTs, where usually trapping comes from the well-known 0.5 eV level [20, 21]. First-principles Density-Functional-Theory (DFT) calculations [22, 23], as well as experiments [24], have associated that trap level with Fe-impurities in GaN. TCAD simulations by Uren *et al.* [25] have shown that trapping in a passivated AlGaN/GaN HEMT with Fe-doped buffer will mainly affect the region under the gate and a narrow part of the drain access region, after high V_{ds} stress. Electron trapping will be negligible at the source access region and the major part of the drain access region.

In this paper, we demonstrate a trap model for GaN-HEMT devices, focusing only on drain-lag effects, neglecting the gate lag. The model involves both linear and non-linear scaling of model parameters depending on quiescent drain voltage V_{dsq}, simulating accurately the pulsed output I-V curves for the whole range of gate voltage. It is capable to describe the real interaction of the input signal with traps by distinguishing the different time constants for the emission and capture of electrons in a straightforward procedure already used with other compact models [26–29]. Another aim of this study is the proposal of a simplified extraction procedure for ASM-HEMT which adds efficiency on device modeling and minimizes the complexity of the drain-lag description. Thus, we use only pulsed I-V and pulsed *S*-parameter measurements for the model extraction, diminishing the uncertainty created by several measurements on the same device, as firstly proposed by Mallet-Guy *et al.* [30]. We investigate the dependence of surface-potential parameters and the drain access region resistance on the quiescent drain voltage. The present study seeks not only to describe in detail our drain-lag model for ASM-HEMT, as firstly presented in the European Microwave Integrated Circuits Conference (EuMIC) of 2020 [31], but also to update the drain-lag model parameters. In our previous work, we neglected the impact of trapping on the drain access region, omitting the accurate simulation of the knee-walkout observed in GaN HEMTs. The performance of the upgraded drain-lag model at high RF input power is significantly enhanced. Additionally, we continue supporting the weak impact of trapping at the source access region, maintaining the high numerical convergence and the efficient extraction due to the omission of an additional non-linear scaling parameter.

The device under test (DUT) is a two-finger HEMT with 250 nm gate length and 125 µm gate width per finger from the GaN-on-SiC process of the Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik. The semiconductor heterostructure consists of an $Al_{0.25}Ga_{0.75}N$ barrier with a GaN cap layer on top, the GaN channel layer, and a GaN:Fe buffer grown on 4H semi-insulating SiC substrate. The device has an encapsulated gate, formed by two layers of SiN_x passivation, deposited by plasma-enhanced chemical vapor deposition [32].

Required measurements

As mentioned before, one scope of this study is to minimize the required measurements for the extraction procedure. Pulsed *S*-parameters for different quiescent biases are capable to provide us with pulsed I-V measurements and *S*-parameters at once. Considering the great progress on modern devices in manipulating and almost diminishing the gate-lag effect, we focus only on the impact of different drain quiescent voltages, in order to investigate the drain-lag effect. Thus, for determining the trap-affected parameters of the model, pulsed I-V and *S*-parameter measurements for three different drain quiescent biases V_{dsq} (8, 15, and 28 V) were carried out. The gate quiescent bias V_{gsq} must be adjusted according to the operating point of the amplifier. In our simulations, we use a quiescent point related to class AB amplifiers, hence $V_{gsq} = -2.3$ V. The three respective I_{dsq} values are 13, 24, and 35 mA.

At this step, the adjustment of pulse conditions is a crucial factor in order to obtain iso-trapping measurements. The processes of electron capture and emission follow the SRH statistics [15, 16], which describes the recombination of carriers through trapping. The energy difference between the trap level and the conduction-band minimum regulates the emission of electrons. Typical values of the electron emission time constant in GaN range between microseconds and seconds or even more. Following the well-studied analysis of transient drain currents [33], we investigated the trap levels in the DUT and their nature. Our study suggests the presence of one trap level with an activation energy of 0.48 eV, and a capture cross-section of $2.94 \cdot 10^{-16}$ cm^2, creating an emission time constant of 6 ms at room temperature. The activation energy indicates that Fe is the responsible element for trapping in the DUT, in agreement with previous studies [20–24]. On the other hand, the capture of electrons from deep levels in GaN is a fast process with a relatively short time constant. It is strongly dependent on the density of electrons in the conduction band (hence by the Fermi level). According to the theory [34, Ch. 5], knowing the capture cross-section, one can estimate the capture time constant considering the material properties of GaN. Taking also into account that the main region of trapping as shown in [25] would be the upper part of the Fe-doped buffer and the channel, the capture process would have a time constant in the range of nanoseconds. Gomes *et al.* proposed a new characterization technique for the capture time constants in GaN HEMTs [35]. Their results exhibit a fast capture, much faster than 600 ns, making its characterization with common pulsed measuring setups infeasible. They also observed a capture mechanism with a much longer time constant in the range of milliseconds. In our case, where we are treating narrowband signals without long off periods, that slow mechanism can be neglected. Finally, pulse-width must be short enough to reduce temperature variations during the pulse, maintaining the device temperature constant [36].

Taking all the above into account, we used a pulse width of 250 ns and a pulse period of 250 µs [36, 37]. With such pulse conditions, we expect iso-thermal and iso-trapping measurements. Self-heating effect is constant during the measurement, regulated by the dissipated power at the quiescent region. Also, traps are remaining overcharged for V_{ds} below V_{dsq} due to the insufficient time for the slow emission. Thus, pulsed I-V measurements with various quiescent voltages provide us with an insight on different magnitudes of trapping in a steady state.

Trap model description

The proposed drain-lag model can be divided into two main parts: the trap-affected parameters and the drain-lag sub-circuit. The first simulates the device behavior during a steady state of trapping, and the second introduces the transient response of

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the traps into the model. Then, we use both of them to simulate all the possible trapping conditions that can arise depending on time-dependent variations of V_{ds}.

Drain-lag model parameters

The approach behind the iso-trapping conditions allows us to take advantage of the steady-state region of our measurements. Traps will be remaining charged, and the device in a steady state for the V_{ds} values smaller than the quiescent drain voltage V_{dsq}. Thus, we focus on that bias region to extract the model parameters that best describe all steady states, namely all the pulsed measurements. Then we try to correlate the differences between the extracted models. The correlation will provide the trap-affected parameters. Those parameters will reshape our model to simulate trapping effects in their steady states. At this step, as described in section "Required measurements", keeping pulses as short as possible and in the nanoseconds range is crucial to avoid electron emission or self-heating mechanisms. Longer pulses, e.g. microseconds, would obstruct steady state and introduce self-heating effects during the measurement window, creating uncertainties to the extraction procedure.

At first, the extraction of the ASM-HEMT is executed according to the extraction flow for RF modeling suggested by Ahsan *et al.* [14]. The exception here is that we start by simulating one of the pulsed output characteristics instead of the DC one. For this work, the model parameters have been firstly extracted from the characteristic of $V_{dsq} = 8$ V and $V_{gsq} = -2.3$ V. Intrinsic parasitic capacitances have been extracted from pulsed *S*-parameters of the same measurement.

Figure 1 presents simulated and measured pulsed output I-V curves for three different V_{dsq} ((a) 8, (b) 15, and (c) 28 V). Gate voltage V_{gs} is swept from −3 to 1 V with a step of 1 V for all three cases. Simulations are provided by the proposed drain-lag model (black solid line). Also, Fig. 2 presents simulated and measured DC output and transfer characteristics for comparison. The advantage of using only pulsed output I-V curves is significant when the typical kink effect (lies between 4 and 6 V at the drain in Fig. 2(a)) is observed on the static measurements. This behavior prevents the accurate extraction of model parameters based on static measurements alone, ending up with a low modeling performance. A previous study suggests that this kink effect comes from buffer traps [38]. In Fig. 2(a), current exhibits higher values after the kink effect, indicating a repeated electron emission and capture, at low and high V_{ds}, respectively. Thus, trapped electrons' population varies during the voltage sweep in static measurements, creating significant uncertainties in parameters' extraction because of the continuously affected device performance. On the other hand, iso-trapping pulsed measurements cannot exhibit such kink effects. The population of trapped electrons is always constant, defined by the high quiescent voltage V_{dsq}.

We observed that scaling only five model parameters can simulate pulsed output I-V curves over a wide range of V_{dsq}. A positive shift of the threshold voltage with V_{dsq} is observed due to the decrease of the electron concentration in the 2DEG. Scaling the parameter VOFF allows for an accurate description of the threshold voltage shift. As can be seen from the output I-V curves, a higher reduction of the current is apparent for intermediate and high values of V_{gs}. In our case, this effect can be accurately described by an increase of mobility degradation UA with the vertical electric field in the channel. Additionally, Drain Induced Barrier Lowering (DIBL) effect is affected by electron trapping. Model parameters

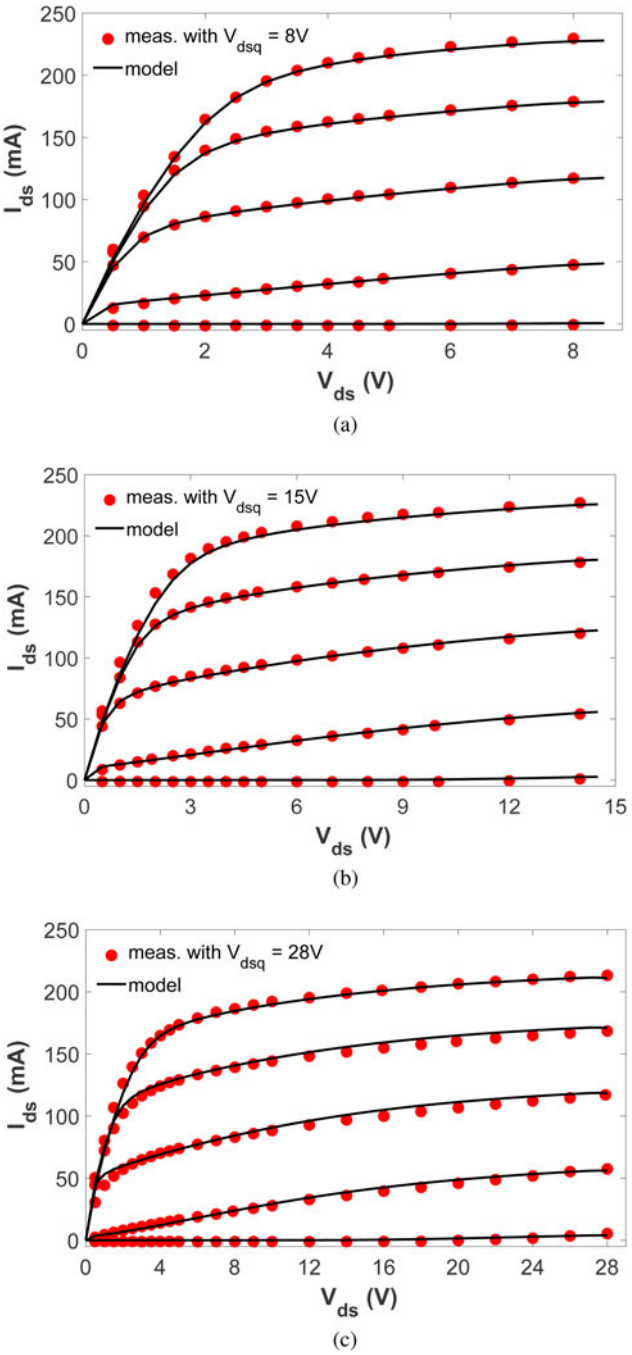


Fig. 1. Simulated and measured pulsed output I-V curves for $V_{gsq} = -2.3$ V and three different V_{dsq} ((a) 8 V, (b) 15 V, (c) 28 V). V_{gs} varied from −3 to 1 V with a step of 1 V.

ETA0 and VDSCALE should be changed according to the magnitude of trapping. The above four model parameters exhibit a linear relation with V_{dsq} given by the equation

$$\mathrm{P}_{V_{dsq}} = \mathtt{trP} \cdot (V_{dsq} - V_{dsqref}) + \mathrm{P}_{\mathtt{ref}} \quad (1)$$

where $\mathrm{P}_{V_{dsq}}$ stands for one of the four parameters to be used for fitting the output I-V curve for the desired V_{dsq}, trP is the respective scaling factor, V_{dsqref} takes the value of V_{dsq} from where we extract main model parameters, i.e. 8 V in our case, and P_{ref} the reference value of the parameter determined for V_{dsqref}.

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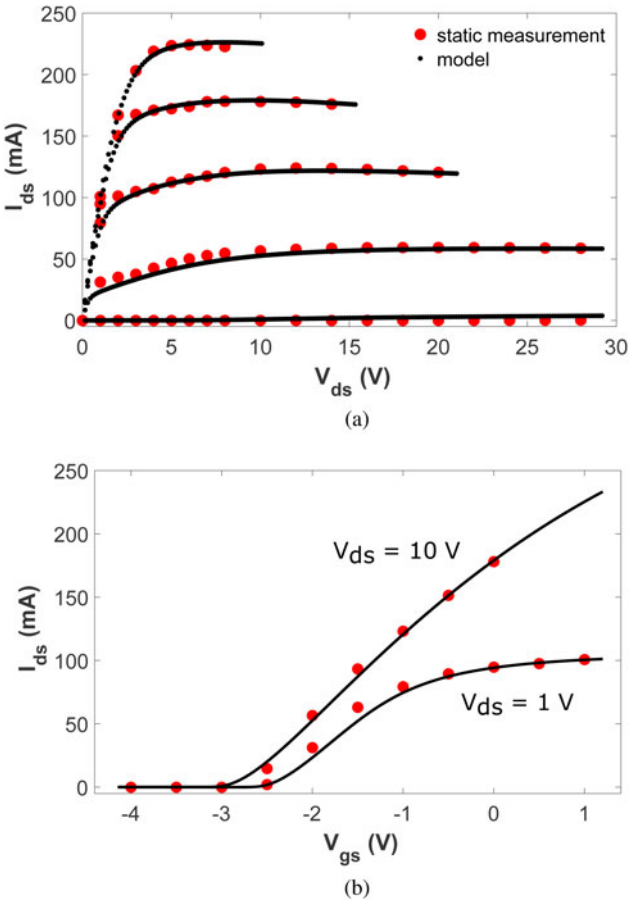


Fig. 2. Simulated and measured DC (a) output and (b) transfer characteristics are presented for comparison.

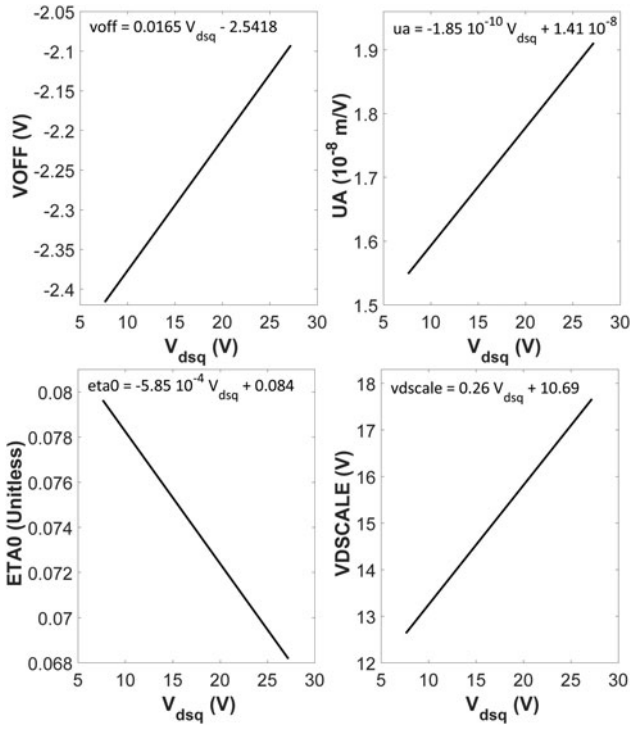


Fig. 3. Scaling lines that the four linearly trap-affected parameters follow depending on V_{dsq}.

The accurate simulation of the knee-walkout and the dynamic R_{on} of the device is achieved by the inclusion of the drain access region resistance in our drain-lag model. A non-linear reduction of the parameter ns0accd (represents the 2DEG density at the drain access region) with respect to the V_{dsq} is observed. We scale ns0accd according to equation (2) (partly adapted from [19]), where $P_{V_{dsq}}$ stands for the paramater ns0accd, trP is the initial scaling factor of ns0accd, V_{dsqref} takes the value of V_{dsq} from where we extract main model parameters, i.e. 8 V in our case, P_{ref} is the reference value of ns0accd determined for V_{dsqref}, V_{dsqsat} is the V_{dsq} where the saturation of scaling begins, and k is used for the best fit of the saturated scaling.

$$P_{V_{dsq}} = P_{\mathrm{ref}} + \mathrm{trP} \cdot V_{dsqsat} \cdot \left(\frac{V_{dsq}}{\left(V_{dsq}^{1/k} + V_{dsqsat}^{1/k}\right)^{k}} - \frac{V_{dsqref}}{\left(V_{dsqref}^{1/k} + V_{dsqsat}^{1/k}\right)^{k}} \right) \quad (2)$$

The proposed drain-lag model can accurately simulate pulsed output I-V curves for all bias regions and every quiescent voltage. Figure 3 presents the scaling lines that every linear trap-affected parameter follows w.r.t. V_{dsq}, whereas Fig. 4 shows the non-linear scaling of ns0accd.

There is a tight connection between all the five trap-affected parameters and the population of trapped electrons. However, the non-linear scaling of ns0accd could provide an interesting insight into trapping effects. In Fig. 4 one can observe a scaling with two different slopes and the transition between them. Parameter trns0accd is the initial scaling factor and parameter k can change that slope when the scaling of ns0accd tends to saturate after V_{dsqsat}. A saturated scaling suggests that the total population of trapped electrons in that region does not change despite the higher V_{dsq}. Therefore, we could hypothesize that the parameter k is related to the highest values of trapped electrons' population in the drain access region. However, further investigation is needed for this assumption.

Drain-lag sub-circuit

A drain-lag model should adequately reproduce the interaction of applied V_{ds} with traps, by imitating the real trap activity in the semiconductor. Discrete trap levels in semiconductors have characteristic time constants for the capture and the emission of electrons, creating the well-known transient response we call lag. Thus, an accurate drain-lag model should reproduce the lagged response that traps create when a change at the applied V_{ds} happens.

For this purpose, we implemented a more straightforward procedure than previous studies with ASM-HEMT to simulate the different time constants of capture and emission. We employed part of the well-established trap model from Jardel *et al.* [26] to create different time constants for the charging and discharging process. Figure 5 shows the model structure used for the purpose of this study. In the upper part, the main model consists of ASM-HEMT accompanied by the extrinsic elements of the device, which are determined by cold-FET *S*-parameter data. The drain and source resistances, R_d and R_s, are omitted from the extrinsic part of the device. They are fully covered by the access region resistance model of ASM-HEMT, which contains both access region and

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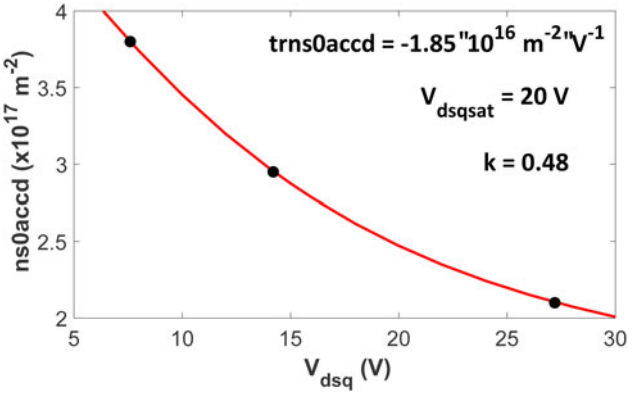


Fig. 4. Extracted values of ns0accd (black dots) and the fitted line versus V_{dsq}.

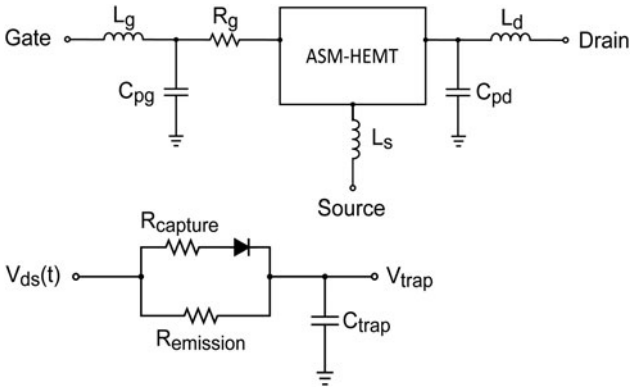


Fig. 5. Schematic of the model topology. V_{trap} is fed back into the model, updating trap-affected parameters.

contact resistances. The drain-lag sub-circuit is shown at the bottom of Fig. 5. The two time constants are defined as follows

$$\tau_{emission} = R_{emission} \cdot C_{trap} \tag{3}$$

$$\tau_{capture} = R_{capture} \cdot C_{trap} \tag{4}$$

In this work, the emission time constant $\tau_{emission}$ is set at 6 ms, while the capture time constant $\tau_{capture}$ at 1 ns. Then, the extracted ASM-HEMT model with the present drain-lag implementation can be used for accurate device large-signal modeling. In order to combine the extracted scaling parameters discussed previously, with the R-C sub-circuit, equations (1) and (2) take the following form

$$\mathrm{P} = \mathrm{trP} \cdot V_{trap} + \mathrm{P}_0 \tag{5}$$

$$\mathrm{P} = \frac{\mathrm{trP} \cdot V_{trap} \cdot V_{dsqsat}}{\left(V_{trap}^{1/k} + V_{dsqsat}^{1/k}\right)^k} + \mathrm{P}_0 \tag{6}$$

where the feedback of the R-C sub-circuit V_{trap} takes the place of V_{dsq}, and instead of P_{ref}, we use the extracted intercept P_0 from Figs 3 and 4, which represent the value of each trap-affected parameter for $V_{dsq} = 0$ V.

Model validation

Before the final validation of the proposed drain-lag model with RF signals, we tested ASM-HEMT's temperature-dependent parameters [39] with our scaling approach. For this purpose, we simulated pulsed output characteristics under different ambient temperatures. Then, the proposed drain-lag description was implemented in ASM-HEMT and used in Keysight ADS design software [40]. A comparison of simulations with *S*-parameters as well as with load-pull measurements at 8 GHz was performed. During this step, we compare the performance of our model with the case that we do not consider any trapping effects using only static measurements for the extraction procedure.

Temperature-dependent effects

In real applications, GaN HEMTs are commonly subjected to ambient temperatures varying in a wide range. High temperature

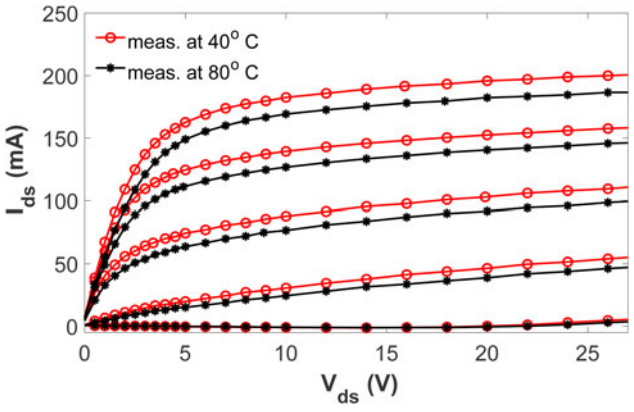


Fig. 6. Measured pulsed output characteristics for two different ambient temperatures (red circles for 40 °C and black dots for 80 °C).

negatively affects microwave performance [41]. A compact model needs to simulate trapping effects in parallel with temperature-dependent phenomena. Figure 6 compares measured pulsed output characteristics at different ambient temperatures varying between 40 and 80 °C, at 26 V of V_{dsq}. According to SRH statistics [15], [34, Ch. 5], the emission of electrons coming from a trap, with activation energy close to 0.5 eV or more [20, 21], and a capture cross-section of 10^{-16} cm^2, is not shorter than microseconds under reasonably high temperatures (< 400 K) [42]. The above suggests that high temperature will not affect our drain-lag model performance for microwave GaN devices. Simulations at high frequency allow us to neglect the temperature-dependent nature of trap's time constants.

The pulsed measurements shown in Fig. 6 present a steady state of the device because of the short pulse-width compared with the long emission time constant even at high temperature. The temperature-dependent parameters of ASM-HEMT [39] could cover the difference that we observe between the two measurements. Indeed, Fig. 7 presents simulation results with an excellent fit of pulsed output characteristics under three different ambient temperatures. The presented model includes the temperature-dependent parameters UTE, UTES, UTED (temp-dependent electron mobility under the gate, source access, and drain access, respectively), AT (temp-dependent saturation velocity), and KRDC (temp-dependent drain contact resistance). For the accurate extraction of the thermal model parameters, one should also consider the

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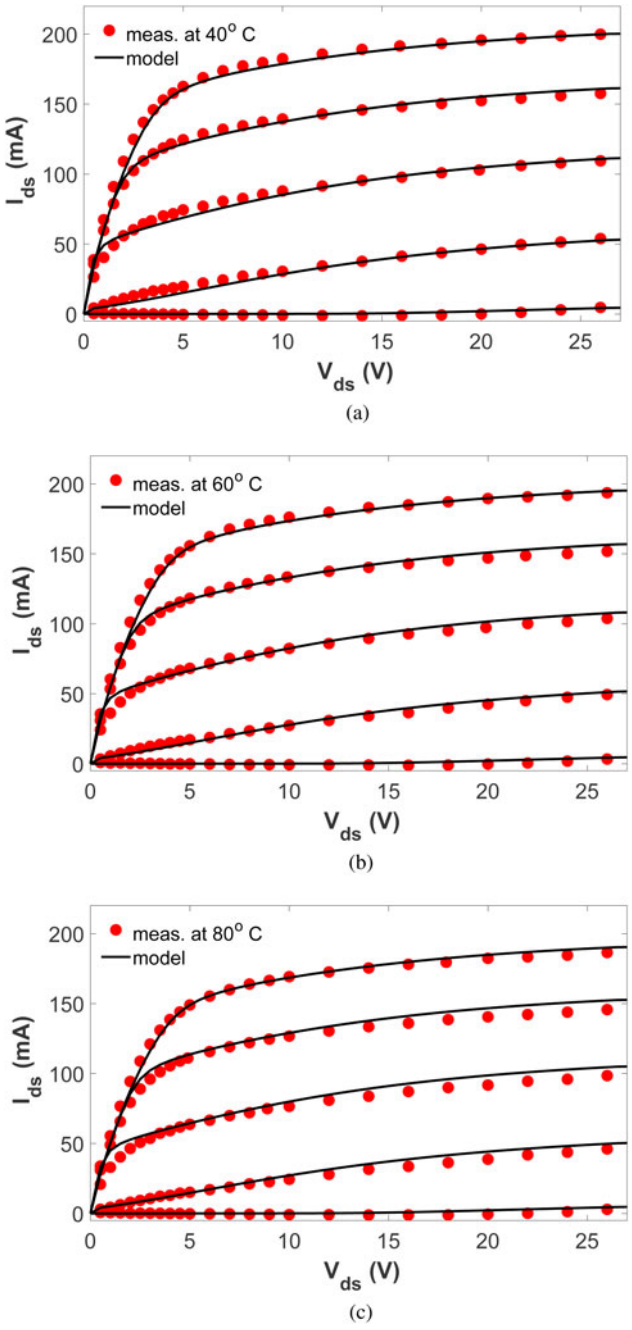


Fig. 7. Simulated pulsed output characteristics for three different ambient temperatures. (a) at 40°, (b) 60°, and (c) 80 °C.

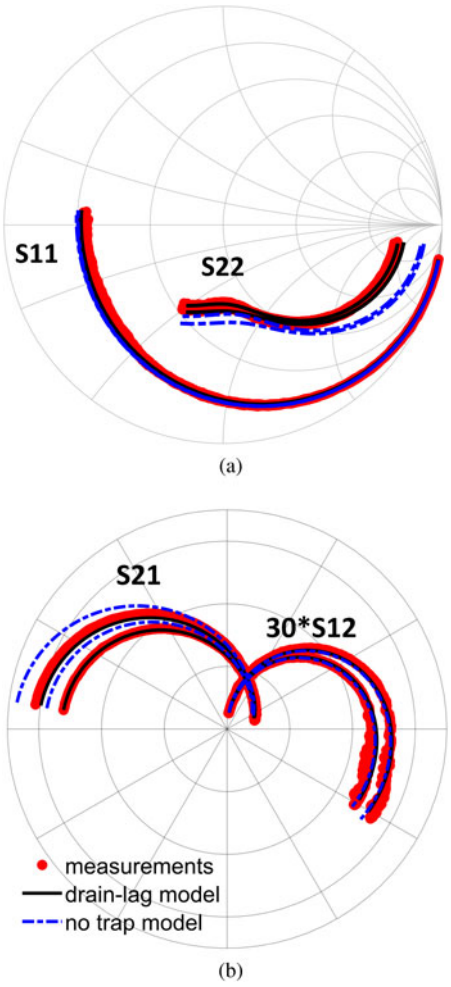


Fig. 8. Simulations (lines) and measurements (dots) for (a) S_{11} and S_{22} at V_{gsq} = −2.3 V, V_{dsq} = 15 V, V_{gs} = −2, and − 2.5 V, V_{ds} = 14 V and (b) S_{21} and S_{12} at the same voltages. Frequency at 0.5–40 GHz (solid lines: extracted from pulsed measurements with the proposed drain-lag model, dashed lines: extracted from static measurements without any trap model).

self-heating effect. In our case, we used the already built-in thermal network of ASM-HEMT with a single thermal time constant. GaN HEMTs during static I-V measurements, such as the one presented in Fig. 2, exhibit self-heating effect appearing with the decrease of I_{ds} for high V_{ds} and high V_{gs}. That bias region allows us to extract the thermal-resistance parameter RTH0 [14] and consider the self-heating effect for our model.

Small-signal model behavior

Figure 8 presents the comparison between simulation results and measurements of pulsed *S*-parameters for V_{dsq} at 15 V and V_{gsq} at −2.3 V. Instantaneous V_{gs} is at −2 V, and −2.5 V, whereas V_{ds} is at 14 V. Biasing of the device was chosen to better address its small-signal behavior in a class-AB power amplifier. Simulations consist of the two different cases referred to before. It is the proposed drain-lag description (black-solid line), and the extracted model from the static output I-V curve of Fig. 2 with no trap model (blue dashed line).

S_{11} and S_{12} are strongly affected by the capacitance description. In both V_{gs} conditions, the two models show an almost identical behavior following the measurements accurately. However, transconductance g_m and output conductance g_{ds} have a strong influence on S_{21} and S_{22}, respectively, concluding that simulations without a drain-lag description provide poor results compared with the ones obtained with the trap model and the exclusive use of pulsed measurements. The appearance of the kink effect at low drain voltages makes the extraction procedure difficult and inaccurate. For devices with such trapping effects, the employment of only pulsed measurements for the extraction of the model is necessary. The ASM-HEMT with our drain-lag description provide a great fit of the measured *S*-parameters, indicating that the extraction from pulsed *S*-parameter measurements

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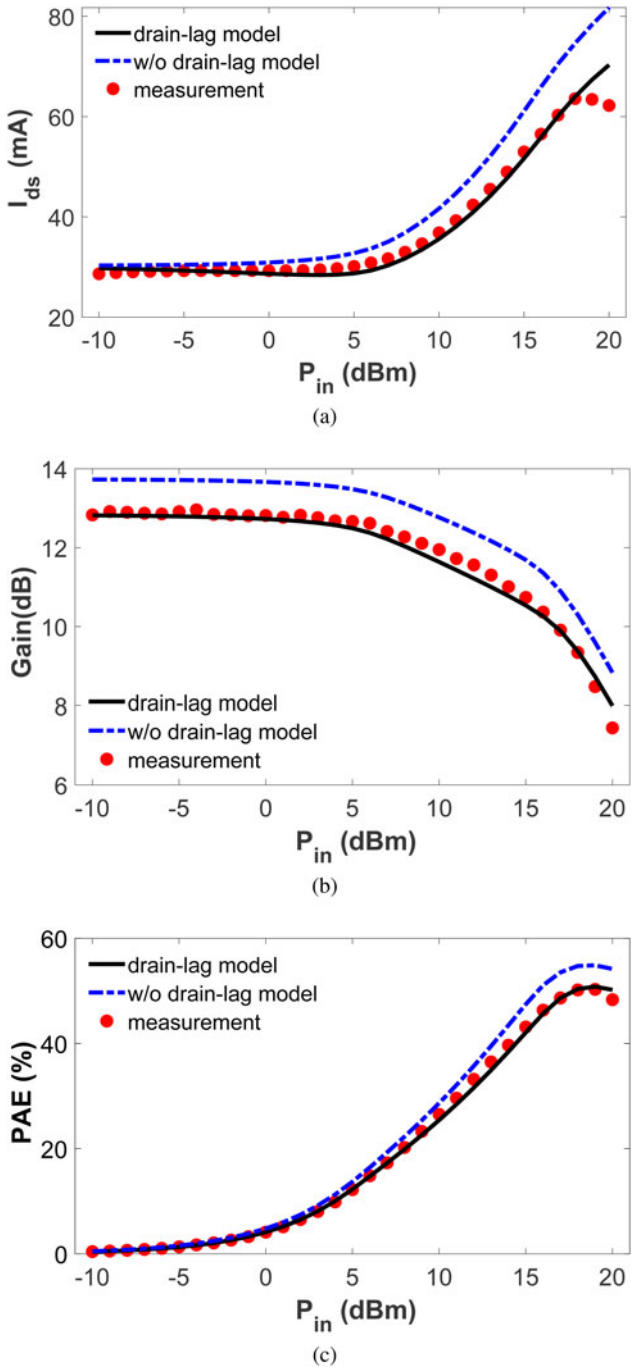


Fig. 9. Simulations (lines) and measurements (dots) of (a) I_{ds}, (b) gain, and (c) power-added efficiency (PAE) at 8 GHz for $I_{dsq} = 110$ mA/mm and $V_{ds} = 15$ V (solid lines: extracted from pulsed measurements with the proposed drain-lag model, dashed lines: extracted from static measurements without any trap model).

only is a crucial and sufficient step to bridge the gap between DC measurements and *S*-parameters, as seen here.

Large-signal model behavior

The validation of the model under large-signal excitation has been examined, comparing RF power-sweep measurements with simulation results. The measurement presented here was performed at 8 GHz with $V_{ds} = 15$ V and $I_{dsq} = 110$ mA/mm, in a region related to class AB amplifier operation. The source and load impedances were chosen at the optimum values for providing maximum output power. Harmonic-balance simulations were carried out, taking into account source and load impedance for the fundamental frequency and the 2nd harmonic.

Figure 9(a) presents a comparison between measurements and simulations for the DC output current I_{ds}, Fig. 9(b) for the RF gain, and Fig. 9(c) for the power-added efficiency (PAE). We observe an excellent agreement between the proposed model's results (solid lines) and measurements (red dots) for the whole range of input power P_{in}. In the same figures, with dashed lines, the model without considering any trapping effects, extracted from the static measurements of Fig. 2, shows its inability to follow the experimental results, presenting a high discrepancy for the whole range of P_{in}. At low P_{in}, both models' behavior is similar to the small-signal operation presented in Fig. 8. Well-fitted *S*-parameters suggest that simulation results here would be close to the experimental values. As can be seen in Figs 9(a) and 9(b), the model without the trap description begins from the correct I_{ds} but the simulated gain is not the real one, in agreement with the discrepancy observed in S_{21} and S_{22}. The implementation of the proposed drain-lag model fixes this error with excellent results. As P_{in} increases, charging of traps continues due to the increase of the dynamic V_{ds} by the RF signal. As a result, the static model cannot follow the measured I_{ds} and fails on providing a good representation of the device. The drain-lag model with the scaling approach always changes its simulation results according to the trap potential conducing to the accurate representation of the DUT.

Conclusion

In this paper, we present a new drain-lag description for the physics-based ASM-HEMT model, dedicated to microwave GaN HEMTs. An R-C sub-circuit simulates trap's transient response by distinguishing the different time constants of capture and emission. We showed that trapping effects in the DUT influence only five parameters of the model. Scaling them depending on V_{trap}, we can accurately describe its large-signal behavior. The proposed description reduces the required measurements for the model parameter extraction to the minimum by employing only pulsed I-V and pulsed *S*-parameter measurements. The model has been validated by *S*-parameter and load-pull simulations, as well as with pulsed I-V measurements at various temperatures. The good agreement with the measurements suggests that it can accurately predict trapping presence in GaN HEMTs' performance.

Acknowledgments. The authors acknowledge financial support from the Graduate Research School (GRS) of Brandenburg University of Technology Cottbus-Senftenberg under Cluster 6 "Hybride Simulation von GaN-HEMTs und Mikrowellenschaltungen" and by Deutsche Forschungsgemeinschaft (DFG) under ref. 440549658. FBH gratefully acknowledges financial support from the German BMBF within the "Forschungsfabrik Mikroelektronik Deutschland (FMD)" framework under ref. 16FMD02.

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