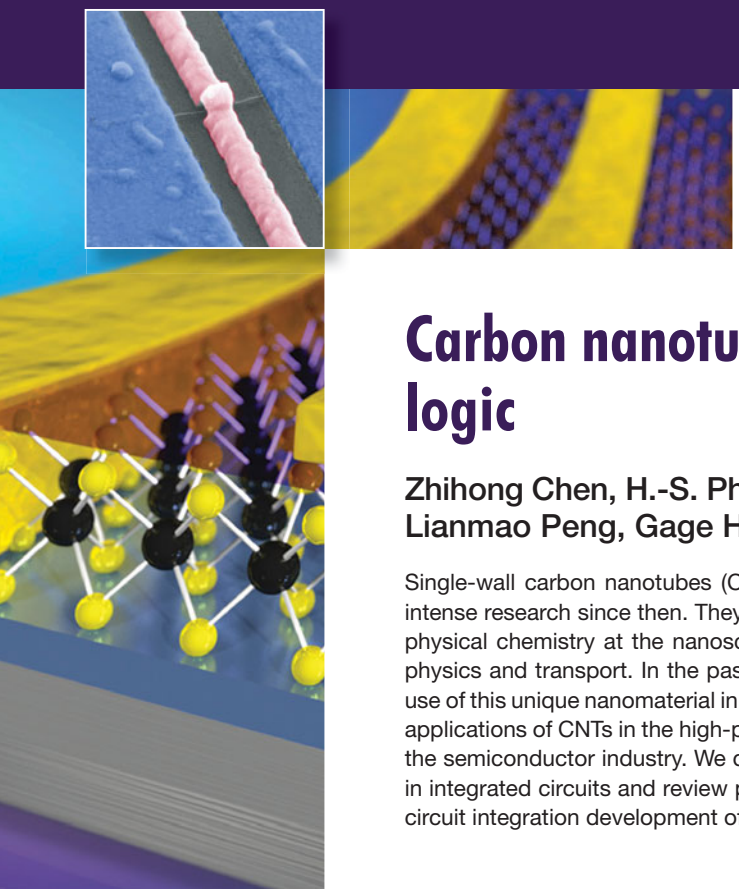


Carbon nanotubes for high-performance logic

Zhihong Chen, H.-S. Philip Wong, Subhasish Mitra, Ageeth Bol, Lianmao Peng, Gage Hills, and Nick Thissen

Single-wall carbon nanotubes (CNTs) were discovered in 1993 and have been an area of intense research since then. They offer the right dimensions to explore material science and physical chemistry at the nanoscale and are the perfect system to study low-dimensional physics and transport. In the past decade, more attention has been shifted toward making use of this unique nanomaterial in real-world applications. In this article, we focus on potential applications of CNTs in the high-performance logic computing area—the main component of the semiconductor industry. We discuss the key challenges for nanotubes to replace silicon in integrated circuits and review progress made in recent years on the material, device, and circuit integration development of CNT technology.

Introduction

Improving the packing density and switching speed of field-effect transistors (FETs) has been the main focus of complementary metal oxide semiconductor (CMOS) computing for decades. It is well understood that both can be achieved through channel length scaling by reducing the physical dimensions and gate capacitance of the FETs. Owing to its one-dimensional (1D) ultrathin nature, electrostatic gate control of a carbon nanotube (CNT) is more efficient than that of a 3D Si channel, which allows for more aggressive channel length scaling in CNT field-effect transistors (CNTFETs). Moreover, CNTs are well known for their high mobility and saturation velocity.[1] All of these exceptional properties make CNTs an ideal channel material and bring the promise of new generations of smaller and faster FETs for high-performance logic computing.

Besides electrostatic gate control, device designs of contacts, gate stack, and layout will also impact the switching speed of the FET. For high mobility channel materials such as CNTs, designing the right gate stack and making good contacts are crucial to access their intrinsic material properties. The most common layout for a CNTFET is the Schottky barrier (SB) transistor,[2] in which metal source/drain electrodes are attached to an intrinsic CNT channel without complicated doping profiles. The contact interface and gate dielectric deposition are found to be critical to the SB-CNTFET device performance.

In the following sections, we present an overview of research on CNT growth, a design paradigm for material imperfection tolerance, post-synthesis material preparation, CNT device fabrication and transport, a compact modeling and performance benchmark, p, n-FETs for CMOS logic, and the largest CNT integration up to date—a CNT computer—as well as 3D integration.

CNT array growth and imperfection-immune paradigm

Controlled manufacturing of CNTs with desired diameter and chirality at predefined spots on a wafer remains one of the biggest challenges for CNT implementation in high-performance logic. While a CNTFET can be fabricated from a single CNT,[3] this device design is perhaps not the most realistic basis for future high-performance integrated circuits (ICs). Even though a single CNT allows for extremely high current density, the current output of such a single-CNT device remains low due to the small size of the channel. Also, the

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DOI: 10.1557/mrs.2014.164

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https://doi.org/10.1557/mrs.2014.164 Published online by Cambridge University Press

statistical variation of CNT properties (mostly due to variations in their diameters and thus bandgaps) is difficult to overcome and would result in a large device-to-device variation. Dense arrays of horizontally aligned CNTs likely provide a more effective basis for high-performance devices, because the parallel electrical transport pathways allow for higher current outputs, and the statistical variation in individual CNTs is averaged out, resulting in a smaller device-to-device variation.

Dense arrays of horizontally aligned CNTs can be achieved by growing CNTs on well-defined single-crystal substrates such as quartz and sapphire (**Figure 1**) by chemical vapor deposition (CVD).[4,5] During the growth, CNTs align along the crystal lattices, resulting in straight CNTs and a high degree of alignment. The CNT density can reach 20–30 CNTs/μm,[6] and in some cases up to 50 CNTs/μm are observed.[7,8] More than 99.9% of the CNTs are horizontally aligned, and their deviation from a perfectly linear architecture is less than 5 nm along lengths of 5 μm.[8]

While high tube densities seem to be attainable, it is well known that substantial position imperfections and a mixture of metallic and semiconductor components inherent in CNT materials remain the main obstacles to the demonstration of robust and complex CNTFET circuits. Mispositioned CNTs create stray conducting paths, leading to incorrect logic functionality, whereas metallic CNTs have little or no bandgaps, resulting in high leakage currents and incorrect logic functionality.[9] The imperfection-immune paradigm, which combines circuit design techniques with CNT processing solutions, overcomes both of these problems.[9,10] The first step is to perform a full wafer-scale aligned CNT growth on a quartz substrate, as shown in Figure 1.[11] Since these crystalline substrates are not suitable for device fabrication, CNTs are then transferred to the substrate used for circuit fabrication (e.g., amorphous SiO_2) through a low-temperature (125°C) transfer method, which maintains the alignment level and density from the growth.[11,12] To remove the remaining mispositioned CNTs, the mispositioned CNT-immune design technique is used.[10,13] Using design principles described in References 11, 14, and 15, CNTFET circuits that ensure correct logic functionality despite mispositioned CNTs have been experimentally demonstrated. These circuits are known as mispositioned CNT-immune circuits, and they are created by etching CNTs from regions pre-defined during circuit layout design using oxygen plasma, such that mispositioned CNTs cannot cause incorrect circuit functionality.[13] The costs associated with this technique are small, and it is also highly scalable: mispositioned CNT-immune digital logic structures have been demonstrated at the wafer scale.[11]

The remaining challenge is the presence of metallic CNTs (m-CNTs) in the array. Several groups have demonstrated strategies to selectively grow well-aligned semiconducting CNTs (s-CNTs).[16–18] By optimizing the carbon feedstock, a purity of 95% s-CNTs has been demonstrated.[16] Since it is currently still impossible to have 100% purity, electrical breakdown can be performed to remove m-CNTs, whereby a sufficiently large source-drain voltage is pulsed to breakdown m-CNTs through Joule self-heating (while a back-gate turns off all s-CNTs), which has shown the ability to remove the required >99.99% m-CNTs[19] for very large-scale integration (VLSI) applications. A specific electrical breakdown technique is known as VMR (VLSI-compatible metallic CNT removal); it is a combined CNTFET processing and design technique that allows electrical breakdown to be performed at the entire chip scale, thereby making it practical for VLSI circuits.[20] Many of the CNTFET circuit demonstrations discussed later in the article, including the CNT computer, employ VMR to remove m-CNTs. Another method to remove m-CNTs exploits nanoscale thermocapillary flow, as reported by Jin et al.[21] In this technique, a very thin layer of a so-called "thermocapillary resist" is evaporated on top of CVD-grown aligned CNTs. A large voltage is applied across the CNTs along with a high positive gate voltage to shift s-CNTs into a non-conducting state. Joule heating causes m-CNTs to heat up and force the resist to flow away, exposing the CNTs. Thus, an etch mask is created that protects the s-CNTs, while the exposed m-CNTs can be removed by subsequent reactive ion etching.

Post-synthesis separation and placement

A different approach for achieving large arrays of s-CNTs is focused on post-synthetic sorting: separating or sorting CNTs by their types (metallic or semiconducting) and/or diameters takes place after they have been grown, but prior to their placement on target substrates. CNTs are first suspended in solution, sometimes combined with selective functionalization of metallic or semiconducting CNTs. A variety of techniques (typically borrowed from life sciences) such as electrophoretic separation,[22] chromatography,[23–26] and ultracentrifugation[27,28] can then be used to separate CNTs by various properties such as their lengths, diameters, and electronic types, as well as separate individual CNTs from bundles.[29] A simple and effective approach for sorting s-CNTs from m-CNTs is based on column chromatography.[26] A solution of CNTs is loaded into a column containing

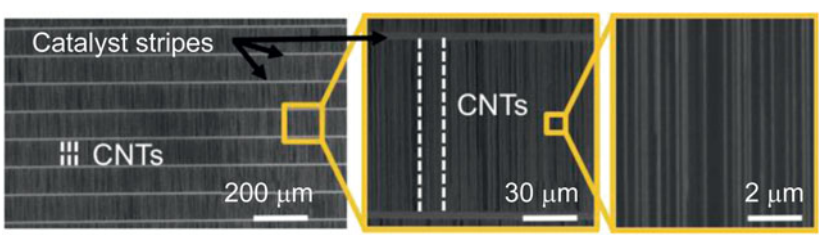


Figure 1. Chemical vapor deposition growth of highly aligned carbon nanotubes (CNTs) on a quartz substrate.

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a gel filtration medium down, which CNTs slowly elute due to gravity. The CNT solution (originally black) separates into red and blue bands that pass through the column at different rates, allowing separated collections at the bottom of the column. The separation mechanism is complicated and is believed to be based on a combination of selective adsorption of the s-CNTs to the column material and difference in travel speed through the pores. The blue band is found to contain m-CNTs, while the red band consists of s-CNTs. By iteratively applying this method, solutions can be purified until they contain more than 99.9% s-CNTs, as confirmed by electrical testing of more than 4000 transistors.[26]

After sorting CNTs by electronic types in solution, the solution containing the required type must be placed on target substrates. While this can be done by simple drop-casting or spin-coating techniques, these will result in random networks of CNTs that are not suitable for large device array fabrication. Recently, it has been shown that selective placement of CNTs, and even some degree of horizontal alignment, can be achieved by chemically functionalizing parts of a patterned substrate, onto which the CNTs are then selectively deposited from solution,[30] see **Figure 2**. A patterned HfO_2/SiO_2 is covered with a monolayer of 4-(N-hydroxycarboxamido)-1-methylpyridinium iodide (NMPI) molecules, which are known to self-assemble on HfO_2 surfaces but not on SiO_2. CNTs are coated with sodium dodecyl sulphate (SDS) solution, which undergoes an ion-exchange reaction with the NMPI in the patterned HfO_2 regions, causing the CNTs to be selectively deposited. By creating very narrow trenches of HfO_2, CNTs even align along the trench direction, creating well-defined areas of horizontally aligned CNTs with densities up to 10^9 CNTs/cm^2.

CNTFET contact interface control

While sp^2-bonded carbon atoms guarantee mechanical and chemical stabilities of CNTs, they make doping CNTs a challenging task. A doping-free approach is thus preferred for high-performance logic device fabrication, where the nature (*p*-type or *n*-type) of the FET is not controlled by doping, but by the contact type instead. The **Figure 3** inset shows a schematic of a simple back-gated CNTFET—a device layout commonly adopted in CNT research. A heavily doped Si substrate covered with 10 nm SiO_2 is used as the supporting substrate, and often can also serve as the back gate and gate dielectric of the FET. Source/drain metal contacts are directly defined on top of the CNT surface by lithography and subsequent metal lift-off.

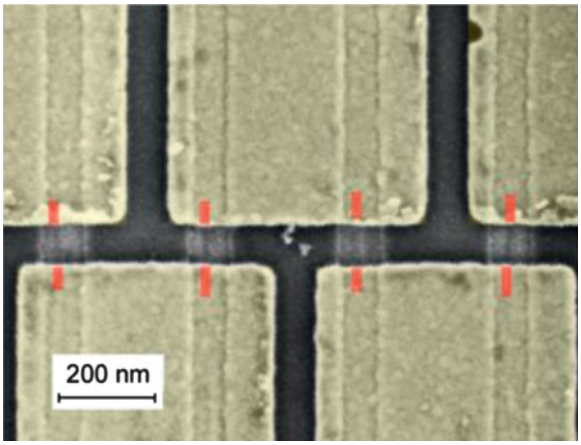


Figure 2. Selective placement of carbon nanotubes (CNTs) by chemical self-assembly. Locations of the CNTs are indicated by red marks.

Unlike 3D semiconductors, the electronic properties of 1D CNTs largely depend on their physical structure.[1] For example, the bandgap of a s-CNT is inversely proportional to its diameter. Since precise diameter control cannot be achieved by growth or post-growth purification yet, and the chemical termination of the CNT surface under a metal contact is not well understood, a large range of on-state currents (I_{on}) from 10^{-5} to 10^{-9}A are reported for CNTFETs with similar device geometries. More importantly, the interface between the metal contact and CNT also behaves differently from that of conventional semiconductors. The well-known Fermi level pinning caused by metal-induced gap states is not a strong effect in CNTs. In order to find the origin of the large I_{on} variation, an investigation of over a hundred CNTFETs was carried out to study the current injection from various metals to CNTs with different diameters.[3]

The transfer characteristics in Figure 3 show high on-state currents at large negative and positive gate voltages, and the device off-state appears in the middle. Given the negative drain biases applied, hole carriers injected from the source contact are responsible for the observed on-state branch (*p*-branch) at the negative gate voltages, while electron carriers injected from the drain contact form the on-state branch (*n*-branch) at the positive gate voltages. In between, the gate voltages set the contact barriers to be so thick that no carriers can be injected into the channel, and the device off-state is formed. These so-called ambipolar characteristics are unique for small bandgap materials directly contacted by source/drain metal contacts. The band profiles illustrating these two current injections are presented in the bottom insets in Figure 3. For circuit applications, the current branch with less drain voltage dependence is desired, which is the *p*-branch in this case and is what we will focus on.

As indicated in the band profile, the current is injected from the source to the CNT channel through a SB. The barrier width is determined by the gate oxide and CNT channel, while the barrier height is determined by the work function difference between the metal contact and CNT as well as the carbon surface chemistry under the contact. On a log scale, I_{on} is inversely proportional to the SB height that is linearly proportional to the bandgap. Given that the bandgap is inversely proportional to the CNT diameter, diameter-dependent I_{on} plots for three different contact metals, Pd, Ti, and Al, are presented in **Figure 4**.[3] All the curves

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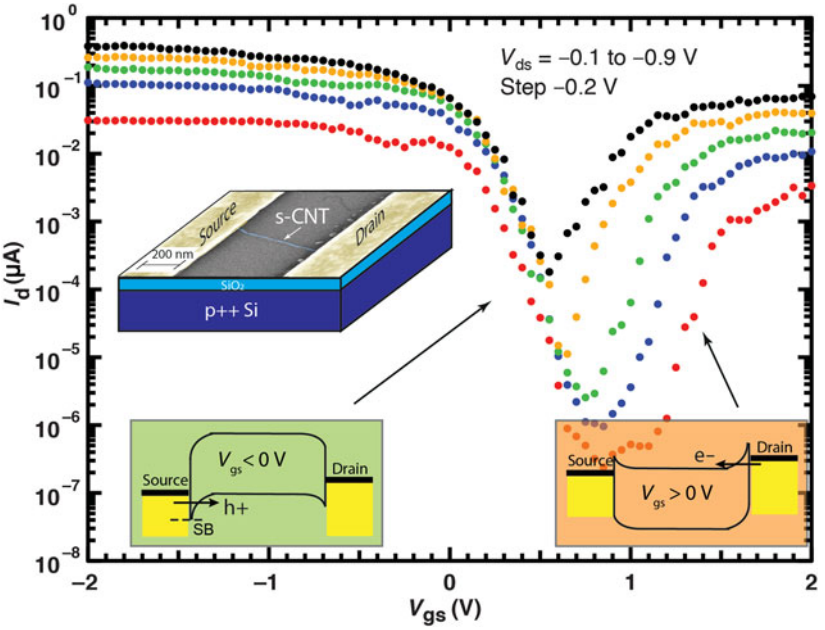


Figure 3. Transfer characteristics of a carbon nanotube field-effect transistor (CNTFET) showing ambipolar behavior. Top inset is the schematic of a back gated CNTFET with a colored scanning electron miscroscopy image on top. The bottom insets show the band profiles for *p*- (left) and *n*- (right) type carrier injection. The *p*-branch is formed by injecting holes from the source into the valence band of the CNT through a gate voltage controlled SB, and the *n*-branch is formed by injecting electrons from the drain to the conduction band of the CNT through a drain voltage controlled SB. Therefore, the drain voltage independent *p*-branch is desired in the FET device operation. Note: V_{ds}, source/drain bias; I_d, source/drain current; V_{gs}, gate voltage; SB, Schottky barrier.[1]

show the same diameter dependence, and the general I_{on} trend follows that of the metal work function. SB heights are extracted by self-consistently solving the Poisson and Schrödinger equation using the nonequilibrium Green's function formalism (NEGF).[3] It is clear that larger diameter CNTs form a smaller SB and carry larger I_{on}. More importantly, the current variation among small diameter CNTs is much more severe than that in the larger ones. When gate dielectrics with smaller effective oxide thickness (EOT) are used, higher I_{on} is observed in the CNTFETs (blue data points in Figure 4) since thinner SBs are obtained through stronger gate control,[31] while SB heights stay the same for the same choices of CNT and metal contact. Thus, in order to conclude whether SBs are present in a device or not, it is not sufficient to rely on high currents and linear output characteristics alone. The near ohmic behavior of Pd, Sc, and Y contacts to large diameter CNTs can be verified by temperature-dependent measurements.[32–34] Unlike large SB contacts, these devices show that I_{on} monotonically increases as temperature decreases.

For a given CNT, both the metal work function and surface chemistry play important roles in the on-state performance of the CNTFET. It is experimentally found that among all high work function metals, palladium (Pd) makes the best contact for *p*-type CNTFETs, and scandium (Sc) and yttrium (Y) are the best contact choices for *n*-type CNTFETs among all low work function metals. When the diameter of the CNT is larger than 1.5 nm, Pd is able to form a nearly SB free contact to its valence band and reach a contact resistance of ~11 kΩ,[32,35] which is close to the quantum limit we will discuss later. Similarly, Sc and Y can form SB-free contacts to large diameter CNTs and reach a contact resistance of ~13 kΩ[33,34] to the conduction band.

Ballistic transport

Due to the 1D confinement, electrons can only travel forward and backward on the surface of a CNT. The requirement of energy and momentum conservation constrains the available phase space for scattering. This results in extremely high mobility in CNTs with very long mean free paths for elastic and acoustic phonon scattering. When the device channel length is scaled down to be close or even shorter than these mean free paths, almost no scattering occurs when electrons travel from the source to the drain. This is defined as ballistic transport, in which the entire source/drain voltage bias is dropped at the contact interface, and electrons travel at their Fermi velocity limit in the channel. Ballistic transport is the best performance that an electronic device can reach. This has been achieved in both metallic and semiconducting CNTs, as shown in **Figure 5**—device

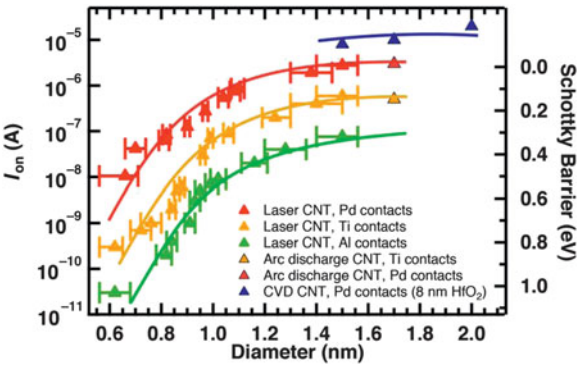


Figure 4. On-state current I_{on} as a function of the carbon nanotube (CNT) diameter for Pd, Ti, and Al contacts. All devices are fabricated on 10 nm SiO_2/Si substrates, except the blue data points that are from CNTFETs fabricated on an 8 nm HfO_2/Si substrate.[31] The right axis shows the extracted Schottky barrier heights from nonequilibrium Green's function formalism simulations for CNTFETs with 10 nm SiO_2 gate dielectric (not applicable for the blue data points). Note: Laser CNT, laser ablation synthesized CNT; arc discharge CNT, arc discharge synthesized CNT; CVD CNT, chemical vapor deposition grown CNT.[3]

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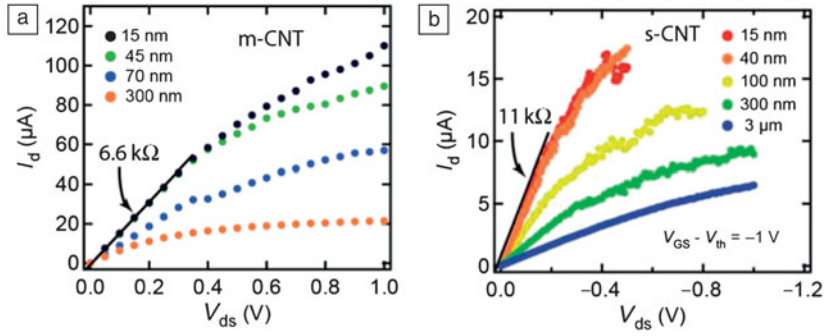


Figure 5. Output characteristics of (a) metallic carbon nanotube (m-CNT) and (b) semiconducting carbon nanotube (s-CNT) devices with various channel lengths. Channel lengths are indicated in the annotation of each figure. Low field resistances for both devices reach the ballistic limit (black solid line). Note: I_d, source/drain current; V_{ds}, source/drain voltage; V_{GS}, gate voltage; V_{th}, threshold voltage.[35]

currents no longer increase as the channel lengths decrease to below 40 nm.[35] To our knowledge, this nearly perfect ballistic transport has only been achieved at room temperature in CNTs. The extracted mean free path for low field scattering is ~200 nm, which again confirms the excellent transport properties of 1D CNTs. From the m-CNT plot, a total resistance of ~6.6 KΩ is extracted from the low field slope. This value is expected as the minimum interface resistance between a 3D metal contact and a 1D conductor with two conduction modes (~13 KΩ for each mode), which is defined as quantum resistance—the fundamental limit of contacting a low-dimensional material. Due to the extra SB and other interface resistances, the s-CNT devices show a larger resistance of ~11 kΩ.

Gate structure and material choices

Due to the chemical inertness of the CNT surface, depositing high-quality, uniform, ultrathin gate dielectrics on CNTs has been identified as a major challenge in CNTFET device fabrication. Earlier studies on the contact properties revealed that some metals, such as Sc and Y, can nicely wet the CNT surface and be easily oxidized to form an ultrathin oxide layer.[34] **Figure 6** shows that a 5 nm yttria (Y_2O_3) layer serves as a perfect dielectric material for a CNTFET, yielding an ideal sub-threshold swing of 60 mV/decade at room temperature.[36] Using low-energy electron diffraction and scanning tunneling microscopy, it is shown that Y_2O_3 forms a complete monolayer on the carbon surface and is stable at high temperature.[37] Both transport and capacitance measurements carried out at cryogenic temperatures also confirm that Y_2O_3 contains very few short-range scattering centers and is an ideal dielectric material for carbon-based devices.[38]

While the ultrathin CNT channel allows for more aggressive channel length scaling, a gate-all-around (GAA) structure is expected to be the ideal geometry to maximize the electrostatic gate control. However, to achieve the GAA structure, CNTs need to be freestanding before the gate stack deposition, and the aforementioned surface inertness is found to cause more serious challenges in fabrication. Atomic layer deposition of high-κ dielectric, Al_2O_3, followed by a gate metal layer, WN, with *in situ* NO_2 functionalization prior to the dielectric deposition was specially developed to address this problem.[39] The nanotube channel is completely encapsulated in the gate metal and dielectric stack, as shown in **Figure 7**.[40] This GAA structure provides the maximum electrostatic gate control that allows for abrupt doping profiles (e.g., the *p*-type/intrinsic/*p*-type (*p*/*i*/*p*) doping illustrated in the schematic), which is key for novel device operations such as tunnel FETs. Recently, GAA devices down to 20 nm gate lengths have been demonstrated to continue the scaling path for CNTFETs and further prove the competitive position of CNTs in high performance CMOS applications.[41]

Compact modeling and performance benchmarking

Energy-efficiency is typically measured in terms of performance per watt, and it has been a key driver for the scaling of digital systems over the last few decades.[42,43] CNTFETs are excellent candidates for building highly energy-efficient digital systems in the future, owing to the aforementioned superior electrostatic control, high mobility, and low supply voltage of operation.[44]

Significant projected CNT technology benefits have led to the development of highly accurate compact CNTFET device models, which account for parasitic resistances, capacitances, and other undesirable effects (such as direct source/drain tunneling current) that exist in highly scaled CNTFET devices.[45–48] Such compact models enable accurate

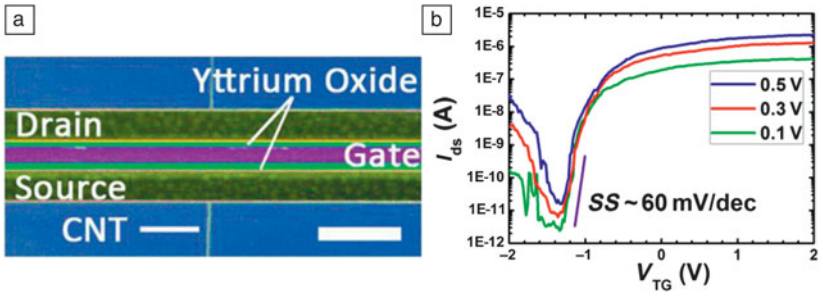


Figure 6. Carbon nanotube field-effect transistor (CNTFET) with yttria top gate dielectric. (a) Colored scanning electron microscope image of a CNTFET, with the CNT diameter d = 1.2 nm and scale bar denoting 4 μm. (b) Transfer characteristics of the device for V_{ds} = 0.1 V, 0.3 V, and 0.5 V, showing a perfect subthreshold slope (*SS*) of 60 mV/decade at room temperature. Note: I_{ds}, source/drain current; V_{TG}, top gate voltage.

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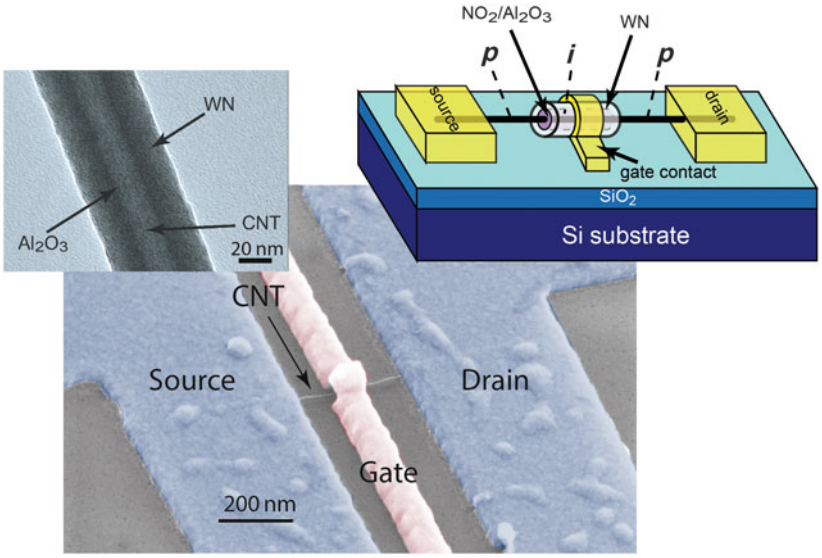


Figure 7. Colored scanning electron microscope image of a gate-all-around (GAA) carbon nanotube field-effect transistor (CNTFET) with wraparound Al_2O_3 gate dielectric and WN gate metal. The CNT segments close to the source/drain contacts are exposed for doping. Left inset is a transmission electron microscope image of the GAA CNT, and the right inset is a schematic of a metal oxide semiconductor field-effect transistor, such as GAA CNTFET, with a *p/i/p* doping profile.[40]

prediction and optimization of the energy-efficiency benefits of CNTFET-based digital systems. In Reference 47, for example, chip-level optimization is performed to achieve the fastest speed under different total chip power constraints for a four-core microprocessor with 1.5 M logic gates and 5 MB of SRAM per core at the 11 nm technology node. In this case, the CNTFET technology is projected to offer 5x faster speed at the same total chip power consumption (across a wide range of power constraints from 10 mW to 100 W) compared to an optimized Si-CMOS technology using partially depleted silicon-on-insulator devices.[47] Note that the energy-efficiency benefits of CNTFETs assume that the CNT density is between 100–200 CNTs per micrometer.[47,49] Many techniques exist for improving CNT density (including techniques to improve grown CNT density,[6,7] as well as multiple transfer techniques[12]), but CNT densities above 100 CNTs per micrometer have not yet been experimentally demonstrated.

p- and n-FETs for CMOS logic

One very important, but often less noted, aspect of CMOS technology is the symmetry between *n*-type and *p*-type devices. For a typical semiconductor, the conduction and valence bands are usually not symmetric, with the effective electron mass at the bottom of the conduction band being much smaller than the effective hole mass at the top of the valence band. As a result, electron mobility in a conventional semiconductor is usually many times larger than the hole mobility, making the design of large-scale ICs more complicated.

The situation for s-CNTs is very different. The band structure is symmetric for the conduction and valence bands, resulting in the same carrier mobility for the two types of carriers. In addition, nearly ohmic contacts are available for efficient injection of both electrons and holes, preparing perfectly symmetric high-performance *n*- and *p*-type CNTFETs for CMOS logic.[50] **Figure 8** shows device characteristics for a pair of *n*- and *p*-FETs fabricated on the same s-CNT. Both transfer (Figure 8a) and output characteristics (Figure 8b) show almost symmetric behaviors.[50] Since doping processes are avoided in the fabrication of CNTFETs, its integration circuit fabrication then becomes much simpler than that of Si CMOSs.

CNT computer

Leveraging the imperfection-immune paradigm, complex CNTFET-based digital systems can now be realized. For example, a general-purpose fully programmable processor has been experimentally demonstrated.[51] This processor can be used to execute any arbitrary program (given enough time and memory), and represents the increased level of integration enabled by the imperfection immune paradigm. It consists of 178 CNTFETs, each comprising 10–200 CNTs (depending on the CNTFET sizes), and is created using the highly scalable fabrication techniques and design flows described in References 9, 12, 51, and 52. The processor circuit contains both combinational circuit elements (e.g., for arithmetic) and sequential circuit elements (e.g., for timing and control), thus demonstrating that any arbitrary digital system can be created using CNTFETs.

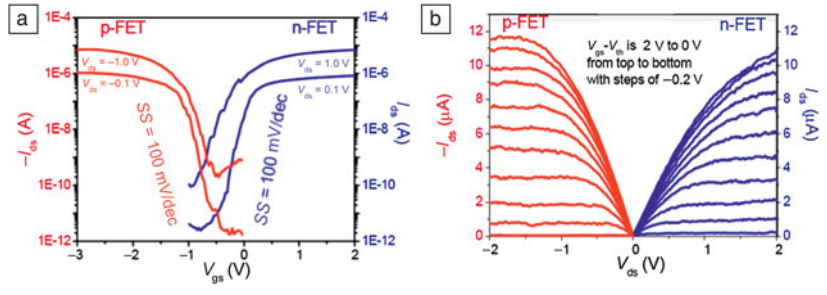


Figure 8. Symmetric carbon nanotube field-effect transistors (CNTFETs) for complementary metal oxide semiconductor logic. (a) Transfer and (b) output characteristics of a *n*-type and a *p*-type CNTFET fabricated on the same (semiconducting) s-CNT, showing almost perfect symmetric performance between *n*- and *p*-type CNTFETs. Note: V_{ds}, source/drain voltage; V_{gs}, gate voltage; I_{ds}, source/drain current; V_{th}, threshold voltage.[50]

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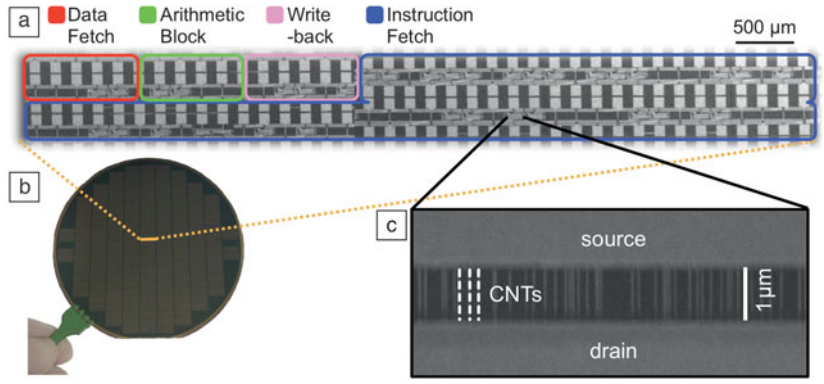


Figure 9. (a) Scanning electron microscope image of a full carbon nanotube field-effect transistor (CNTFET)-based processor, including data fetch, arithmetic block, write-back, and instruction fetch units (full circuit-level and architectural-level details can be found in Reference 51). (b) Optical image of the 4" wafer where multiple instances of the processor are fabricated. (c) Scanning electron microscope image of a single CNTFET in the processor, depicting multiple CNTs bridging the source and drain.

An image of such a full processor is shown in **Figure 9**. Although CNT circuits are projected to operate faster than Si-CMOS circuits (see section on Compact Modeling and Performance Benchmarking), the current CNT computer operates at 1 kHz. This is not a fundamental limit of the CNT technology; instead, the performance is limited by capacitive loading from the measurement setup, the one micrometer minimum lithographic feature size of the fabrication facility it was produced in, and the CNT density of 5 CNTs per micrometer. The CNTFET processor proves that mispositioned CNTs and m-CNTs can be overcome to realize highly scalable CNT circuits. Further advancements in CNT densities will continue to improve the energy-efficiency of experimental CNT circuits. However, the CNTFET processor proves that both mispositioned CNTs and m-CNTs can be overcome in a highly scalable manner, a significant development for the advancement of CNT circuits.

Monolithic 3D circuits

Three-dimensional circuit integration is an attractive technology option because it offers further scaling benefits for digital systems, such as increased device density for the same circuit footprint.[53] In particular, monolithic 3D integration enables interlayer connections at the transistor scale, which is ideal for 3D integrated circuits (3D ICs).[54] Despite these benefits, however, silicon-based 3D ICs are challenging because during the sequential processing of FETs on each layer, high-temperature processing for top-layer FETs degrades the performance of bottom-layer FETs. In contrast, by employing the low-temperature multiple-layer CNT transfer process to build circuits, CNTFETs provide a unique opportunity to enable monolithic 3D ICs. To overcome the mispositioned CNTs and m-CNTs on each layer, the imperfection immune paradigm is extended. Mispositioned CNT-immune design is readily scalable to 3D, and m-CNTs can be removed via the 3D VMR technique described in Reference 55. The left image in **Figure 10** illustrates the process flow for CNT monolithic 3D ICs. This process flow has enabled experimental demonstrations of complex digital logic circuits spanning multiple circuit layers, as shown in Reference 55. Transmission electron microscopy images of these circuits, depicting CNTFETs on three circuit layers, are provided in the right images of Figure 10.

Future outlook

As reviewed in this article, carbon nanotube (CNT) technology has been continuously developed in the past 15 years. From materials, device transport, to large-scale circuit integration, much progress has been made. To push CNTs further into industrial production and make them become part of consumer electronics, many more issues such as reliability and reproducibility need to be considered and evaluated. It will again require material scientists, chemists, electrical engineers, and many other experts from different fields to work together on all these challenges.

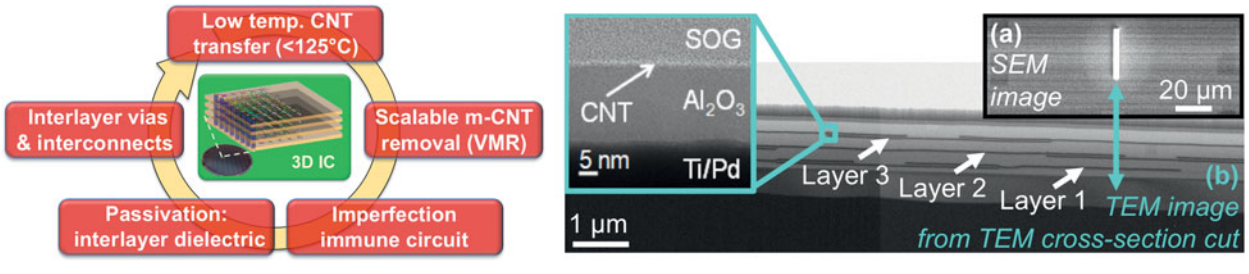


Figure 10. Flow chart for the fabrication of carbon nanotube field-effect transistor (CNTFET) monolithic 3D integrated circuits (ICs). As shown in the inset, a bi-layer of Ti/Pd is used as a local-back-gate with Al_2O_3 as the gate dielectric. Spin-on-glass (SOG) is used as the passivation layer for lower-layer CNFET circuits, such that CNTs can be transferred onto smooth top surfaces for upper-layer CNFET circuit fabrication. All details can be found in Reference 55. Note: IC, integrated circuit; m-CNT, metallic carbon nanotube; VMR, VLSI-compatible metallic CNT removal.

https://doi.org/10.1557/mrs.2014.164 Published online by Cambridge University Press

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https://doi.org/10.1557/mrs.2014.164 Published online by Cambridge University Press