International Journal of Microwave and Wireless Technologies

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High efficiency 35 GHz MMICs based on 0.2 μm AlGaN/GaN HEMT technology

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Research Paper

Cite this article: Cankaya Akoglu B, Sutbas B, Ozbay E (2023). High efficiency 35 GHz MMICs based on 0.2 μm AlGaN/GaN HEMT technology. *International Journal of Microwave and Wireless Technologies* **15**, 384–392. https://doi.org/10.1017/S1759078722000617

Received: 2 February 2022
Revised: 9 May 2022
Accepted: 9 May 2022
First published online: 16 June 2022

Keywords:
Gallium nitride; HEMT; Ka-band; high efficiency; power amplifier; driver amplifier; MMIC

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Abstract

In this paper, two high efficiency monolithic microwave integrated circuits (MMICs) are demonstrated using NANOTAM's in-house *Ka*-band fabrication technology. AlGaN/GaN HEMTs with 0.2 μm gate lengths are characterized, and an output power density of 2.9 W/mm is achieved at 35 GHz. A three-stage driver amplifier MMIC is designed, which has a measured gain higher than 19.3 dB across the frequency band of 33–36 GHz. The driver amplifier exhibits 31.9 dB output power and 26.5% power-added efficiency (PAE) at 35 GHz using 20 V supply voltage with 30% duty cycle. Another two-stage MMIC is realized as a power amplifier with a total output gate periphery of 1.8 mm. The output power and PAE of the power amplifier are measured as 3.91 W and 26.3%, respectively, at 35 GHz using 20 V supply voltage with 30% duty cycle. The high efficiency MMICs presented in this paper exhibit the capabilities of NANOTAM's 0.2 μm AlGaN/GaN on SiC technology.

Introduction

Gallium nitride (GaN) technology has started dominating high power applications, especially in phased-array radars, wireless communication systems, and transmitters at millimeter-wave frequencies. GaN transistors are preferable in terms of high output power thanks to the high breakdown field, high saturation velocity, and superior thermal properties of the material. AlGaN/GaN structures can be grown on SiC substrates, having low lattice mismatch and low thermal expansion mismatch, which are ideal conditions for high power applications. Owing to these properties, AlGaN/GaN HEMTs are being used in many applications, such as high power and high gain amplifiers, as well as robust low noise amplifiers and highly survivable switches. Moreover, usage of GaN processes for transceiver modules is now in demand for a highly compact single aperture for phased array antennas.

The performance of GaN HEMTs for *Ka*-band has been developed over the years, and many monolithic microwave integrated circuits (MMICs) are designed with AlGaN/GaN and InAlGaN/GaN HEMT structures [1–12]. At 35 GHz, a saturated power density of 4 W/mm is achieved for an AlGaN/GaN device with 0.18 μm gate length in [1]. Another AlGaN/GaN device is reported in [2] with a 5 W/mm power density at 35 GHz. In [4], a 40 W MMIC is realized using a process with 4 W/mm output power density at 30 GHz with 28 V operating voltage. Another high power example is given in [5], showing an output power density of 3.2 W/mm and 24% power-added efficiency (PAE) with 24 V operating voltage. The 0.1 μm AlGaN/GaN HEMT on SiC technology is demonstrated in [6] with 4 W output power and 27% PAE from 29 to 31 GHz, where the saturated drain current density is higher than 1600 mA/mm. GaN on Si technology with 0.1 μm gate length is also used for a high frequency MMIC design in [7], showing 5.6 W output power and 30% PAE at 32 GHz with 12 V supply voltage. Using an InAlGaN/GaN structure, a power density of 2.7 W/mm at 30 GHz is achieved in [8]. Another InAlGaN/GaN HEMT work with AlGaN back-barrier introduces an improved epitaxial structure for the reduced recovery time of drain current, which would be favorable, especially for low noise amplifiers in transceivers for radar applications [10]. The limitations of design for large bandwidths at *Ka*-band frequencies are discussed in [11] which shows a design example with 26% PAE using 15 V operating voltage and 50 W/mm drain current. A large bandwidth is obtained in [12] with 15.5 W output power and 16% PAE over 15.6% bandwidth from 26.5 to 31 GHz.

NANOTAM has been developing in-house AlGaN/GaN processes for millimeter-wave applications, with 0.2 μm gate length, using the epitaxial structure grown in the same facility. The fabricated transistor with 4 × 50 μm periphery has a maximum available gain (MAG) of 9 dB at 35 GHz. The average output power density of the fabricated devices is 2.9 W/mm with 34.5% PAE at the same frequency. Two standalone MMICs are designed to achieve high efficiency results at *Ka*-band using the HEMTs fabricated with this process. A three-stage MMIC is designed and realized, which shows a gain higher than 19.3 dB, an output power of 31.9 dB,

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and a PAE of 26.5% at 35 GHz. Also, measurement results show that a two-stage MMIC designed for higher output power exhibits 35.9 dB output power with 26.3% PAE at 35 GHz. These high efficiency values are achieved using 20 V drain voltage with 30% duty cycle in the measurements, which is challenging considering that other works around the same frequency range operate with 10% duty cycle [2, 3, 9]. To compare with the other published work and to show the large-signal performance dependency on duty cycle, PA MMIC is also characterized with 10% duty cycle and continuous wave (CW) conditions at 35 GHz, showing 28.1% and 25.8% PAE, respectively. NANOTAM's 0.2 μm gate length technology capabilities are proven with the presented MMIC designs and measurement results.

In this paper, in-house fabrication technology is detailed in section "GaN fabrication technology". HEMT characterization is discussed in section "HEMT characterization", while MMIC design considerations are explained in section "MMIC design considerations". Measurement results and comparisons with other published work are given in section "Measurement results", and the paper is concluded in section "Conclusion".

GaN fabrication technology

NANOTAM's in-house 0.2 μm AlGaN/GaN fabrication technology is used for *Ka*-band applications. The active and passive devices are fabricated on the epitaxial structure grown by metal-organic chemical vapor deposition (MOCVD) method on a 3-inch SiC substrate. The epitaxial structure is optimized to achieve high performance for *Ka*-band transistors. AlGaN barrier layer is grown with a thickness of 22 nm and an Al concentration of 28.4% to increase 2DEG density as much as possible without any relaxation [13]. The buffer layer is grown with Fe-doping in the structure, with prior knowledge of the effects of the buffer layer's doping properties on the buffer leakages and the trapping mechanism. The existence of deep-acceptor traps in the C-doped buffer results in a high voltage-dependent current collapse, whereas Fe-doping only causes mild current collapse thanks to the lack of these deep-acceptor traps [14]. Moreover, buffer leakage current is smaller in the Fe-doped structures due to the higher energy barrier between the channel and the buffer layer [15].

For active devices, ohmic contacts are formed as non-alloyed by growing InGaN into the AlGaN layer using the MOCVD method to define conducting sources and drains with Cr/Au metal stack. The ohmic contact resistance of the process is around 0.3 Ωmm. The device structure showing the epitaxial layers and regrown ohmic contacts is shown in Fig. 1. The most critical step in the fabrication for higher frequencies is the gate formation, which is performed by an e-beam lithography system. A gate foot length of 200 nm with 500 nm head length is determined for this process, ensuring its uniformity and durability. After patterning the foot and head of T-gates, the foots are formed by a dose of 2000 μC/cm^2 in the e-beam lithography system. The gate formation is finalized by metallization using Ni/Au metals, followed by lift-off operation. The completed gate structure can be seen in Fig. 2. After gate metallization, a Si_3N_4 passivation layer is deposited by plasma-enhanced chemical vapor deposition. Two metal layers of Au metal are used in the process, forming the active device connections and passive structures as metal-insulator-metal (MIM) capacitors and interconnections using air-bridges in between when necessary. MIM capacitors have a capacitance density of 180 pF/mm^2. The fabrication also has a thin film resistor process with a sheet resistance of 30 Ω/□. To have a microstrip

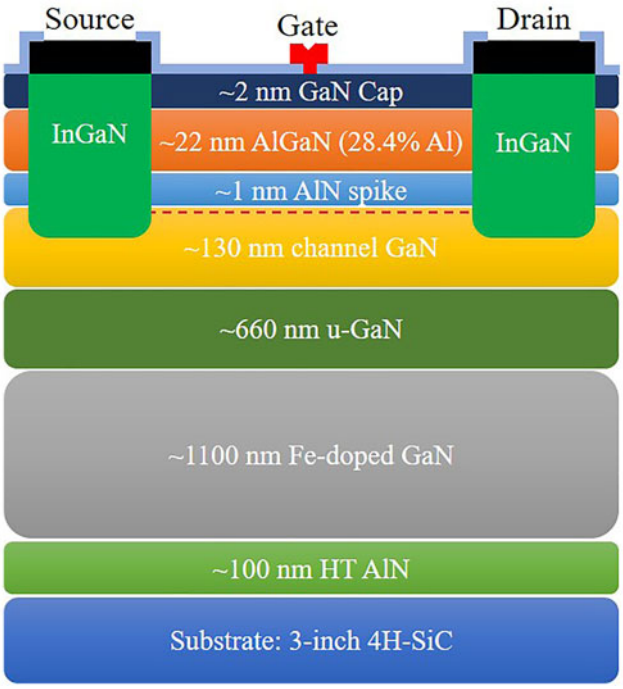


Fig. 1. Device structure showing the epitaxial layers grown by MOCVD and InGaN regrowth for ohmic contacts.

structure for transistors and passive elements, via holes of 85 μm diameter are etched and filled with Au metal after thinning the wafers to 100 μm.

HEMT characterization

HEMTs, fabricated using NANOTAM's 0.2 μm GaN on SiC technology, show an average maximum drain current of 1.05 A/mm with an average transconductance of 280 mS/mm. The gate and drain leakages of such transistors are measured to be 21 μA/mm and 40 μA/mm, respectively, at 20 V drain voltage. Transistors of 4, 6, and 8 fingers with 50 and 75 μm peripheries exhibit MAGs ranging from 6 to 9 dB at 35 GHz, measured under CW operation with 20 V drain voltage and 100 mA/mm drain current. Cut-off frequency (f_T) and maximum oscillation

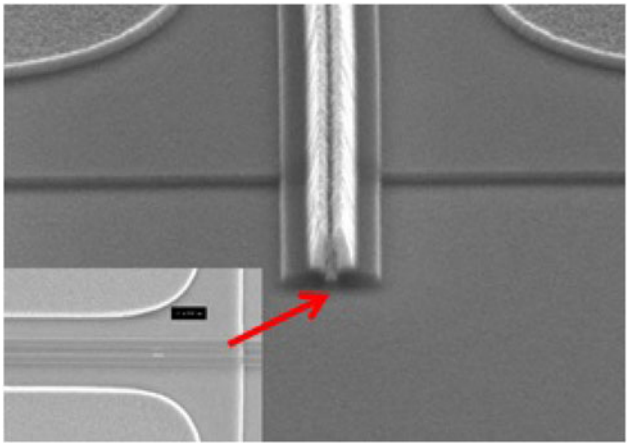


Fig. 2. SEM image of T-gate of a *Ka*-band HEMT, showing its 200 nm gate foot.

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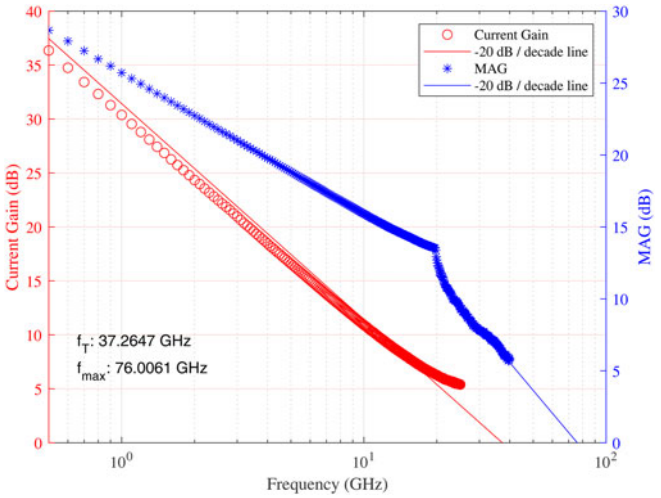


Fig. 3. Current gain and MAG graphs and extrapolated fits for f_T and f_{max} calculations of a 6 × 75 μm HEMT.

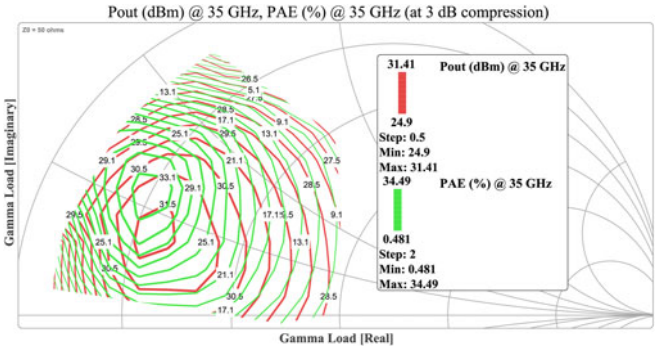


Fig. 5. Output power and PAE contours of a 6 × 75 μm HEMT at 35 GHz at 3 dB gain compression.

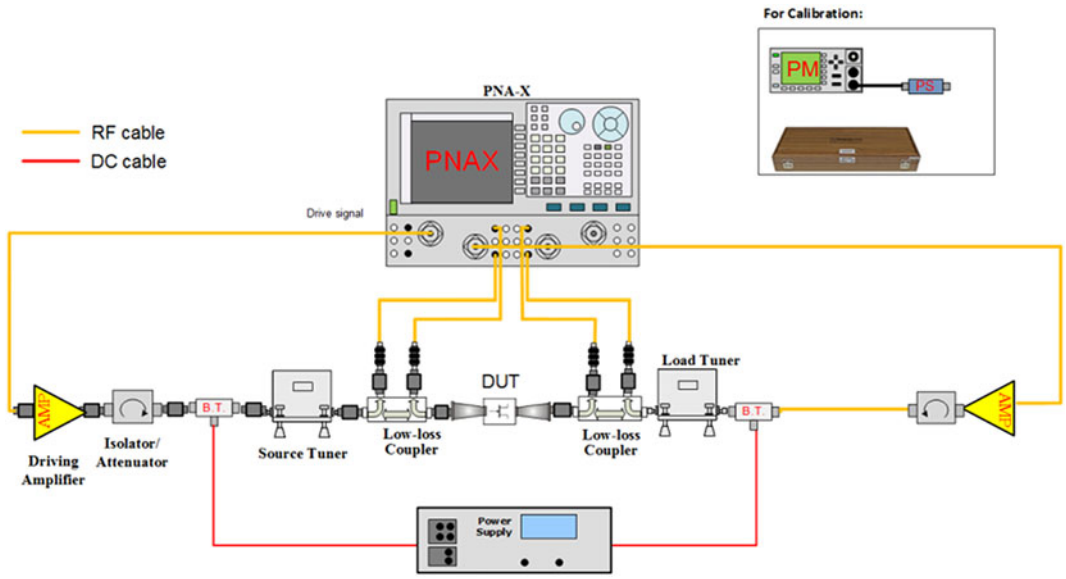


Fig. 4. Schematic of the hybrid vector-based load-pull measurement setup.

frequency (f_{max}) of transistors are also characterized using small-signal measurement data by extrapolating the current gain and MAG curves. Figure 3 shows the results for a 6 × 75 μm HEMT, where f_T is calculated as 37.3 GHz and f_{max} is calculated as 76 GHz.

The large-signal measurements of the devices are performed using a hybrid vector-based load-pull setup with a pulse width of 33 μs and 30% duty cycle at 35 GHz. The load impedance seen by the device under test (DUT), that is the ratio of the reflected wave by the forward-traveling wave, is limited by the losses in the system. Moreover, the optimum load impedance of the transistor changes according to the bias condition and the parasitic components, which makes it also dependent on the frequency of interest. For higher frequencies, it becomes impossible to determine the optimum load impedances of transistors using passive load-pull systems for small devices. To overcome this issue, a hybrid load-pull system is used to determine the optimum load and source impedances. The reflected wave at the output side of the device is boosted by injecting an external signal to overcome the losses of the setup in a hybrid load-pull measurement system. Therefore, impedance points that are not achievable using a conventional passive vector-based load-pull setup can be presented to the DUT to obtain optimum impedance points for maximum output power, efficiency, and gain. The schematic of the hybrid vector-based load-pull measurement setup is shown in Fig. 4. The setup utilizes PNA-X from Keysight Technologies[1], tuners from Maury Microwave Technologies[2], driving amplifiers from Exodus Advanced Communications[3], and IVCAD software of AMCAD Engineering[4].

Figure 5 shows the output power and PAE contours of a 6 × 75 μm transistor at 35 GHz at room temperature. The

[1]Keysight Technologies, Inc., Santa Rosa, CA 95403, USA
[2]Maury Microwave Technologies, Ontario, CA 2900, USA
[3]Exodus Advanced Communications, Las Vegas, NV 89120, USA
[4]AMCAD Engineering, Limoges 87068, France

https://doi.org/10.1017/S1759078722000617 Published online by Cambridge University Press

maximum output power of 31.4 dB is achieved at 3 dB gain compression at (12+j9) Ω load impedance, while the maximum PAE is 34.5% at (10+j14) Ω load impedance, which is close enough to the optimum impedance for the maximum output power. Large-signal measurements of various HEMTs from the same tape-out show an average output power density of 2.9 W/mm.

MMIC design considerations

Two MMIC designs, a driver amplifier (DA) and a power amplifier (PA), are completed using the GaN HEMT process to benchmark the technology at *Ka*-band frequencies. The designs are based on CW small-signal and pulsed large-signal characteristics of the unit transistors.

Driver amplifier MMIC design

A three-stage MMIC is designed to achieve high gain with moderate output power to drive the power amplifier in an amplifier chain. Transistors with sizes of 4 × 75 μm are used in each stage, showing a MAG of 7.9 dB at 35 GHz with 20 V drain voltage and 30 mA drain current. Transistors are stabilized unconditionally down to 1.7 GHz in even-mode using parallel *RC* networks with values of 120 Ω and 0.25 pF at their gates. The stability (K) factor and the MAG of the transistor with and without this *RC* network is given in Fig. 6. Low-frequency stability is achieved with the series resistors (values of 14 Ω, 10 Ω, and 15 Ω) and shunt *RC* networks at gate bias lines which are included after designing the matching networks and analyzing the stability parameters (μ and μ') of each stage [16]. The stability parameters are increased from below 1 to above 1 using the resistive components in the gate bias lines for all three stages. The simulation results for the second stage of MMIC are shown in Fig. 7.

Two transistors are paralleled at the output stage, and the output matching network is optimized to get the maximum output power from these transistors. The input and interstage matching networks are designed for maximum gain from the three stages. Odd-mode stability analysis is performed by checking the oscillation conditions for each possible odd-mode excitation, as described in [17] and detailed in [18]. The conditions considered

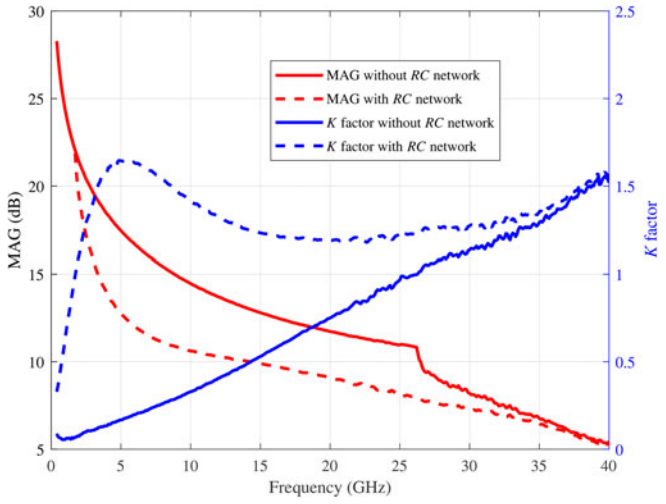


Fig. 6. MAG and K factor of the 4 × 75 μm HEMT with and without the stability network.

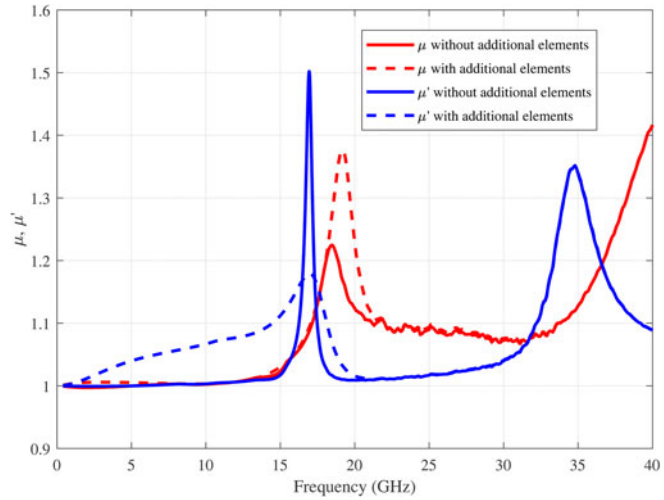


Fig. 7. Simulated even-mode stability parameters (μ and μ') of the second stage of DA MMIC with and without additional elements on the gate bias line.

to avoid odd-mode instability are given in (1), where the input and output impedances are calculated by splitting them into two from the parallel transistors' gate or drain sides.

$$\begin{aligned} \mathrm{Re}(Z_{\mathrm{o,n,in}} + Z_{\mathrm{o,n,out}}) < 0, \\ \mathrm{Im}(Z_{\mathrm{o,n,in}} + Z_{\mathrm{o,n,out}}) = 0. \end{aligned} \tag{1}$$

Checking the odd-mode oscillation mode of [+, −] for the second and third stages, the odd-mode suppression resistors are placed between the second and third stage transistors to ensure odd-mode stability. The optimized values are 10 Ω and 5 Ω for the gate and drain sides of the second stage, respectively, and 12 Ω and 5 Ω for the gate and drain sides of the third stage. As shown in Fig. 8, real part of the sum of impedance values seen from the gate and drain sides of the transistors for the second and third stages are above zero for the entire simulation band, which ensures the odd-mode stability. Simulations and analysis are performed using PathWave Advanced Design System (ADS) from Keysight Technologies[1]. The chip design is finalized by adding odd-mode resistors. Figure 9 shows the schematic of the designed DA MMIC.

Power amplifier MMIC design

PA MMIC is designed as two-stage with a larger periphery device compared to DA MMIC to obtain a higher output power performance. The output stage of PA MMIC consists of four parallel transistors of 6 × 75 μm. MAG of the unit transistor is 7.1 dB at 35 GHz when it is biased with 20 V drain voltage and 45 mA drain current. The drive ratio is chosen as 2:1. The load impedances of the transistors are matched for optimum efficiency together with output power at each stage. Second stage transistors are used with parallel *RC* networks with values of 130 Ω and 0.42 pF for even-mode stability, while the first stage transistors are stabilized using resistors of 45 Ω at the gate bias lines. Odd-mode stability is also analyzed for this MMIC considering all odd oscillation modes for both stages, e.g., [+, −, −, +], [+, +, −, −], and [+, −, +, −] modes for the second stage. In the analysis, the variation of transistors throughout the MMIC is also checked by introducing phase disturbances. The odd-mode stability of the MMIC is achieved by utilizing small

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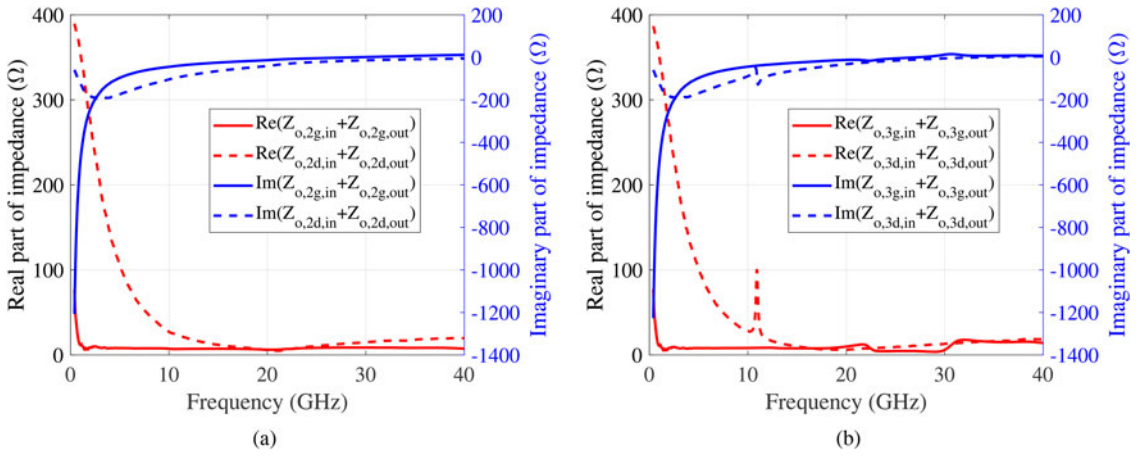


Fig. 8. Stability check for [+ , −] odd excitation mode: (a) at the gate side (2g) and at the drain side (2d) of the second stage and (b) at the gate side (3g) and at the drain side (3d) of the third stage of DA MMIC.

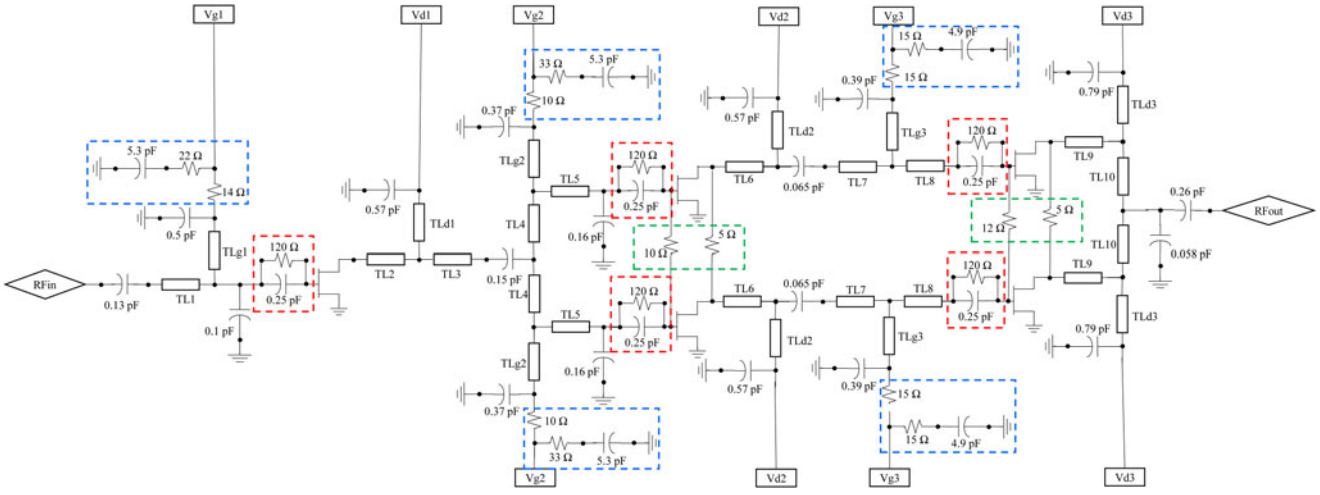


Fig. 9. Schematic of the designed DA MMIC, showing even-mode stability circuits at the gate (red) and at the biasing (blue) with odd-mode stability resistors (green).

odd-mode resistors, approximately 10 Ω, between gates and drains of the parallel transistors. The schematic of the designed PA MMIC is given in Fig. 10.

Measurement results

The designed MMICs are fabricated using the process described in section "GaN fabrication technology" on a 3-inch SiC wafer. The microscope images of the fabricated MMICs are given in Fig. 11. The chip size of the designed DA MMIC is 4 mm × 2.4 mm, and the size of PA MMIC is smaller than 4.4 mm × 2.1 mm. Small-signal measurements are performed on-wafer under CW operation at room temperature. On the other hand, large-signal responses of MMICs are measured with a pulse width of 33 μm and 30% duty cycle at room temperature, again on-wafer.

For the DA MMIC, the bias point of its each transistor is set to 20 V drain voltage with 30 mA drain current. The small-signal measurement results are shown in Fig. 12, together with the electromagnetic (EM) simulations. In the measurements, the achieved gain is between 19.3 and 23.4 dB for the desired frequency band of 33–36 GHz. Measured gain of MMIC is better than the simulated one, which is between 18.2 and 20.4 dB, while their peaks are at the same frequency. Measured input return loss (IRL) and output return loss (ORL) are better than 6 and 8.5 dB at 35 GHz, respectively. In the MMIC design, a via-hole is shared between the paralleled transistors of the output stage, while the unit transistors are characterized as single cells. This may be the reason for the difference between the simulated and measured gain, where the measured gain is higher.

Large-signal measurement of DA MMIC is performed at 35 GHz, and the measurement results are given in Fig. 13. The DA MMIC achieves 31.9 dB output power and 26.5% PAE at 5 dB gain compression, with a large-signal gain higher than 18.8 dB. Moreover, P1 dB of the DA is measured as 26.5 dB.

PA MMIC is characterized with 20 V drain voltage and 45 mA drain current for all transistors. As a two-stage circuit, the measured gain is higher than 9.9 dB for the frequency range of 33–36 GHz, with a peak of 12.9 dB. IRL and ORL are measured as better than 10 and 7 dB at 35 GHz, respectively. The reason for the lower gain in the simulations may also be the shared via-

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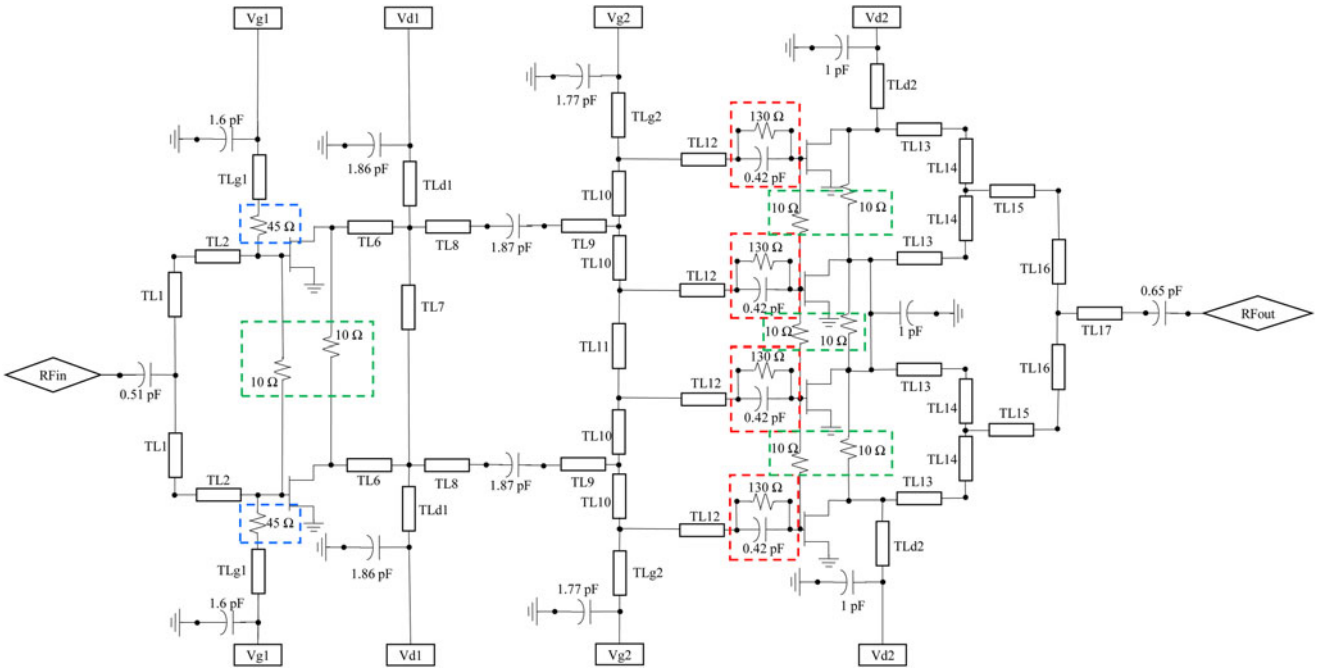


Fig. 10. Schematic of the designed PA MMIC, showing even-mode stability circuits at the gate (red) and at the biasing (blue) with odd-mode stability resistors (green).

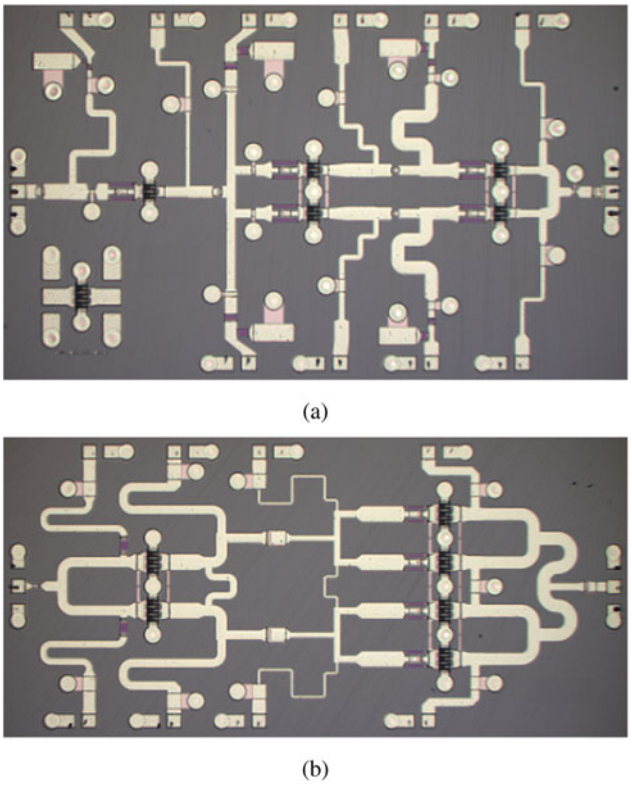


Fig. 11. Microscope images of fabricated MMICs: (a) DA MMIC (size of 4 mm × 2.4 mm) and (b) PA MMIC (size of 4.4 mm × 2.1 mm).

holes at the second stage, while the difference is larger compared to DA MMIC results due to the four parallel transistors of PA MMIC. Small-signal measurement and simulation results are given in Fig. 14 for the PA MMIC.

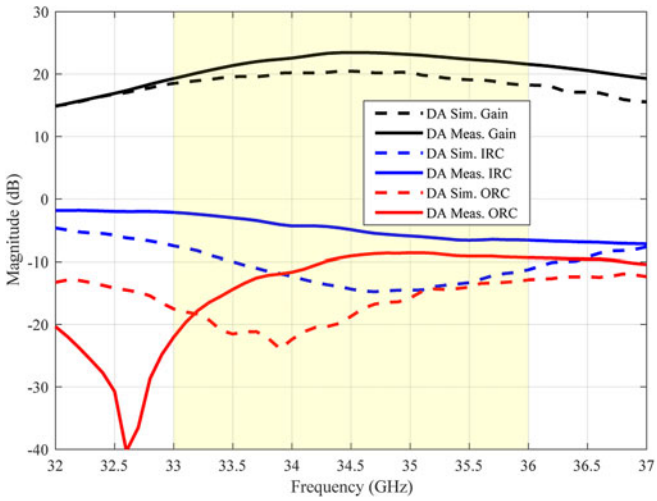


Fig. 12. Small-signal simulation and measurement results of the DA MMIC.

Load-pull measurement of PA MMIC is also performed with a pulsed signal of 30% duty cycle at 35 GHz at room temperature. Figure 15 shows the large-signal measurement results of the PA MMIC versus available input power. The saturated output power of 35.93 dB is achieved when the gain is compressed by 7.4 dB, which is 3.91 W at 35 GHz. The maximum PAE is 26.3% at 3 dB gain compression.

The power measurements of PA MMIC are also performed with a duty cycle of 10% and under CW conditions. The output power and PAE results are compared for the three measurement conditions in Fig. 16. The output power results are 3.95 W, 3.91 W, and 3.54 W for 10% duty cycle, 30% duty cycle, and CW condition, respectively, while peak PAE values are 28.1%, 26.3%, and 25.8%, respectively. As the duty ratios of RF signal

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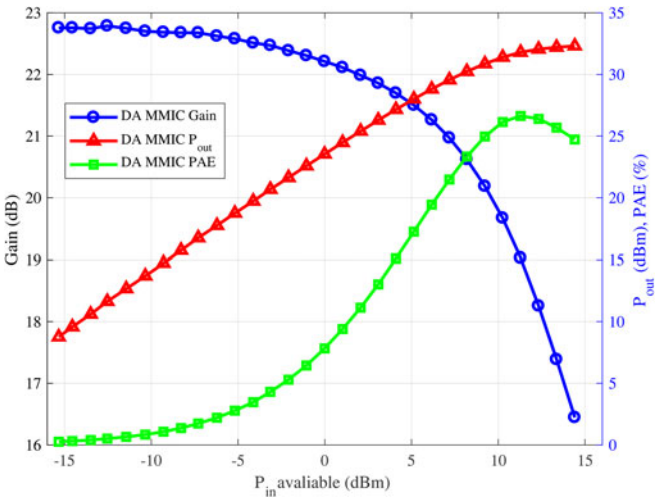


Fig. 13. Measured gain, output power, and PAE of the DA MMIC versus available input power at 35 GHz.

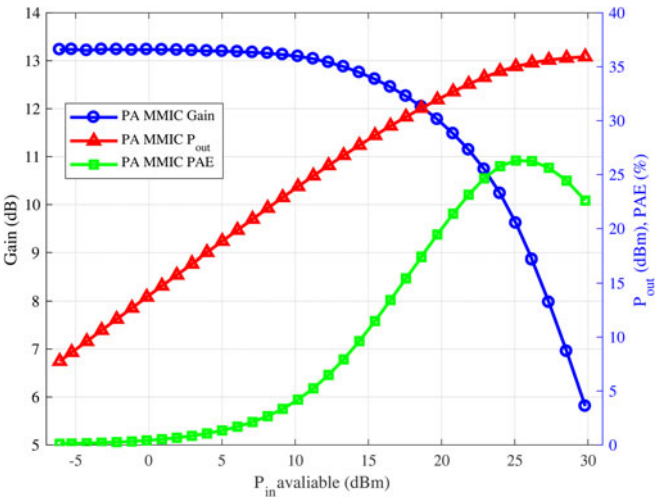


Fig. 15. Measured gain, output power, and PAE of the PA MMIC versus available input power at 35 GHz for 30% duty cycle.

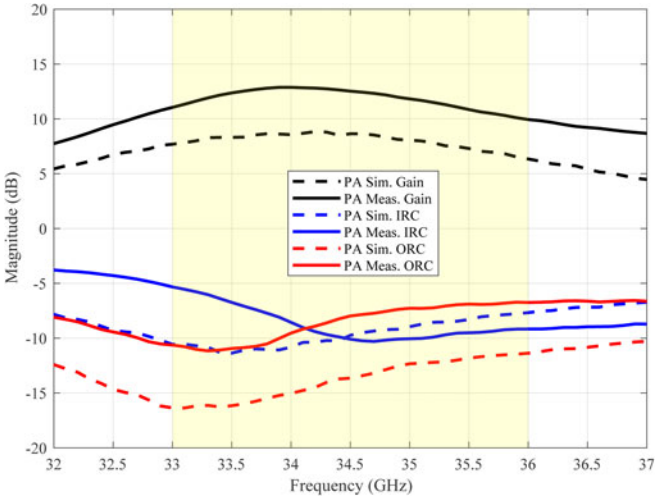


Fig. 14. Small-signal simulation and measurement results of the PA MMIC.

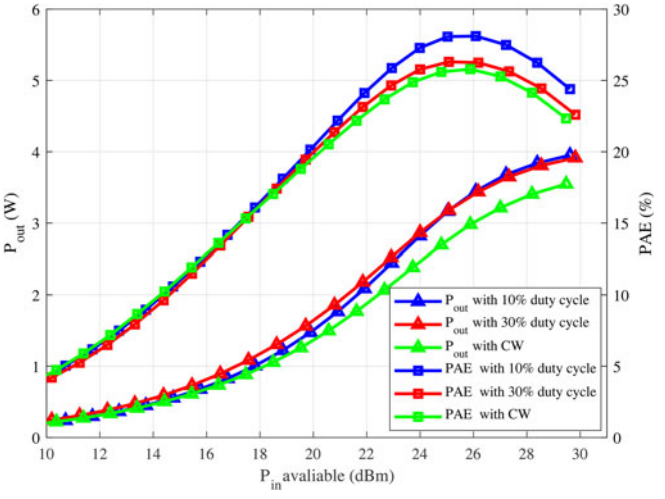


Fig. 16. Measured output power and PAE of the PA MMIC for 10% duty cycle, 30% duty cycle, and CW conditions at 35 GHz.

Table 1. A comparison of designed MMICs with other GaN-based amplifiers at *Ka*-band

Ref.	Number of Stages	Frequency (GHz)	Operating condition	Supply voltage (V)	Gain (dB)	Max. P_{out} (W)	Max. $P_{density}$ (W/mm)	Peak PAE (%)
[1]	2	35	CW	24	12	3.8	3.1	23
[2]	3	35	10%	24	26	15	3.3	30
[3]	2	30	10%	28	10	20	3.1	16
[9]	2	35	10%	20	17	4.5	2.5	25
[5]	3	34	10%	24	26	31	3.2	24
[11]	3	31	N/A	15	20	6.5	1.7	26
DA	3	35	30%	20	23.1	1.5	2.6	26.5
PA	2	35	10% 30% CW	20	11.8	3.95 3.91 3.54	2.19 2.17 1.97	28.1 26.3 25.8

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and DC supply increase, all transistors heat up more, causing a decrease in the efficiency and output power values. The efficiency improvement from 30% to 10% duty cycle is 2% at the peak, while CW condition causes only 0.5% degradation of PAE.

Table 1 shows the comparison to some recent MMICs based on AlGaN/GaN HEMTs at similar frequencies. The power density of each MMIC is calculated taking the total gate periphery of the output stages into account. Two MMICs of this work exhibit high PAE values, higher than 26%, with a 20 V supply voltage of 30% duty cycle. PA MMIC also shows high PAE of 28.1% with 10% duty cycle and PAE of 25.8% with CW condition. MMIC of [11] shows a comparable PAE of 26% with the proposed MMICs, however the operating condition is not mentioned. Besides, the efficiencies of the proposed MMICs are highest after [2], which has a unit device with 40% PAE, while our unit device shows a maximum PAE of 34.5% at the optimum load impedance at 35 GHz. The presented MMICs also show high power densities as 2.6 W/mm and 2.2 W/mm, considering the maximum power density available from the unit devices.

Conclusion

Aiming *Ka*-band applications, two MMICs are designed and realized using NANOTAM's 0.2 μm AlGaN/GaN on SiC technology. DA and PA MMICs are optimized for 35 GHz frequency for maximum output power and efficiency, while having a bandwidth from 33 to 36 GHz in the small-signal operation. Three-stage DA MMIC has a gain higher than 19.3 dB with a variation of ±2 dB. It exhibits 31.9 dB output power with a PAE of 26.5% at 5 dB gain compression at 35 GHz. Having an output periphery of 0.6 mm, the output power density is 2.6 W/mm for the DA MMIC. Two-stage PA MMIC shows a minimum small-signal gain of 9.9 dB for the desired frequency band, having a ripple of 3 dB. The output power and PAE of this MMIC are measured as 3.91 W and 26.3%, respectively, at 35 GHz under pulsed operation with 30% duty cycle. The total output periphery of the PA MMIC is 1.8 mm, yielding an output power density of 2.2 W/mm which is lower than that of DA MMIC because of the increasing combining loss of the output matching network while the number of devices in parallel increases. The designed and realized MMICs exhibit the capabilities of NANOTAM's 0.2 μm AlGaN/GaN on SiC technology with high power-added efficiency values while maintaining comparable output power with recent works.

Acknowledgements. The authors would like to thank RF Design Group of NANOTAM for their help in the measurements. The authors would also like to thank the fabrication team of NANOTAM for fabricating the devices.

Conflict of interest. None.

References

1. **Darwish A, Boutros K, Luo B, Huebschman B, Viveiros E and Hung H**. 4-Watt Ka-band AlGaN/GaN power amplifier MMIC. IEEE MTT-S International Microwave Symposium Digest, 2006, pp. 730–733.
2. **Yu X, Tao H and Hong W**. A Ka band 15 W power amplifier MMIC based on GaN HEMT technology. IEEE International Workshop on Electromagnetics: Applications and Student Innovation Competition (iWEM), 2016, pp. 1–3.
3. **Ng C, Takagi K, Senju T, Matsushita K, Sakurai H, Onodera K, Nakanishi S, Kuroda K and Soejima T**. A 20-watt Ka-band GaN high power amplifier MMIC. Proceedings of European Microwave Conference. Rome, Italy, 2014, pp. 1348–1351.
4. **Din S, Wojtowicz M and Siddiqui M**. High power and high efficiency Ka band power amplifier. IEEE MTT-S International Microwave Symposium, 2015, pp. 1–4.
5. **Litchfield M and Dugas D**. 10 W and 30W, 32–37 GHz, Ka-band GaN MMIC power amplifiers on SiC. IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2021, pp. 1–4.
6. **Chéron J, Campovecchio M, Quéré R, Schwantuschke D, Quay R and Ambacher O**. High-efficiency power amplifier MMICs in 100 nm GaN technology at Ka-band frequencies. 2013 European Microwave Conference, 2013, pp. 1463–1466.
7. **Leblanc R, Ibeas NS, Gasmi A, Auvray F, Poulain J, Lecourt F, Dagher G and Frijlink P**. 6W Ka band power amplifier and 1.2 dB NF X-band amplifier using a 100 nm GaN/Si process. 2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), 2016, pp. 1–4.
8. **Potier C, Piotrowicz S, Chang C, Patard O, Trinh-Xuan L, Gruenenpuett J, Gamarra P, Altuntas P, Chartier E, Jacquet J, Lacam C, Michel N, Dua C, Oualli M and Delage SL**. 10 W Ka band MMIC power amplifiers based on InAlGaN/GaN HEMT technology. Proceedings of European Microwave Conference. Paris, France, 2019, pp, 824–827.
9. **Chen S, Nayak S, Campbell C and Reese E**. High efficiency 5 W/10 W 32–38 GHz power amplifier MMICs utilizing advanced 0.15 μm GaN HEMT technology. IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), 2016, pp. 1–4.
10. **Piotrowicz S, Jacquet J, Gamarra P, Patard O, Dua C, Chartier E, Michel N, Oualli M, Lacam C, Potier C, Altuntas P and Delage S** (2018) InAlGaN/GaN with AlGaN back-barrier HEMT technology on SiC for Ka-band applications. *International Journal of Microwave and Wireless Technologies*, **10**, 39–46.
11. **Neininger P, John L, Thome F, Friesicke C, Brückner P, Quay R and Zwick T**. Limitations and implementation strategies of interstage matching in a 6-W, 28–38-GHz GaN power amplifier MMIC. IEEE Transactions on Microwave Theory and Techniques, Vol. 69, no. 5, 2021, pp. 2541–2553.
12. **Nakatani K, Yamaguchi Y, Hangai M and Shinjo S**. A Ka-band CW 15.5 W 15.6% fractional bandwidth GaN power amplifier MMIC using wideband BPF inter-stage matching network. IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2019, pp. 1–4.
13. **Medjdoub F**. Gallium nitride (GaN): physics, devices, and technology. Devices, circuits, and systems, Taylor & Francis, 2015.
14. **Uttam S, Towhidur R and Yuewei Z**. Wide bandgap semiconductor electronics and devices. Selected topics in electronics and systems, World Scientific Publishing Company, 2019.
15. **Kawada Y, Hanawa H and Horio K** (2017) Effects of acceptors in a Fe-doped buffer layer on breakdown characteristics of AlGaN/GaN high electron mobility transistors with a high-k passivation layer. *Japanese Journal of Applied Physics*, **56**, 108003.
16. **Akoglu BC** (2020) GaN HEMT based MMIC design and fabrication for Ka-band applications, MS thesis, Department of Electrical and Electronics Engineering, Bilkent University, Ankara, Turkey.
17. **Freitag RG**. A unified analysis of MMIC power amplifier stability. IEEE MTT-S Microwave Symposium Digest, Vol. 1, 1992, pp. 297–300.
18. **Jankowski M, Limiti E and Longhi PE**. Freitag method application to PA stability test. Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits, 2008, pp. 14–152.



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https://doi.org/10.1017/S1759078722000617 Published online by Cambridge University Press

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https://doi.org/10.1017/S1759078722000617 Published online by Cambridge University Press