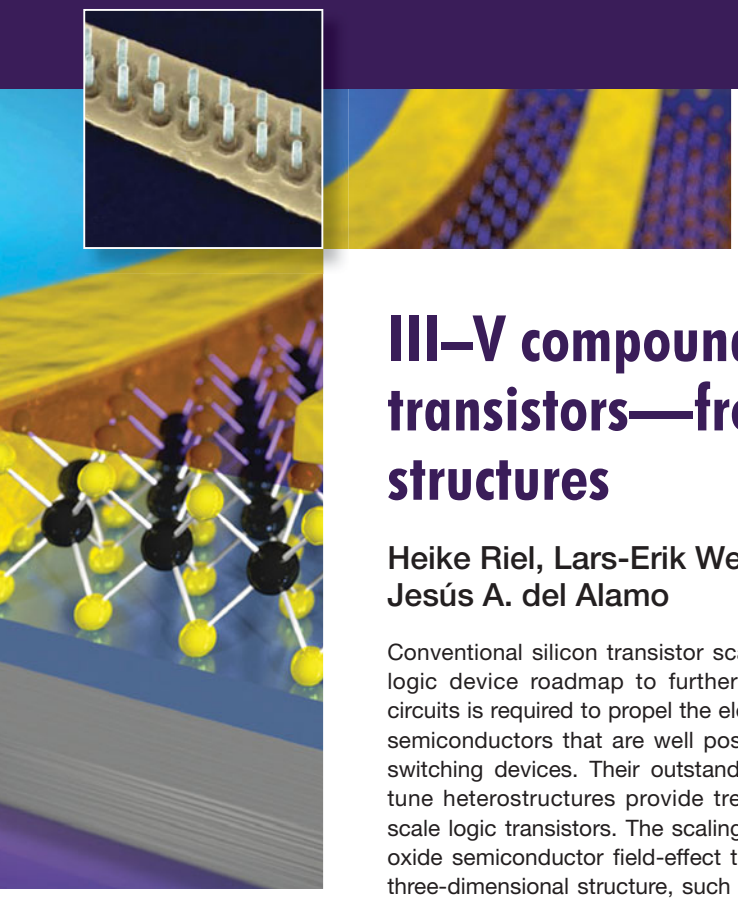


III–V compound semiconductor transistors—from planar to nanowire structures

Heike Riel, Lars-Erik Wernersson, Minghwei Hong, and Jesús A. del Alamo

Conventional silicon transistor scaling is fast approaching its limits. An extension of the logic device roadmap to further improve future performance increases of integrated circuits is required to propel the electronics industry. Attention is turning to III–V compound semiconductors that are well positioned to replace silicon as the base material in logic switching devices. Their outstanding electron transport properties and the possibility to tune heterostructures provide tremendous opportunities to engineer novel nanometer-scale logic transistors. The scaling constraints require an evolution from planar III–V metal oxide semiconductor field-effect transistors (MOSFETs) toward transistor channels with a three-dimensional structure, such as nanowire FETs, to achieve future performance needs for complementary metal oxide semiconductor (CMOS) nodes beyond 10 nm. Further device innovations are required to increase energy efficiency. This could be addressed by tunnel FETs (TFETs), which rely on interband tunneling and thus require advanced III–V heterostructures for optimized performance. This article describes the challenges and recent progress toward the development of III–V MOSFETs and heterostructure TFETs—from planar to nanowire devices—integrated on a silicon platform to make these technologies suitable for future CMOS applications.

Introduction

For more than 40 years, miniaturization of semiconductor technology has been the driving force for the success of information technology. A continuous decrease in transistor dimensions has led to higher device densities and enabled extraordinary improvements in logic performance together with a cost reduction for microprocessors. Today, however, scaling is seriously challenged, as silicon (Si) complementary metal oxide semiconductor (CMOS) field-effect transistors (FETs) are reaching their fundamental physical limits.[1,2] Increasing leakage currents and the saturation of supply voltage scaling at around 0.8–0.9 V result in high power consumption—the largest problem of advanced CMOS technology today.[2–5] Thus, future scaling will require reducing the supply voltage to lower the power consumption. New strategies such as the use of innovative device architectures, novel materials, and new device operation mechanisms are needed on the Si platform to energize the future roadmap and enable continued dimensional scaling and required operation voltage reduction without compromising performance.

Implementing novel FET architectures—switching from a planar channel to a three-dimensional (3D) fin-like and nanowire (NW) channel (see **Figure 1**a)—is the first disruptive technology the Si industry is currently taking to enable the next nodes of scaling below the 20 nm gate length. This device evolution, starting with a thin fin covered by the gate on two or three sides (FinFET or Trigate-FET, respectively) and moving to NW FETs with a cylindrical gate-all-around (GAA) channel, as shown in Figure 1a, results in increasing the electrostatic integrity.[6,7] The improved electrostatic gate control minimizes short-channel effects (SCEs) that degrade the ideal metal oxide semiconductor field-effect transistor (MOSFET) characteristics and allows a steeper transition from the OFF- to the ON-state (see Figure 1b), which is crucial to

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minimize the supply voltage and OFF-state power consumption. The steepness of the transition around threshold is measured by the subthreshold swing, *SS* (see the yellow triangle in Figure 1b). This is a key figure of merit in logic devices; *SS*, at best, has a value of 60 mV/decade at room temperature. Thus, minimizing the SCEs achieved by the evolution from planar to 3D device architecture enables devices with a shorter gate length and smaller footprint.[6,8]

Reducing the operating voltage without loss in performance, however, demands further disruptive technologies, such as implementing new channel materials that can achieve higher currents than Si FETs do at the same voltage (see blue and green lines in Figure 1b).[9,10] In nanoscale FETs, the ON-current, I_{on}, is determined by the product of the injection velocity and the density of states.[11,12] In that respect, III–V compound materials such as InAs and InGaAs are very attractive for *n*-channel MOSFETs.[9] Their very high electron injection velocity (see Figure 1c), in combination with a reasonable electron density of states, promises to deliver high I_{on} at a supply voltage lower than that of Si FETs.[13] The injection velocity of InGaAs is more than twice that of Si MOSFETs even at half the operating voltage, see Figure 1c. For *p*-channel MOSFETs, Ge[14] and III–V materials such as GaSb,[15] InSb,[16] and InGaSb[17] are promising materials to achieve the required performance improvements. Thus, implementing high-mobility channel materials onto silicon will present a second disruptive technology change.

Scaling the supply voltage even further (i.e., below 0.5 V) while maintaining a high I_{on} and low OFF-current, I_{off}, can only be achieved by increasing the turn-on steepness of the device, which means decreasing the subthreshold swing below the 60-mV/decade limit of MOSFETs (Figure 1b). This will require a fundamental change in the operation mechanism.[5,18] Tunnel FETs (TFETs) avoid this limit by using quantum-mechanical band-to-band tunneling (BTBT), where charge carriers tunnel from one energy band to another energy band, rather than thermally injecting charge carriers into the channel.[19,20] Today, TFETs represent the most promising steep-slope switch candidate, having the potential to use a supply voltage of about 0.3 V, thereby offering significant power dissipation savings. Recent TFET performance results indicate that III–V compound semiconductors and their heterostructures are crucial materials for this third disruptive technology transformation.

In this article, we highlight recent scientific and technological progress achieved in III–V MOSFETs and TFETs following the evolution from planar to 3D device structures integrated on silicon, and we point out the challenges still to be overcome to make these technologies suitable for future CMOS applications. In particular, the integration of these structures on Si will be key to make III–V logic a success.

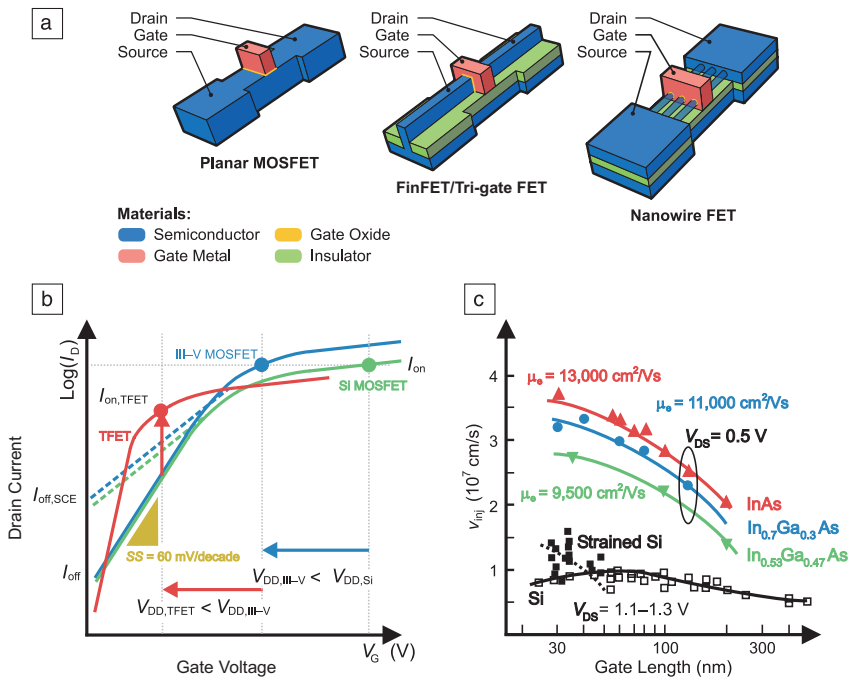


Figure 1. (a) Evolution of field-effect transistor (FET) architectures with, from left to right, increasing electrostatic integrity and scalability. (b) Qualitative comparison of the influence of the material, device architecture, and injection mechanisms on the transistor transfer characteristics ($\log(I_D)$–V_G with drain current I_D and gate voltage V_G). Because of higher mobility, the III–V metal oxide semiconductor field-effect transistors (MOSFETs) can deliver higher currents than Si MOSFETs at the same voltage. Thus, to achieve the same ON-current, I_{on}, the III–V MOSFET can be operated at a lower supply voltage, $V_{DD,III-V}$, than the Si MOSFET with supply voltage $V_{DD,Si}$ ($V_{DD,III-V} < V_{DD,Si}$). Short-channel effects (SCEs) degrade the device characteristics (dashed lines) leading to higher OFF-current, $I_{off,SCE}$, compared with the OFF-current of FETs without SCEs, I_{off}. Tunnel field-effect transistors (TFETs) can achieve a steep slope in the transfer characteristics (red line) with a subthreshold swing $SS < 60$ mV/decade and thus significantly reduce the TFET operating voltage, $V_{DD,TFET}$ compared to III–V MOSFETs ($V_{DD,TFET} < V_{DD,III-V}$). Although the value of the TFET ON-current, $I_{on,TFET}$ may be lower than the I_{on} of Si and III–V MOSFETs, it can be achieved at a much smaller voltage, $V_{DD,TFET}$. (c) Electron injection velocity, v_{inj}, for InAs and InGaAs high-electron-mobility transistors (HEMTs) with different channel compositions and for Si MOSFETs as a function of gate length. The III–V HEMTs are measured at a source-drain voltage $V_{DS} = 0.5$ V, the Si MOSFETs at $V_{DS} = (1.1–1.3)$ V. InGaAs with different indium composition possesses a significantly higher electron injection velocity than Si (unstrained and strained) leading to higher ON-currents. Increasing indium content in InGaAs yields higher electron mobility, μ_e and thus higher v_{inj}. (c) Reproduced with permission from Reference 9. © 2011 Nature Publishing Group.

Planar III–V MOSFETs

N-type InGaAs MOSFETs

InGaAs and InAs have been used for many years for high-speed and high-frequency electronic devices, in particular as high-electron-mobility transistors (HEMTs), in which modulation doping in a heterostructure is exploited to achieve high electron mobility.[21] Mature HEMT technology intrinsically suffers from high gate leakage

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and is thus not the best option for highly scaled devices such as MOSFETs.[22] However, it has acted as an excellent model system in demonstrating the superior properties of III–Vs and thus has helped to push the development of III–V CMOS technology.

Figure 2 shows the remarkable recent progress achieved for InGaAs MOSFETs (with the InAs composition anywhere between 0 and 1) by contrasting it with the relatively well-established InGaAs HEMTs.[23] InGaAs MOSFETs have now matched the highest transconductance, g_m ($g_m = dI_D/dV_{GS}$ at constant V_{DS} with drain current, I_D, source-gate voltage, V_{GS}, and source-drain voltage, V_{DS}) ever obtained in HEMTs (Figure 2a).[24–26] Crucial for this were significant improvements made in two critical areas of InGaAs MOSFETs: the gate stack and the parasitic resistance. Regarding the gate stack, the excellent scalability of the gate oxide thickness has greatly boosted channel charge control by the gate. The parasitic resistance, on the other hand, consists of contact resistance, source-drain extension resistance, and heterojunction barrier resistance. It is this last component that is greatly improved in MOSFETs with respect to HEMTs. In fact, InGaAs MOSFETs today show a smaller ON-resistance than HEMTs (Figure 2b). In spite of this impressive recent progress, a logic InGaAs MOSFET technology ready for insertion into a sub-10-nm CMOS node still needs significant improvements in the gate stack and the parasitic resistances and faces numerous challenges with the integration of III–V on Si.

The dielectric/III–V semiconductor interface

The core of a MOSFET is the gate stack, which is of utmost significance to the device performance. The gate stack is composed of a metal gate and a high-κ dielectric barrier on top of the semiconductor channel, and its quality is crucial for effectively modulating the electrostatic potential inside the semiconductor.[27] Achieving a high-quality gate stack requires a high-permittivity dielectric free of trapped charges and other defects that is appropriately scaled in layer thickness, possesses a smooth oxide–semiconductor interface with few interfacial imperfections, and has high thermal stability. For the electrical characteristics of III–V MOSFETs, the interface state density, D_{it}, and the equivalent oxide thickness (EOT or equivalent thickness of SiO_2 that has the same capacitance per unit area) are particularly important.[28] Interface states are electronic states at the semiconductor/dielectric interface occurring because of non-ideal bonding between the two. They can shift the threshold voltage, degrade the channel mobility, increase the subthreshold swing and thus reduce I_{on} for a given I_{off}, and also be a source of instability.[27] For high-performance scaled MOSFETs, the gate dielectric has to be appropriately scaled with an EOT far below 1 nm to achieve strong electrostatic gate coupling.

Whereas the development of Si technology has had the advantage of its native oxide SiO_2, the native oxides of III–V materials easily result in Fermi-level pinning,[29] and thus the gate is unable to control the channel charge. This was the reason why III–V MOSFETs did not progress in performance for a long time. Early discoveries toward unpinning the Fermi level were based on the *in situ* deposition of oxides such as $Ga_2O_3(Gd_2O_3)$ [GGO][30,31] and Gd_2O_3[32] on GaAs. Tremendous progress has been achieved in the past few years in preparing and understanding dielectric/III–V interfaces electronically[33] and electrically.[34,35] Perfecting the high-κ dielectric/III–V interfaces to lower the D_{it} and to improve the thermal stability at high temperatures has resulted in improved device performance.[36–39] An important breakthrough was achieved by introducing atomic layer deposition (ALD) to fabricate a decent quality gate stack on GaAs.[40,41] This result was unexpected because of the *ex situ* fabrication of the oxide typically yielding a low-quality interface oxide. This was explained by a "self-cleaning effect" in which the native surface oxides are largely eliminated during the early stages of the ALD process.[42–45] Further investigations have been performed to use dielectrics prepared by ALD on various other III–V materials such as InGaAs,[46,47] InAs,[48] and InP.[49]

Today, the focus is on investigating the possibility of using ALD-deposited high-κ dielectric layers such as Al_2O_3 and HfO_2 and a bilayer of both in InGaAs-based MOSFETs. Interfacial defects, such as As-As dimers and also Ga and As dangling bonds, contribute to the interface state density, which deteriorate device performance.[50] Various approaches to optimizing and engineering the gate stack through pre-deposition cleaning treatments,[51,52] the use of interfacial layers,[53,54] modifications of the deposition chemistry,[55] post-deposition treatments,[51,56,57] and *in situ* ALD[58] are being investigated. For InGaAs, it has been observed that the MOSFET characteristics improved significantly with

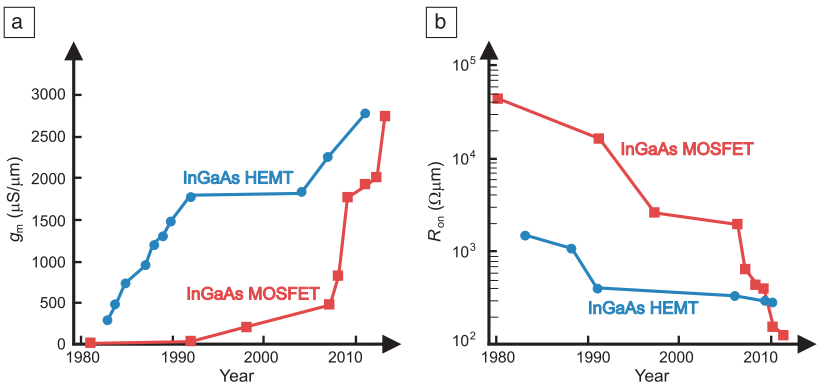


Figure 2. Performance comparison of inversion-type InGaAs metal oxide semiconductor field-effect transistors (MOSFETs) and high-electron-mobility transistors (HEMTs) (with $In_xGa_{1-x}As$ composition between $x = 0$ and 1) versus year: (a) transconductance g_m and (b) ON-resistance R_{on}. The transconductance of InGaAs MOSFETs has been significantly improved over the last years and is now on par with the highest values of HEMTs. Similarly, the R_{on} of InGaAs MOSFETs has been dramatically reduced, reaching values of even below the R_{on} of HEMTs. Reproduced with permission from Reference 23. © 2013 IEEE.

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increasing indium molar fraction.[40] Another approach using InP as a barrier layer, in what is known as a "buried-channel" design, has also yielded good MOSFET performance, but is limited in terms of EOT scalability.[59] A further challenge is to maintain the high electron mobility of InGaAs in MOS structures with scaled gate stacks because of Coulomb scattering, interface roughness scattering, and remote phonon scattering, which can severely degrade the mobility.[60,61]

Parasitic resistance

Another challenge to further improve MOSFET performance is posed by parasitic resistances. As shown in Figure 2b, a significant reduction in the ON-resistance, R_{on}, has already been demonstrated as compared to HEMTs; however, further progress is needed to achieve the parasitic resistance required for ultra-scaled III–V MOSFETs at the contact dimensions allowed for sub-10-nm CMOS nodes. Thus, it is crucial to achieve extremely small metal contact resistance in nanometer-scale contacts. Thanks to the Fermi level pinning location close to the conduction band edge of InGaAs, with an InAs composition of around 70%, very good contacts with small contact resistances have been demonstrated with a variety of metals (**Figure 3**a).[62–68] A contact-first approach, in which the first step in the fabrication process consists of Mo deposition, recently yielded contact resistances below 7 Ω.μm for long contacts (longer than 200 nm) and around 40 Ω.μm for contacts as short as 20 nm.[62] Silicide-like contacts based on Ni, Co, or Pd that is alloyed with InGaAs at relatively low temperatures are also being investigated.[69,70] Although very promising for device integration, this approach is currently yielding inferior contact resistance values.

In addition to the contact resistance, the design of the access region from the source to the channel is crucial for reducing the total parasitic resistance. In that regard, a self-aligned architecture is preferred, where ohmic contacts are very closely spaced from the gate and thus possess low resistance. Gate-first[71,72] as well as gate-last[25,73] III–V MOSFET process flows using precision etching or applying regrown and *in situ*-doped source/drain regions have been introduced that provide reduced access resistance and help improve the drive current and transconductance. Self-aligned InGaAs MOSFETs with gate lengths as short as 20 nm have been demonstrated (Figure 3b).[25]

Integration of III–V semiconductors on silicon

The best integration approach for III–V MOSFETs on Si is still not established and is one of the major challenges. A significant complication is that economic reasons dictate the use of Si as substrate material. A second problem is that a high-performance *p*-channel device, as required in CMOS, will have to be based on semiconductors with high hole mobility, such as Ge[14,74] or InGaSb.[75] Both have different relaxed lattice constants from InAs-rich InGaAs, which renders the combined integration on Si a very difficult technological problem. Several integration schemes are being pursued, such as direct wafer bonding,[76,77] epitaxial layer transfer to a silicon on insulator substrate,[78] and aspect ratio trapping (ART).[79] The first approach relies on the transfer of a thin III–V layer onto a thin dielectric on top of the Si wafer (**Figure 4**a). Instead, the ART process (Figure 4b) is based on the selective growth of lattice-mismatched material inside trenches with high aspect ratios. Threading dislocations are diverted to the sidewalls, and thus high-quality III–V layers at the top of the trench are possible. Efforts have been undertaken to build InGaAs MOSFETs based on this approach.[80]

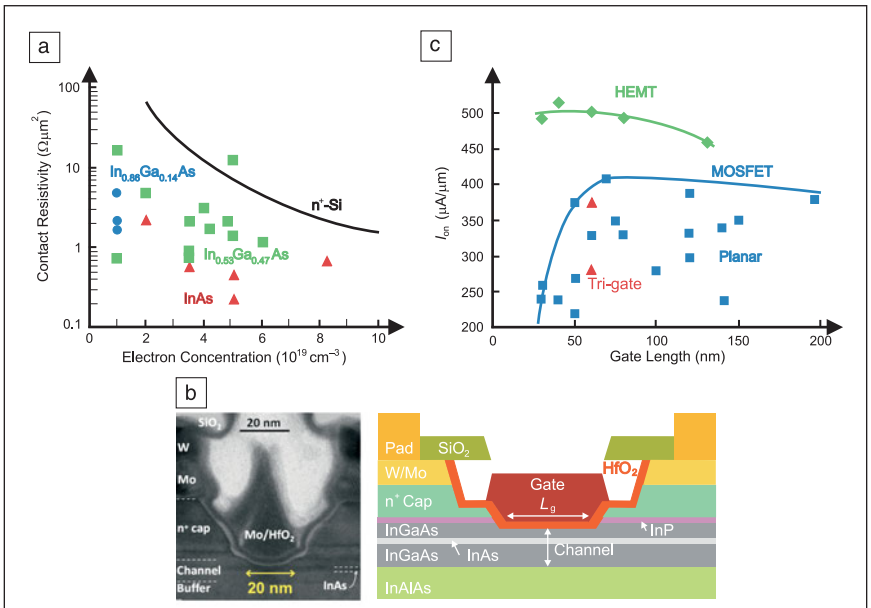


Figure 3. Planar III–V metal oxide semiconductor field-effect transistors (MOSFETs). (a) Contact resistivity of refractory metals on InGaAs versus electron concentration.[62–68] The different color codes for the various compositions of $In_xGa_{1-x}As$ range from $x = 0.53$ to $x = 1$ (pure InAs). For reference, typical contact resistivities of metals on n^+-Si are also shown. Contacts to n^+-InGaAs are as good as, if not better than, those of n^+-Si. Increasing the InAs composition results in better contact resistance. (b) Transmission electron micrograph cross-section and schematics of a 20-nm-gate-length gate-last self-aligned InGaAs MOSFET. The channel includes a thin core layer of InAs and two cladding layers of $In_{0.7}Ga_{0.3}As$. The MOS gate structure is in the middle of the figure and consists of Mo gate metal and HfO_2 as gate dielectric. The source and drain contacts are placed on both sides of the gate and self-aligned to it. They consist of a Mo/W bilayer on top of a recessed n^+-InGaAs cap. This is one of the smallest and most compact working InGaAs MOSFETs demonstrated.[25] (c) ON-current I_{on} for fixed OFF-current $I_{off} = 100$ nA/μm and source-drain voltage $V_{DS} = 0.5$ V, as a function of gate length, L_g for state-of-the-art InGaAs MOSFETs. The blue squares denote planar MOSFETs. The red triangles denote tri-gate MOSFETs. For reference, InGaAs high-electron-mobility transistors (HEMTs) are also shown (green diamonds). The green line is a trend line for HEMTs. The blue line represents the highest performance attained by MOSFETs of any kind. MOSFETs have yet to achieve the performance demonstrated by HEMTs. Also, planar MOSFETs seem to face a scaling limit of about 50 nm in gate length, beyond which the performance drastically drops. The data are taken from Reference 25 and references therein.

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While simple *n*- and *p*-channel FETs have been successfully integrated using some of these approaches,[76–78] high-performance transistor demonstrations using any of these techniques are still lacking.

An approach to completely avoid threading dislocations is to limit the extent of the Si/III–V cross-section in two dimensions. Thus, high-quality III–V materials directly on Si can be achieved by the epitaxial growth of NWs (typical diameter <100 nm) (Figure 4c).[81–84] If the diameter is made sufficiently small, dislocation formation can be completely avoided, as demonstrated in the Si/GaAsSb and Si/GaAs systems.[85,86] Among the common methods to form III–V NWs on Si is the vapor-liquid-solid (VLS) method, in which a nanoparticle is used to collect growth material and enhance the epitaxial growth rate underneath it.[87] The particle thus resides on top of the NW, while the NW grows upward, in most cases along the [111]B direction.[81,88]

NW selective-area epitaxy (NW-SAE) seems a more promising approach for III–V integration on Si because it avoids the use of a catalyst nanoparticle, and instead uses a patterned oxide mask to control the location of III–V growth.[81] The disadvantage of these techniques is that they rely on Si(111) substrates to grow NWs in that direction. Recently, a template-assisted growth technique has been introduced that overcomes various NW growth limitations (Figure 4d).[89] With this technique, epitaxial growth of III–V homo- and heterostructure NWs on various directions, including Si (100) and scaled NWs with a 25 nm diameter, have been demonstrated.[90] Although these wires have a very high potential for future III–V device integration on Si, the vertical device processing is more challenging.

From planar to 3D device structures

A substantial amount of basic InGaAs MOSFET technology has been developed in planar transistors, although mainly on III–V substrates. However, the footprint-scaling potential of this device architecture is limited. Structures offering greater scalability are FinFETs, Trigate MOSFETs, and GAA NW MOSFETs, as discussed previously (Figure 1). In addition, their reduced dimensions may also ease Si integration. For the same channel length, increasing the number of gates that modulate the electron concentration in the channel provides improved gate control and better SCE. Trigate MOSFETs

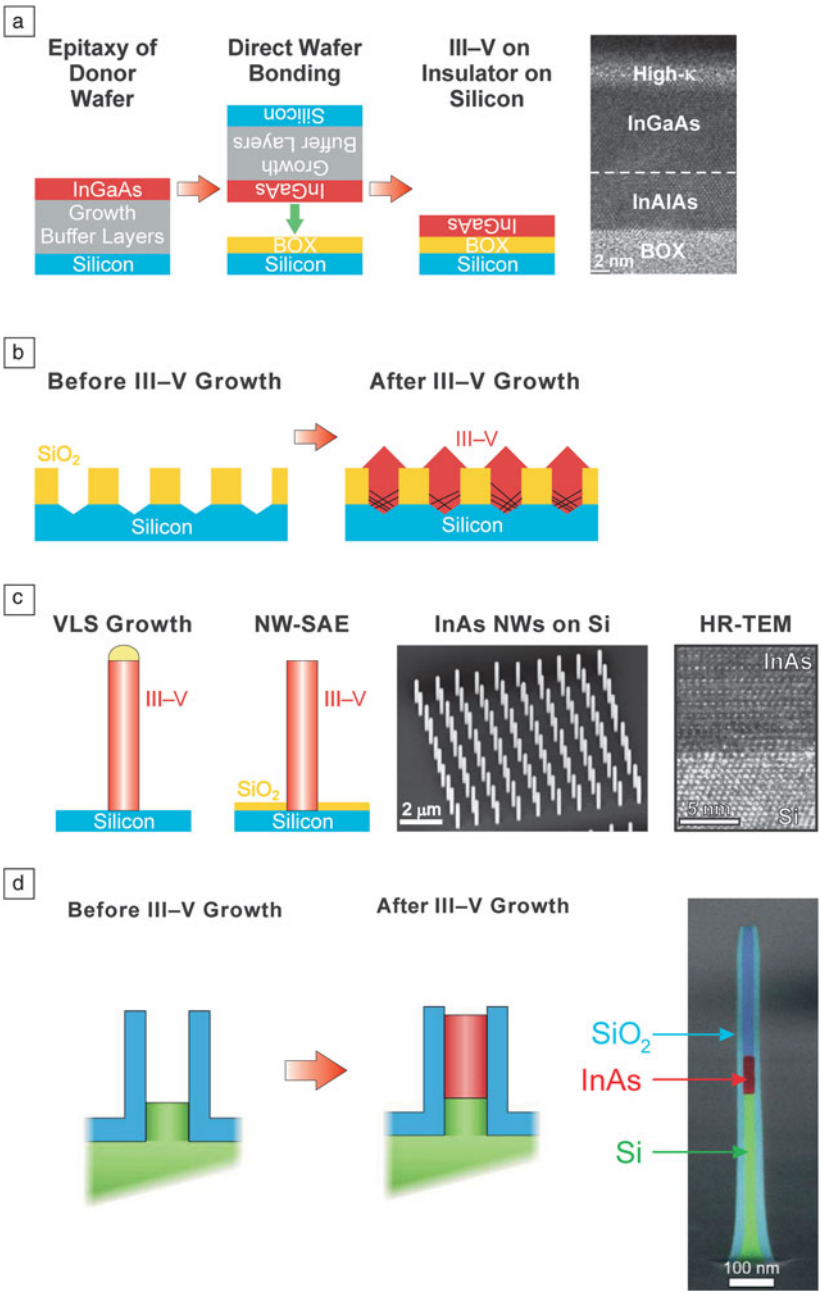


Figure 4. Integration of III–V semiconductors on silicon. (a) Process flow of the direct wafer bonding technique of thin III–V layers such as InGaAs on insulator on silicon. In this approach, heteroepitaxy using thick buffer layers is applied to achieve high-quality III–V layers on large Si substrates. The InGaAs layer is then transferred onto the target Si wafer by bonding to the buried oxide (BOX). In the next step, the bonding wafer is released and can be reused for growth. The high-resolution transmission electron micrograph (HR-TEM) shows a bonded InGaAs/InAlAs layer with ideal crystallinity on top of the BOX and covered with a thin high-κ gate dielectric material.[77] (b) Schematics of the aspect ratio trapping technique before and after III–V layer growth. In this approach, high aspect ratio SiO_2 trenches are fabricated on Si substrates. Threading dislocations and stacking faults caused by the growth of lattice mismatched III–V materials on Si are diverted to the sidewalls, resulting in high-quality III–V layers at the top of the trench. (c) Schematics of a grown III–V nanowire on Si with the vapor-liquid-solid (VLS) technique[87] and nanowire selective-area epitaxy (NW-SAE).[135] The scanning electron micrograph shows InAs grown via NW-SAE on Si, and the HR-TEM image shows the resulting high-quality Si/InAs heterointerface. (d) In the template-assisted growth technique, nanotube templates of oxide are fabricated on Si substrates and filled by selective epitaxy with III–V material.[89] With this technique, very thin nanowires can be grown.[90]

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with fins as narrow as 30 nm and excellent characteristics have been demonstrated.[91]

A summary of the state of the art of top-down fabricated InGaAs MOSFET technology for logic is presented in Figure 3c. This figure shows the ON-current that is obtained by fixing the OFF-current at 100 nA/μm and the operating voltage at 0.5 V.[9] This figure of merit balances the requirements for high current drive at low voltage and good SCEs. It is quite challenging for a device to meet all criteria and be included in this graph. First, the gate length must be below 200 nm. Then, the device must attain a subthreshold current as low as 100 nA/μm when turned off. The graph shows InGaAs MOSFETs of any kind that meet these criteria.[25,91–94] For reference, the graph also shows InGaAs HEMTs,[95] which currently still set the highest mark for performance. Among InGaAs MOSFETs, planar designs reach the highest performance,[25] thanks to aggressive scaling and their self-aligned designs with low parasitics. However, as seen in Figure 3c, their I_{on} drops significantly for short gate lengths, indicating that the scaling potential of this architecture is limited. Trigate and GAA NW MOSFETs are favored from a scalability point of view, but their development is less mature because the process technology, including gate stack and contacts, is even more challenging and not fully optimized yet.

III–V nanowire MOSFETs

NWs as a base material for III–V MOSFETs can be produced by top-down fabrication techniques or bottom-up growth processes in lateral or vertical fashion. The evolution of III–V MOSFETs will strive toward lateral NW devices in the form of Trigate and GAA structures. They are easier to fabricate than vertical transistors, as has been demonstrated for both etched structures and selectively grown NWs. Vertical NW-FETs as shown in **Figure 5**a, on the other hand, may be easier to integrate on Si because the reduced dimensions enable direct growth of III–V NWs on Si. Furthermore, the vertical transistor structure uncouples the gate length and footprint scaling. As a result, device density goals may be reached at longer gate lengths with contacts extending into the third dimension to reduce resistance, thus resulting in far better SCEs and performance than with lateral devices. However, both accurate control of the vertical layer stack and further processing development will be required, including self-aligned gate technologies. High-κ integration on NWs is much less studied than on planar devices,[96,97] and the low capacitance levels combined with the co-existence of various crystal planes and curved surfaces complicate the measurements and the data analysis.

Figure 5b summarizes the status in the field of III–V NW MOSFETs regarding both etched and selectively grown structures processed in either the lateral or vertical direction.[92,98–105] Devices with competitive performance have already been realized successfully. Reduction of the access resistance via regrowth, implantation, or epitaxial technologies has been critical to increase the performance in both the ON-state (transconductance) and the OFF-state (subthreshold characteristics). Diameter reduction is essential for increasing the performance, although the resistance must be kept under control. Finally, the gate length-reduction achieved has also helped increase the performance.[106]

Although vertical device fabrication may be regarded as more challenging than lateral device fabrication, important progress has been made and vertical III–V NW-FETs based on single or arrays of NWs fabricated by either epitaxial or etching techniques have been demonstrated (square symbols in Figure 5b). Moreover, a modulation-doped GAA InGaAs NW-FET integrated on a Si substrate with excellent device properties[103] as well as vertical GAA InAs NW-FETs into which a thin InAs buffer layer had been introduced to reduce the access resistance toward the substrate[107] were recently demonstrated. Competitive radio frequency (RF) performance has been achieved,[108] and the first RF circuits in the form of single-balanced down-conversion mixers operating up to 5 GHz were constructed.[109]

III–V nanowire tunnel FETs

New materials in combination with the 3D architecture are key to achieving optimum MOSFET performance with close to 60 mV/decade subthreshold swing at highly scaled gate lengths, as discussed previously. However, to go below the

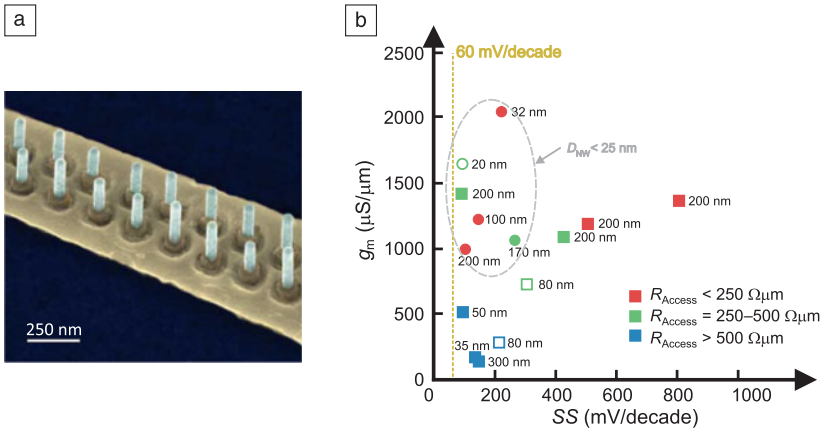


Figure 5. III–V nanowire metal oxide semiconductor field-effect transistors (MOSFETs). (a) Scanning electron micrograph of an array of III–V nanowires (NWs) with wrap-gate formed. (b) Comparison of the transconductance g_m versus subthreshold swing *SS* of published NW MOSFETs at source-drain voltage V_{DS} = 0.5 V.[92,98–105] The MOSFET gate length is given next to the data point. Squares and circles represent vertical and lateral NW devices, respectively. Open and filled symbols depict devices where the NW was fabricated by etching and growth, respectively, and the color code indicates the range of the NW MOSFET access resistance R_{Access}. Achieving a high transconductance requires low access resistance R_{Access}. The data points within the gray dashed ellipse have an active NW diameter, D_{NW}, of below 25 nm. They show the best performance concerning high transconductance g_m and small subthreshold swing *SS*.

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60 mV/decade limit, new device mechanisms must be used. The TFET, which offers a steep slope (SS < 60 mV/decade) (i.e., it can deliver the required I_{on}/I_{off} at lower supply voltage) will always be more energy efficient in that regime.[19] TFETs generally comprise a gated *p-i-n* structure, as shown schematically in **Figure 6**a where *i* represents intrinsic. In the ON-state, the charge carriers are injected by BTBT from the source into the channel (see the energy band diagram in Figure 6b), enabling a steep OFF-ON transition of the transfer characteristics.[110]

A major challenge of current TFET optimization is to achieve the highest possible I_{on}, the lowest SS over many orders of magnitude in the drain current, and the lowest possible I_{off}.[19,20] One prerequisite to achieve optimum TFET performance is a low effective energy barrier for BTBT and a small effective mass, m^*, of the charge carrier. Therefore, heterostructures based on Si/III–V or all-III–V materials are very attractive because their effective bandgap can be engineered from staggered to broken (i.e., the upper band-edge of the valence band of one material is located at the same energy or above the energy of the lower band-edge of the conduction band of the other material), and thus the TFET performance can be significantly enhanced compared to homojunctions.[111–116] This has been experimentally demonstrated with all-III–V heterojunction TFETs based on materials such as InGaAs with different compositions,[117] InGaAs/InP,[118] and In(Ga)As/Ga(As)Sb.[119] Especially with the arsenide/antimonide material system, which enables a broken-gap heterostructure, the ON-currents of TFETs have been boosted significantly,[120–122] see Figure 6c. So far, however, the corresponding I_{on}/I_{off} ratio of the all-III–V heterojunctions is too low to be competitive. In contrast, the InAs-Si heterojunction system[123–125] achieves very high I_{on}/I_{off} ratios of more than 10^6 and also seems promising in terms of high I_{on} because of the record high tunnel currents achieved in Si/InAs tunnel diodes.[126] The Si-InAs heterojunction TFETs are based on a vertical GAA NW architecture achieved by growing InAs NWs on top of a Si substrate (see Figure 6a). So far, they are the only TFETs exploiting III–V materials integrated on Si. Although recently significant improvements in TFET performance have been achieved, and even TFETs with SS < 60 mV/decade have been demonstrated,[117] further breakthroughs are needed to achieve all target parameters (I_{on}, I_{off} and SS) in one device.

As discussed, optimization of the gate stack for small EOT and D_{it} and reduction of parasitic resistances are also necessary for TFETs, similar to III–V MOSFETs. TFET optimization, however, is even more challenging, as the performance depends also on the heterojunction abruptness, the source-channel doping profile, and defects at the interface and within the material that can significantly deteriorate the performance because of trap-assisted tunneling.

Summary and conclusions

For more than 40 years, Si technology primarily relied on miniaturization to increase performance. However, this approach has now reached its limits, and innovations based on

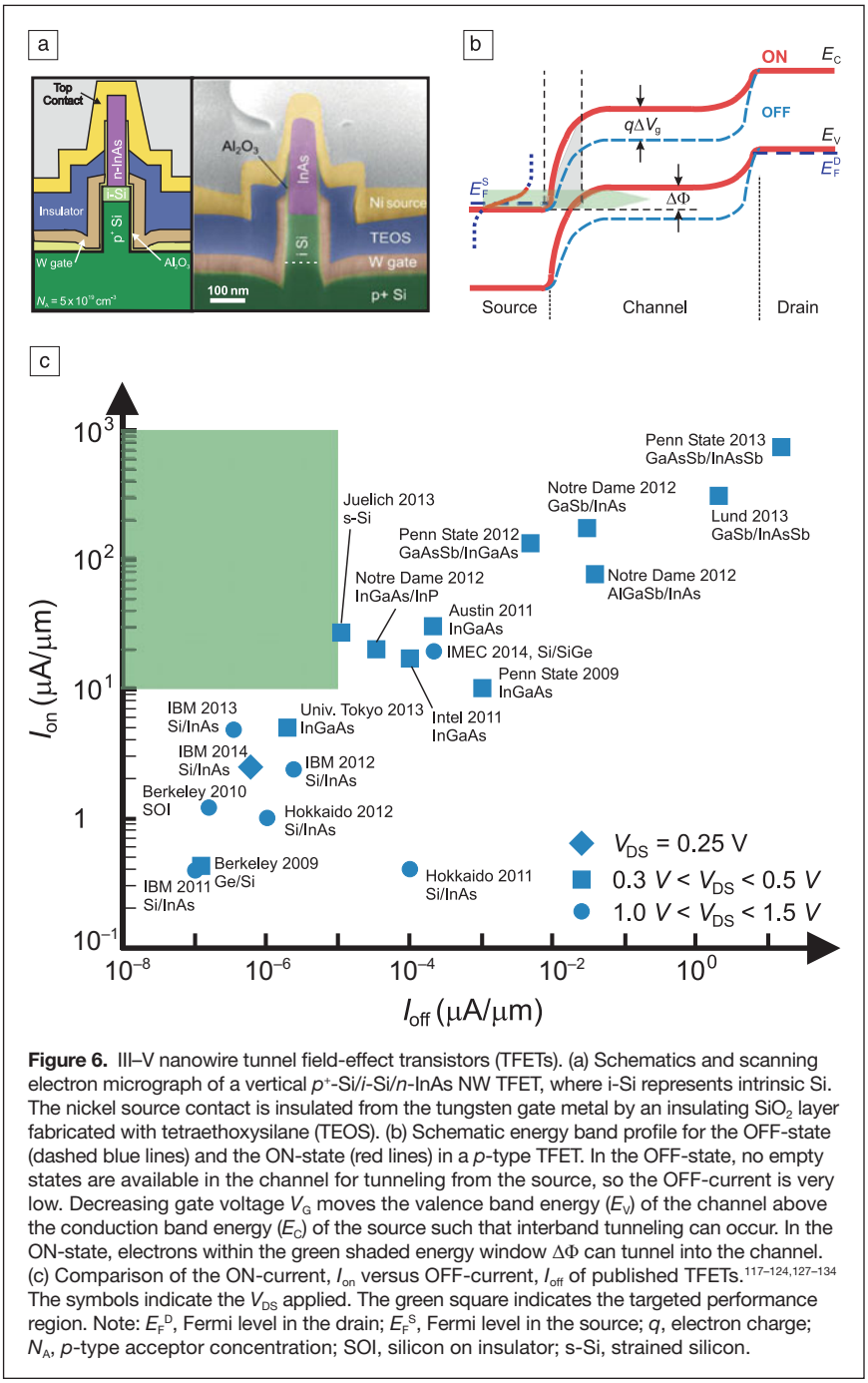


Figure 6. III–V nanowire tunnel field-effect transistors (TFETs). (a) Schematics and scanning electron micrograph of a vertical p^+-Si/*i*-Si/*n*-InAs NW TFET, where i-Si represents intrinsic Si. The nickel source contact is insulated from the tungsten gate metal by an insulating SiO_2 layer fabricated with tetraethoxysilane (TEOS). (b) Schematic energy band profile for the OFF-state (dashed blue lines) and the ON-state (red lines) in a *p*-type TFET. In the OFF-state, no empty states are available in the channel for tunneling from the source, so the OFF-current is very low. Decreasing gate voltage V_G moves the valence band energy (E_V) of the channel above the conduction band energy (E_C) of the source such that interband tunneling can occur. In the ON-state, electrons within the green shaded energy window $\Delta\Phi$ can tunnel into the channel. (c) Comparison of the ON-current, I_{on} versus OFF-current, I_{off} of published TFETs.[117–124,127–134] The symbols indicate the V_{DS} applied. The green square indicates the targeted performance region. Note: E_F^D, Fermi level in the drain; E_F^S, Fermi level in the source; q, electron charge; N_A, *p*-type acceptor concentration; SOI, silicon on insulator; s-Si, strained silicon.

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new materials, device architectures, and physical mechanisms are required to drive the roadmap further and to facilitate performance increases, including reductions in power dissipation, by lowering the supply voltage. Remarkable progress has been made to overcome the extremely demanding problems of introducing III–V semiconductors, such as InGaAs, as high-mobility channel materials into metal oxide semiconductor field-effect transistors (MOSFETs). Essential for the ultimate success, however, will be III–V MOSFETs delivering substantially better performance than Si at future gate lengths below 10 nm with cost-effective manufacturing and required reliability. Thereby integration on silicon is a must. The current less mature GAA III–V nanowire (NW) device architecture offers significant advantages over planar structures. For further progress, improvements of the electrostatic gate coupling as well as the possibility to integrate high-quality III–V NWs directly on Si need to be exploited further. Of particular interest is the possibility to implement vertical device structures to decouple the device density and gate-length scaling. Finally, the potential to engineer the electronic properties by using III–V heterostructures is key for tunnel FETs. They represent the most promising steep-slope switch candidate, having the potential to reduce the supply voltage to offer significant power dissipation savings. Thus, the application of III–V compound materials and structures, especially NWs, is opening up new avenues to increase and improve device performance.

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