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A thermally enhanced evanescent-mode dual-ridged waveguide antenna array for millimeter-wave applications

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Research Paper

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Abstract

In this paper, we present an evanescent-mode dual-ridged waveguide antenna array designed for high-performance millimeter-wave wireless communications. The proposed antenna array addresses critical thermal management issues commonly encountered in active antenna array technologies operating at millimeter-wave frequencies, without compromising electromagnetic performance relative to more conventional alternative technologies. This improvement can be attributed to the metallic construction of the array. Experimental results demonstrate that the proposed array achieves a thermal resistance of only 11.11 K/W, representing more than an order-of-magnitude improvement compared to an equivalent patch antenna array, which exhibits a thermal resistance of 123.3 K/W. Additionally, the antenna array enables wide-angle beam-scanning capabilities, achieving a field of view of 116° along the H-plane and 96° along the E-plane. The characteristics of the proposed design are rigorously validated through experimental measurements performed on an 8 × 8 array prototype.

Introduction

The ever-increasing demand for radio links featuring higher throughput and capacity is driving continuous improvements to existing cellular communication standards. The next generation of wireless networks aims to deliver data rates many times higher than current systems by employing increasingly complex radio-frequency (RF) technologies [1, 2]. Achieving these goals, however, requires access to substantially broader bandwidth, which cannot be accommodated in the frequency ranges currently in use. As a result, a trend has emerged toward utilizing the millimeter-wave (mmWave) spectrum for the next generation of cellular communication systems [3]. Despite the access to broader bandwidths, mmWave communication faces significant challenges. For example, propagation losses are much higher at mmWave frequencies due to an increase in the free-space path loss and the atmospheric absorption. Furthermore, signals at these frequencies are also more susceptible to blockage [4]. These additional losses must be mitigated or compensated to ensure reliable and robust communication links.

Active antenna arrays are expected to play an essential role in mmWave communication systems, because they can provide the high antenna gains needed to overcome the increased propagation losses [5–7]. By employing a large number of antenna elements, such arrays can achieve highly directive radiation patterns that can be electronically steered by implementing a suitable amplitude tapering profile and phase shifts at the array element level. This is crucial for overcoming the limited coverage area inherent to high-gain, narrow beams. However, the implementation of large mmWave antenna arrays introduces new challenges. Electrically steerable arrays require packaged beamforming integrated circuits (BFICs) containing a large number of active components, which, at mmWave frequencies, operate with relatively low efficiency. Furthermore, to suppress grating lobes in the array radiation pattern, the antenna elements must be spaced very closely together (typically less than half a wavelength apart). While the short wavelength of mmWave signals enables compact arrays, it also necessitates extremely dense integration of the active array electronics. This can cause the operating temperature to rise to intolerable levels [8, 9]. For example, one study showed that the temperature in a 128-element array can reach up to 300°C when using a standard long-term evolution power amplifier [10]. Such high operating temperatures are predicted to become one of the major bottlenecks for mmWave communication systems [8]. One approach to controlling the temperature in mmWave antenna arrays is to use antenna elements that can conduct heat, thereby helping to dissipate heat from the system. This approach allows the system to maintain a given operating

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temperature with less stringent requirements on the efficiency of the electronics and the heat sink, while still ensuring stable operation.

The use of antennas with enhanced thermal characteristics has received limited attention in the available scientific literature [11–14]. In [11], a heatsink-integrated antenna array was developed, achieving a reduction of 60°C in operating temperature. However, the design exhibited significant manufacturing challenges. Similarly, in [12], fin-shaped heat sink structures were integrated into a substrate-integrated waveguide slot antenna array operating at 28 GHz. This solution demonstrated a 57% reduction in operating temperature compared to a similar design without fins, while also improving electromagnetic performance. In [13], a dielectric resonator antenna covering the 26.5–29.5 GHz band was proposed, where structural perforations were introduced to facilitate airflow and enhance thermal dissipation along the array. More recently, in [15], a beam-switching heatsink antenna array operating at 26 GHz was proposed, employing complementary split-ring resonator embedded isolation walls that simultaneously serve as thermal fins and electromagnetic barriers, achieving a temperature reduction of approximately 40°C compared to conventional antennas. Although this class of heatsink antennas provides notable temperature reduction benefits, the resulting designs are typically complex to manufacture and may be limited in beam-scanning capability.

A more general approach to improving thermal performance involves the adoption of metal-based antennas, as metallic alloys possess thermal conductivities that are typically an order of magnitude higher than those of dielectric materials. One promising candidate for such implementations is the open-ended waveguide antenna technology. However, standard air-filled rectangular waveguides must exceed half a wavelength in size to support electromagnetic wave propagation. Due to their cutoff frequency, this makes them incompatible with the tight element spacing required to suppress grating lobes in antenna arrays. This limitation can be addressed by introducing ridges along the waveguide walls, which effectively lower the cutoff frequency of the fundamental mode and enable a more compact geometry [16].

In this paper, we introduce an evanescent-mode dual-ridged waveguide antenna (EDA) array featuring a fully metallic, layered architecture, building upon and extending the previous work detailed in [17]. An earlier version of this paper was presented at EuMW 2025 and was published in its Proceedings [1]. While the original study in [17] presented this antenna design as a quad-ridge configuration, its analysis was restricted primarily to unit-cell simulations and measurements conducted on a single, isolated element. Although these initial evaluations provide useful preliminary insights into the antenna radiation patterns and scanning capabilities, finite-array characterizations are essential for accurate assessment, as the performance of an embedded antenna element is inherently influenced by its surrounding array environment. In the current work, we expand the analysis by including extensive finite-array simulations, supplemented by thorough measurements. Additionally, we have integrated a launcher structure on a printed circuit board (PCB) within the EDA design, greatly simplifying its integration with active beamformer circuits and enhancing system-level performance. The construction methodology has been further refined by segmenting the EDA into discrete metallic layers, enabling more conventional, accurate, and cost-effective manufacturing techniques. Although the presented implementation focuses on single polarization, the proposed design inherently supports extension to dual polarization. Due to its all-metallic construction, the antenna structure achieves significantly enhanced thermal dissipation performance, a key advantage verified through detailed simulations and empirical verifications. This characteristic allows for lower operating temperatures even in densely integrated array scenarios. Simultaneously, the antenna demonstrates robust wide-angle beam-scanning capabilities, positioning it as an effective candidate for advanced high-performance mmWave systems in next-generation wireless communications and remote sensing applications.

The remainder of this paper is organized as follows. The second section describes the design of the proposed antenna element and its launcher network. The third section presents simulation and measurement results obtained from an 8×8 array prototype. In the fourth section, the thermal characteristics of the proposed radiating structure are benchmarked against those of an equivalent patch antenna. Finally, conclusions are drawn in the fifth section.

EDA antenna

Antenna element

In this section, the design of the proposed EDA element is introduced, and its electromagnetic performance characteristics are evaluated. Subsequently, the proposed launcher structure designed to excite and feed the antenna will be described. Previous studies, such as [17], have demonstrated the feasibility of quad-ridged evanescent-mode waveguide antennas for array applications. However, these earlier investigations were limited to unit-cell analyses and measurements of a single radiating element, and did not explore the antenna performance in array configuration and in combination with a suitable launcher necessary for integration with active electronics.

Figure 1 illustrates the proposed EDA geometry. Unlike traditional waveguide antennas, which typically open gradually to facilitate the transition from guided waves to a radiated field in free space, the proposed antenna employs alternating ridged and non-ridged square waveguide sections. Proper EDA operation requires the ridged sections to function above their cutoff frequency while the non-ridged sections remain below their cutoff frequency, ensuring evanescent-mode propagation in the latter. Figure 1(c) provides an equivalent circuit model for one period of the EDA, with ridged sections modeled as shunt resonators and non-ridged evanescent sections represented as reactive impedance inverters [18, 19]. The cutoff conditions that define these two operating regimes are quantified below for the specific dimensions of the proposed design.

The non-ridged sections of the EDA consist of square waveguide segments with lateral dimension $W_{\mathrm{WG}} = 4.34$ mm (Table 1). The cutoff frequency of the dominant TE_{10} mode in an air-filled square waveguide is [16]:

$$f_c = \frac{c}{2W_{\mathrm{WG}}}, \tag{1}$$

where c is the speed of light in vacuum. Substituting $W_{\mathrm{WG}} = 4.34$ mm yields $f_c \simeq 34.6$ GHz, which is well above the 28 GHz operating frequency. Consequently, the electromagnetic fields in these sections decay exponentially along the waveguide axis with an attenuation constant [16]:

$$\alpha = \frac{2\pi}{c}\sqrt{f_c^2 - f^2}, \tag{2}$$

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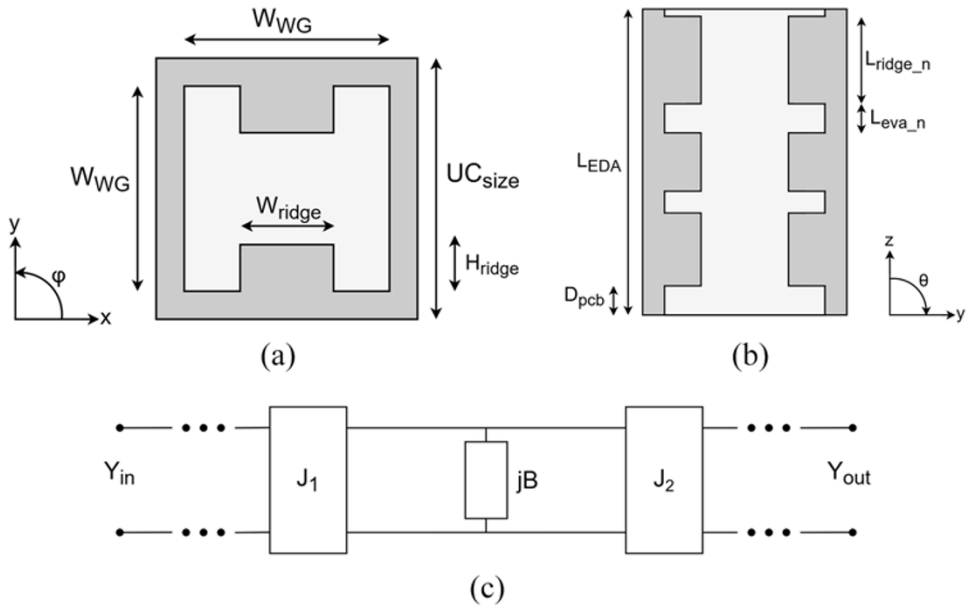


Figure 1. (a) Top view of the EDA, (b) cross-sectional view of the EDA, and (c) circuit representation of the EDA.

Table 1. Final design parameters of the EDA antenna element expressed in mm

Parameter	Value	Parameter	Value	Parameter	Value
UC_{size}	5.34	L_{eva_1}	1.34	L_{ridge_3}	3.14
W_{WG}	4.34	L_{eva_2}	2.51	L_{EDA}	16.4
W_{ridge}	1.33	L_{eva_3}	0.3	d_{patch}	2.54
H_{ridge}	1.08	L_{ridge_1}	3.36	via_{offset}	0.905
D_{pcb}	0.88	L_{ridge_2}	4.96	r_{via}	0.1

which evaluates to $\alpha \simeq 424$ Np/m (3.7 dB/mm) at 28 GHz. The evanescent sections in Table 1 produce attenuations ranging from approximately 1 dB ($L_{\text{eva_3}}$) to 9 dB ($L_{\text{eva_2}}$), corresponding to the different inter-resonator coupling levels required by the band-pass filter synthesis. It is important to emphasize that this evanescent behavior is governed solely by the relationship $f_c > f$ and does not require the section length to satisfy any quarter-wavelength resonance condition. The quarter-wavelength constraint applies to impedance inverters realized by propagating-mode waveguide sections, which represents a fundamentally different topology. In the presented design, the coupling strength between adjacent resonators is controlled by the product αL_{eva}, in accordance with classical evanescent-mode filter theory [19].

In the ridged sections, opposing metallic ridges along the E-plane walls produce a capacitive loading that substantially lowers the cutoff frequency [16, 20]. To quantify this effect, we apply the transverse resonance method to the half cross-section at cutoff (Figure 5), exploiting the TE_{10} symmetry ($\partial E_y/\partial x = 0$ at the waveguide center). The half-structure comprises a gap region (height $h_{\text{gap}} = W_{\text{WG}} - 2H_{\text{ridge}}$, length $W_{\text{ridge}}/2$, open-circuited at the symmetry plane) and a full-height region (height W_{WG}, length $(W_{\text{WG}} - W_{\text{ridge}})/2$, short-circuited at the PEC sidewall). Each region acts as a parallel-plate transmission line with characteristic admittance $Y_0 = h/\eta_0$ ($\eta_0 \simeq 377\,\Omega$). The cutoff wavenumber

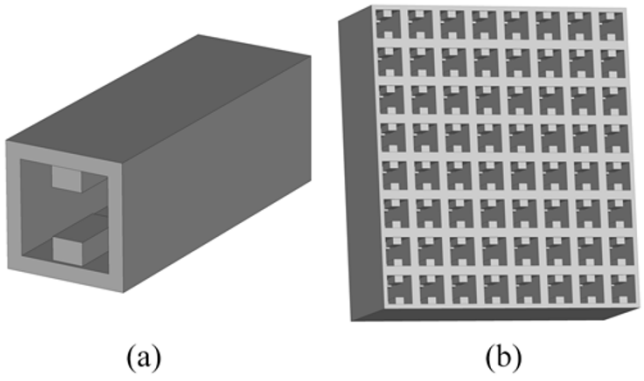


Figure 2. Three-dimensional view of (a) the unit cell simulation model and (b) the complete 8×8 antenna array simulation model.

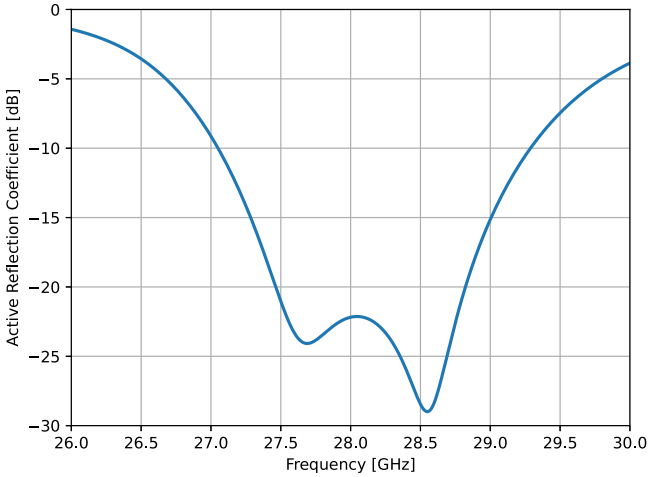


Figure 3. Simulated ARC obtained through unit-cell simulation.

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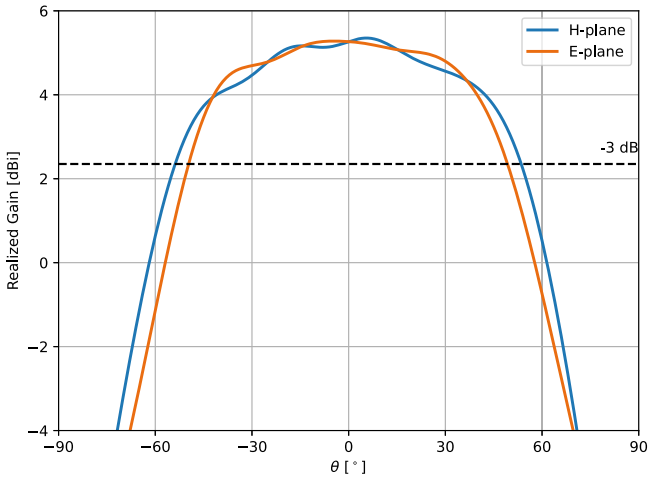


Figure 4. Simulated embedded radiation pattern of the EDA along the E- and H-planes at 28 GHz obtained through simulation of a central element in an 8×8 array. The boresight gain is 5.35 dBi.

$k_c = 2\pi f_{c,\text{ridged}}/c$ is the transverse propagation constant. The input admittances at the step are:

$$Y_{\text{gap}}(k_c) = \frac{jh_{\text{gap}}}{\eta_0} \tan\left(k_c \frac{W_{\text{ridge}}}{2}\right), \tag{3}$$

$$Y_{\text{full}}(k_c) = \frac{-jW_{\text{WG}}}{\eta_0} \cot\left(k_c \frac{W_{\text{WG}} - W_{\text{ridge}}}{2}\right). \tag{4}$$

At the step, the abrupt change in plate separation generates fringing fields that store excess reactive energy, represented by a single shunt susceptance jB_d in the equivalent circuit (Figure 5). For a single E-plane step (one corner), the quasi-static result from Marcuvitz [21] gives a normalized susceptance proportional to $\ln[\csc(\pi h_{\text{gap}}/(2W_{\text{WG}}))]$. In the dual-ridged geometry, the step involves two symmetric corners (one at each ridge tip), each contributing an equal fringing susceptance. Summing both contributions yields:

$$B_d(k_c) \simeq \frac{4W_{\text{WG}}^2 k_c}{\pi\eta_0} \ln\left[\csc\left(\frac{\pi h_{\text{gap}}}{2W_{\text{WG}}}\right)\right]. \tag{5}$$

Equation (5) captures the physical mechanism: reducing h_{gap} (i.e., deepening the ridges) increases B_d because $\ln[\csc(\cdot)]$ grows as the gap narrows, thereby shifting the resonance to a lower k_c and hence a lower cutoff frequency. The transverse resonance condition requires the total admittance at the step to vanish [16, 20]:

$$Y_{\text{gap}}(k_c) + Y_{\text{full}}(k_c) + jB_d(k_c) = 0. \tag{6}$$

Substituting (3)–(5) and solving numerically for the dimensions in Table 1 ($W_{\text{ridge}} = 1.33$ mm, $H_{\text{ridge}} = 1.08$ mm, $h_{\text{gap}} = 2.18$ mm) yields $k_c \simeq 490$ rad/m, corresponding to a ridged-section cutoff of approximately 23.4 GHz. This value is well below the 28 GHz operating frequency, confirming that the ridged sections support propagating modes throughout the operating band. It should be noted that (5) is a quasi-static result derived for infinite parallel plates and does not capture all higher-order effects present in the finite square cross-section.

The combination of propagating ridged sections ($f_{c,\text{ridged}} \ll 28$ GHz) and evanescent non-ridged sections ($f_c \simeq 34.6$ GHz > 28 GHz) constitutes the hallmark of the evanescent-mode waveguide topology [17–19]. In this architecture, the structure alternates

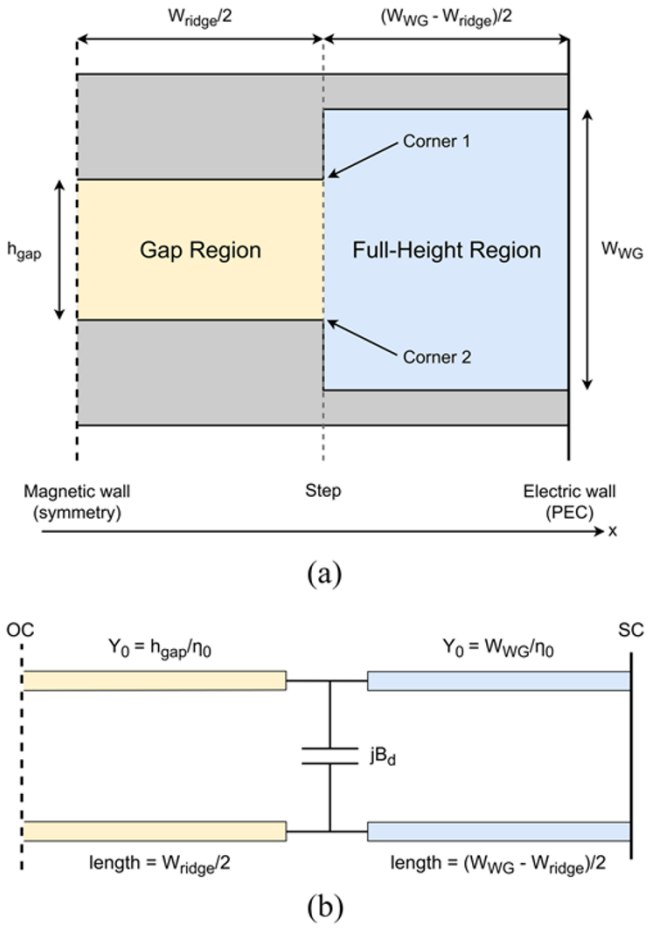


Figure 5. Transverse resonance schematic for the ridged waveguide at cutoff. (a) Half cross-section obtained by exploiting TE_{10} symmetry. The outer metal walls are continuous and flush across both regions; the ridges protrude inward in the gap region only. Two step corners (at the ridge tips) generate the fringing susceptance B_d. (b) Equivalent transmission line circuit with a single shunt capacitor representing the total susceptance jB_d at the step junction.

abruptly between propagation and evanescence, with each ridged section forming a resonant cavity and each evanescent section acting as a reactive impedance inverter. This differs fundamentally from a stepped-ridge configuration, where all sections support propagating modes and the ridge geometry is varied progressively to achieve a broadband impedance taper. In the EDA, no gradual taper exists; instead, the filtering behavior of the evanescent-mode structure defines both the operating bandwidth and the radiation characteristics. The equivalent circuit of Figure 1(c) captures this: each ridged section is modeled as a shunt resonator with frequency-dependent susceptance $B_k(\omega)$, while each evanescent section is represented by an impedance inverter with coupling value J_k, following the classical filter synthesis framework of [19].

Multiple design approaches for evanescent-mode filters are described in the scientific literature that can be used to design the EDA [18, 22]. These methodologies aim to determine optimal lengths for ridged and evanescent sections. Common design techniques include systematic optimization based on full-wave electromagnetic simulations and slope-parameter-based methods. In this work, a slope-parameter design approach [18] is utilized to obtain initial design values for the EDA. This step was followed by optimization through full-wave electromagnetic simulations to

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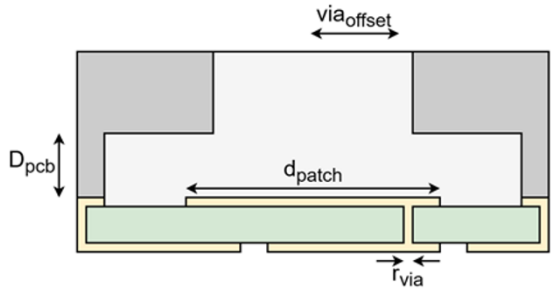


Figure 6. Cross-sectional view of the proposed launcher structure for the individual EDA element.

obtain the final design values. This slope parameter method was implemented as follows.

The first step involves calculating the inverter values J_k as:

$$J_k = \sqrt{\frac{b_k \Delta b_{k+1}}{g_k g_{k+1}}}, \tag{7}$$

where Δ is the fractional bandwidth, b_k represents slope parameters of resonator sections, and g_k are coefficients defining the desired band-pass response. Boundary parameters b_0 and b_n are defined as Y_{in} and Y_{out}, respectively. Intermediate slope parameters are obtained via:

$$b_k = \Delta \frac{\omega_0}{2} \frac{dB_k(\omega)}{d\omega}\bigg|_{\omega=\omega_0}, \tag{8}$$

where $B_k(\omega)$ is the frequency-dependent susceptance of the k-th resonator, and ω_0 denotes the angular center frequency. These calculated values provide an initial EDA design, which can subsequently be optimized through full-wave simulations.

To evaluate the suitability of the EDA for active array applications, particularly those requiring beam steering, preliminary electromagnetic simulations were performed using CST Studio Suite [23]. Figure 2 depicts the unit-cell model configuration as well as the 8 × 8 array configuration used for the upcoming performance analyses. The active reflection coefficient (ARC), which accounts for mutual coupling effects, is an essential parameter for assessing array antenna performance.

Figures 3 and 4 show the simulated ARC obtained from a unit-cell simulation and the embedded radiation pattern, respectively. It is important to note that, for this analysis, the reference impedance is the characteristic impedance of the waveguide structure rather than the conventional 50 Ω. The simulated results indicate a well-matched performance around 28 GHz, achieving a bandwidth of 7.9%. While the bandwidth is limited, it can be further increased by adding additional ridged and evanescent sections, at the cost of increased complexity and size. The radiation pattern of the embedded antenna element also exhibits a broad beamwidth, which is suitable for wide-scanning array applications, with a peak gain (boresight) of 5.35 dBi. This performance is achieved while maintaining an element spacing of less than 0.5λ, which ensures that grating lobes will not appear even when scanning to larger elevation angles. With these results and constraints in mind, the next step is to incorporate the launcher structure to be able to feed the EDA.

Launcher structure

To integrate the EDA with active arrays, a launcher structure is essential. The launcher must excite the desired waveguide mode and provide impedance transformation from the characteristic impedance of the waveguiding section to the standard 50 Ω reference impedance adopted at circuit level. Figure 6 illustrates the cross-sectional view of the proposed launcher, inspired by the design presented in [24]. This launcher consists of a circular, via-fed patch antenna mounted on a single dielectric layer (Rogers RO4350B).

The choice of a PCB-based launcher was driven by two main considerations. Firstly, the PCB integration simplifies interfacing the antenna array directly with the electronics necessary for active operation. Secondly, the selected launcher design can be straightforwardly extended to support dual polarization by introducing an additional orthogonally positioned feeding via and corresponding ridge modifications in the EDA.

The combined performance of the EDA and launcher was investigated through unit-cell simulations, and the final design parameters can be found in Table 1. Figure 7(a) and (b) illustrates the ARC for different scanning angles along the H- and E-planes, respectively. Compared to the standalone EDA, integration with the launcher structure reduces impedance bandwidth from 7.9% to 4.2%, primarily due to the limited bandwidth of the patch antenna. Although bandwidth can be improved by incorporating stacked or parasitic patches, such enhancements fall outside the scope of this study. Nevertheless, the magnitude of the ARC remains below −10 dB for scanning angles up to approximately 50° in both planes.

Figure 8 presents the simulated ERP of the central element within an 8 × 8 array, including the launcher structure. The launcher-integrated EDA exhibits an half-power beamwidth (HPBW) of 115.2° along the H-plane and 103.6° along the E-plane, thus confirming the suitability of the proposed design for wide-angle scanning array applications. The boresight gain with the launcher is about 0.8 dB lower than without the launcher, which can be attributed to a wider beamwidth as well as losses introduced by the launcher structure.

8 × 8 EDA array design

In the previous section, the EDA performance was evaluated through unit-cell simulations, highlighting its key electromagnetic characteristics. In this section, we extend the evaluation to a complete 8 × 8 EDA array prototype through comprehensive full-wave simulations and experimental measurements. The prototype comprises two primary components: a metallic EDA structure and a PCB featuring the integrated launcher structure. An exploded view of the array assembly is presented in Figure 12.

The EDA array demonstrator was fabricated using aluminum via computer numerical control (CNC) machining. Two main adjustments were necessary to facilitate this manufacturing approach. Firstly, inner corners within the EDA structure were rounded with a radius of 0.25 mm to account for the finite radius of the CNC milling tip. This rounding slightly reduces the effective cross-sectional dimensions of the waveguide, resulting in a minor increase in its cutoff frequency. To compensate for this effect, the height of the ridges was marginally increased. Secondly, due to alternating ridged and non-ridged waveguide sections, realizing the entire 8 × 8 array from a single aluminum block is impractical. Consequently, the array was subdivided longitudinally into multiple layers. Each layer was individually fabricated and subsequently

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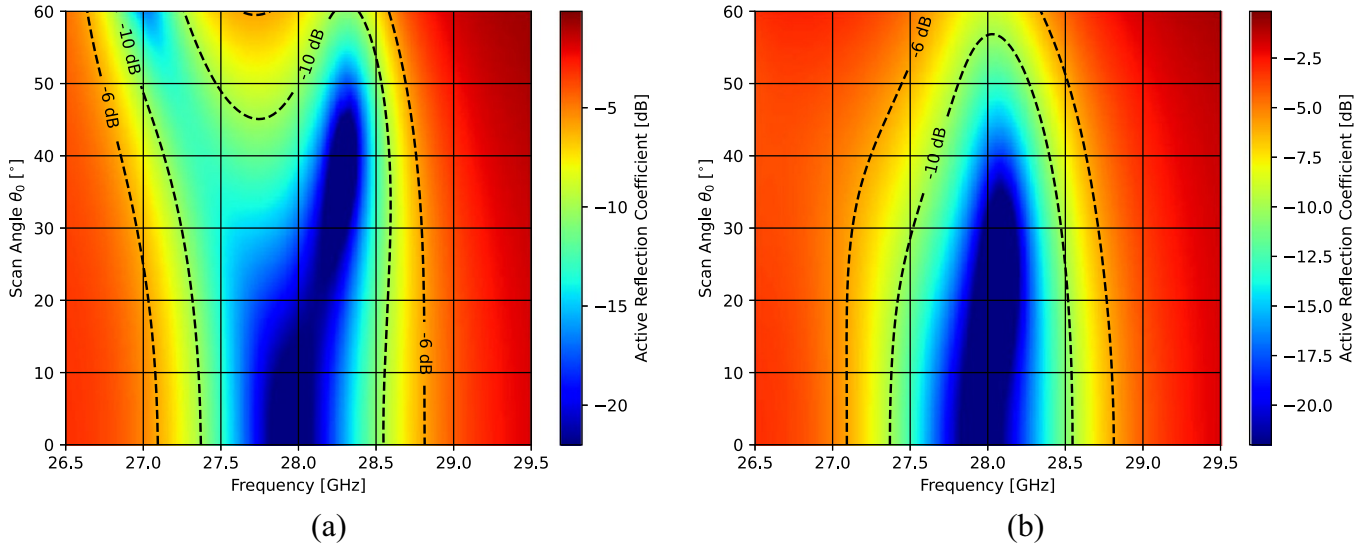


Figure 7. Simulated ARC of the EDA fed by the launcher structure for various scanning angles along (a) the H-plane and (b) the E-plane.

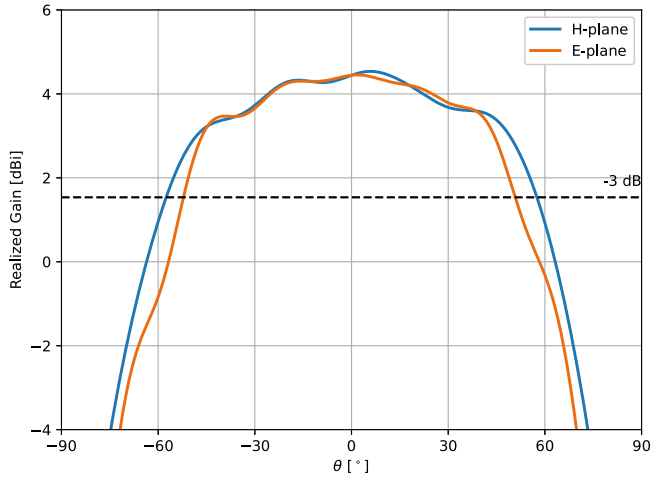


Figure 8. Simulated embedded radiation pattern of the EDA with the launcher structure along the E- and H-planes at 28 GHz obtained through simulation of a central element in an 8 × 8 array. Boresight gain is 4.54 dBi.

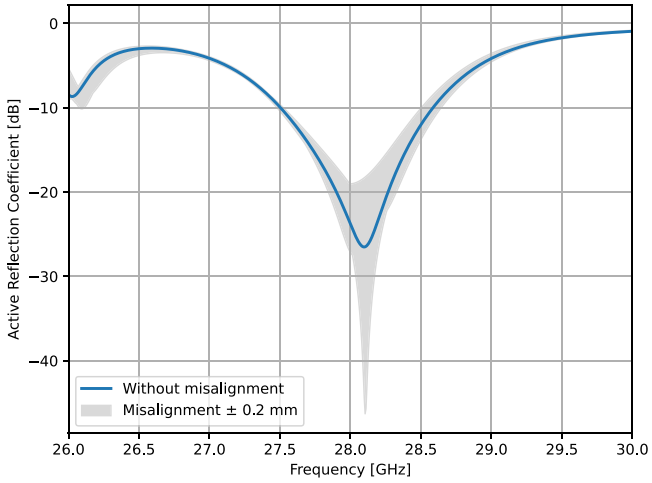


Figure 9. Simulated ARC range of the EDA for various misalignment values obtained through unit-cell simulation.

assembled, offering a practical yet precise manufacturing solution using inexpensive conventional CNC techniques.

The layered structure inherently introduces the possibility of misalignment between adjacent layers along the x- and y-directions. Figure 9 illustrates the simulated impact of such misalignment. Here, the grey region presents the envelope of all misalignment results between ± 0.2 mm. This reveals that the resonance frequency is barely impacted for misalignment on this order; only the matching is deteriorated if the layer alignment is not properly controlled. It is still necessary to carefully align the layers to achieve optimal performance. To facilitate the accurate assembly of the layers, an extended frame was incorporated around the array perimeter to accommodate assembly bolts. These bolts are recessed such that their heads remain flush with the top surface of the array, minimizing any potential adverse electromagnetic effects. The same bolts serve dual purposes, providing mechanical stability and keeping the PCB-based launcher in contact with the metal array structure.

To further understand the implications of manufacturing tolerances on the proposed design, a parameter study was performed specifically on the metal array design. Figures 10 and 11 show the ARC in unit-cell simulations for various values of W_{ridge} and H_{ridge}, respectively. The array response is consistent for tolerances on W_{ridge}; however, this is not the case for H_{ridge}, where even tolerances on the order of 50 μm can produce a noticeable frequency shift. It is therefore important that the height of the ridge is well controlled, which is achievable with the proposed CNC manufacturing methodology.

An 8 × 8 EDA array prototype was fabricated based on the considerations outlined above, with a representative photograph shown in Figure 13. The prototype was evaluated by comparing full-wave simulation-based predictions against measured data obtained from experimental characterization.

Firstly, the ARC of a central array element was measured using a Keysight P5028A vector network analyzer (VNA) [25]. The ARC was determined by measuring the coupling from the element under test to all other elements and then combining these measurements

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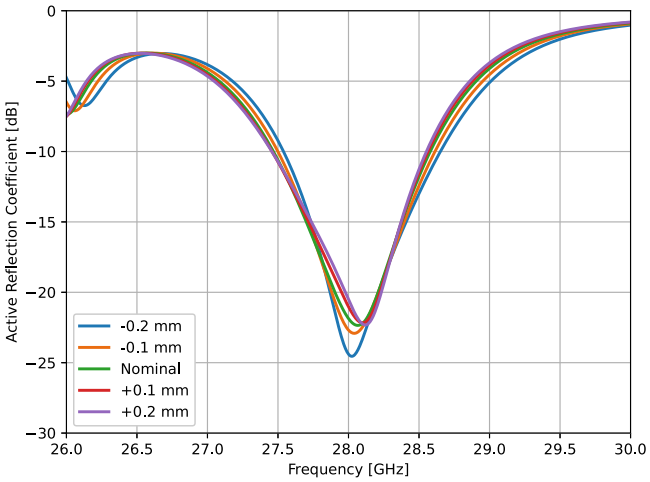


Figure 10. Simulated ARC range of the EDA for various misalignment values obtained through unit-cell simulation.

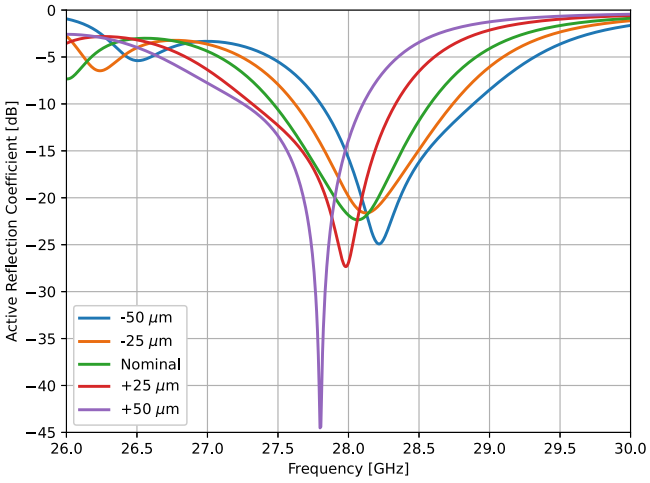


Figure 11. Simulated ARC range of the EDA for various misalignment values obtained through unit-cell simulation.

in post-processing. During these measurements, all other elements were terminated with 50 Ω loads. The simulated and measured performance is illustrated in Figure 15. A slight frequency shift between simulations and measurements can be observed, likely attributable to manufacturing tolerances and minor misalignments during assembly. Despite this shift, the overall measured ARC closely matches the simulated one, confirming the robustness of the electromagnetic characteristics of the developed antenna solution. Furthermore, the maximum inter-element coupling remains below approximately −20 dB across the entire operating frequency band.

Next, the embedded element radiation patterns were experimentally evaluated in a spherical anechoic chamber, as depicted in Figure 14(a). The array was mounted centrally within the chamber on a custom-designed 3D-printed fixture, and a rotating horn antenna probe captured the radiated power levels at multiple elevation angles θ along the E- and H-planes. The horn antenna probe can be rotated, thus allowing for comprehensive co- and cross-polarization characterization.

The measured and simulated embedded radiation patterns for a central array element at 28 GHz are compared in Figure 16(a) (H-plane) and Figure 16(b) (E-plane). The measurements align

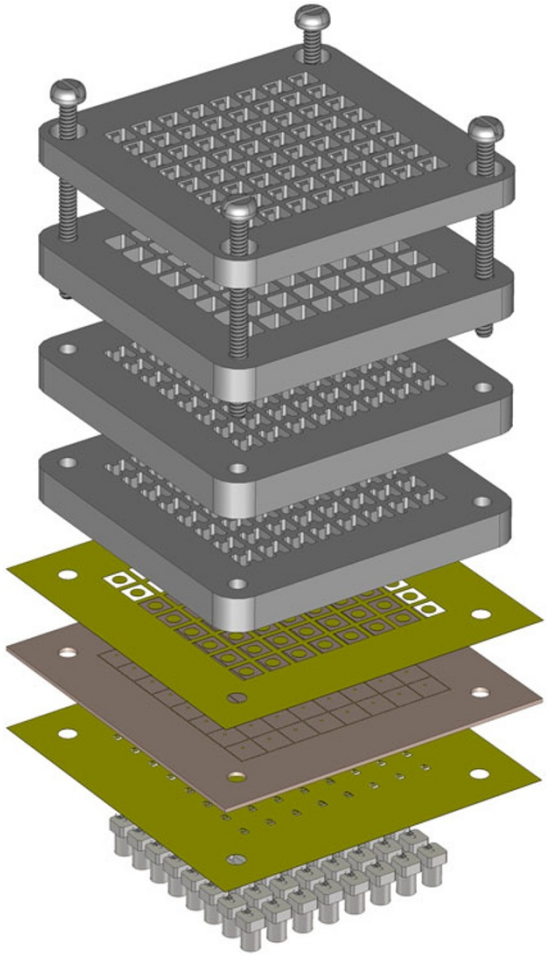


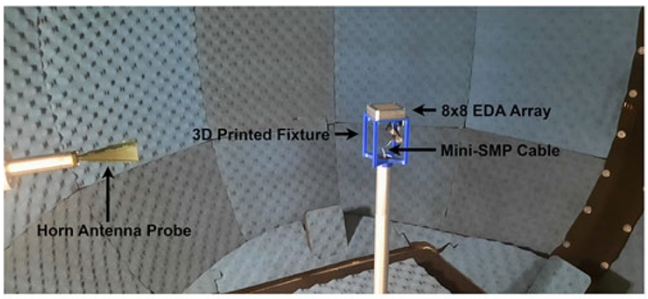
Figure 12. Exploded view of the 8 × 8 EDA array demonstrator assembly.



Figure 13. Photograph of the fully assembled 8 × 8 EDA array prototype used for the experimental measurements.

closely with numerical simulations, aside from minor ripples introduced by spurious reflections occurring in the anechoic chamber.

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(a)



(b)

Figure 14. Photographs of the measurement setups used to validate the performance of the 8×8 EDA array prototype for (a) the embedded radiation pattern measurements in a spherical anechoic chamber and (b) the efficiency measurements in a reverberation chamber.

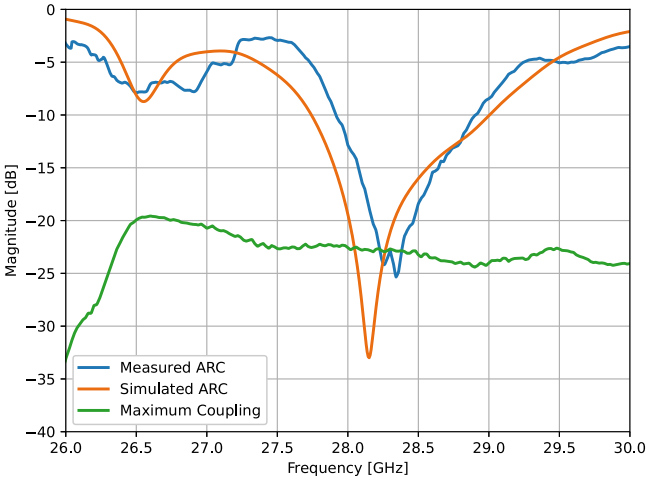
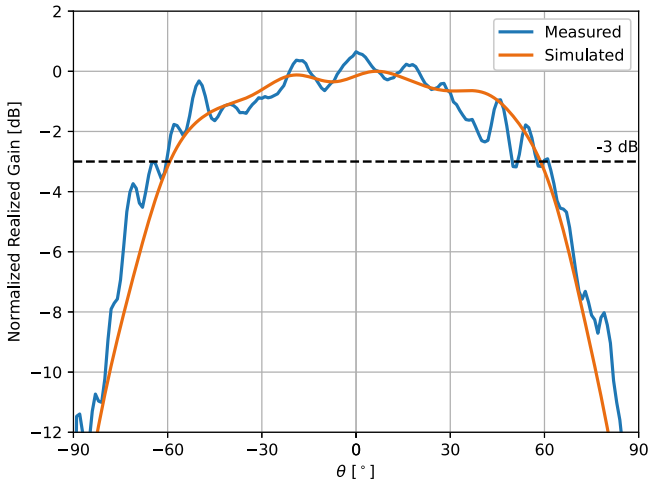
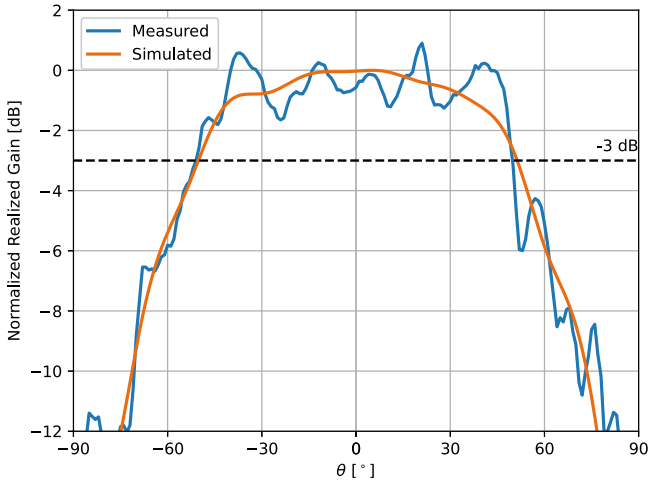


Figure 15. Measured and simulated ARC of a central element in the 8×8 EDA array prototype for boresight scanning. The maximum coupling level between the considered array element and the adjacent ones is also shown.

To mitigate these measurement artifacts, normalization was performed against the average main beam power rather than the peak



(a)



(b)

Figure 16. Measured embedded radiation patterns of a central element in the 8×8 EDA array prototype at 28 GHz compared with simulation results along (a) H-plane and (b) E-plane. Broadside gain measured at 3.45 dBi and simulated at 4.23 dBi.

power level. The agreement in terms of HPBW further supports this alignment, with measured values of 121° (H-plane) and 102° (E-plane) closely matching the simulated values of 119° and 102°, respectively, showing a deviation of at most 2°. From these measurements, the gain of a central element was estimated at 3.45 dBi using a comparative method. The same element achieved a gain of 4.23 dBi in simulation. Since the tolerance of the anechoic chamber is estimated at 1.5 dB, this falls well within the measurement tolerance and is considered a good match; any residual discrepancies can be attributed to manufacturing tolerances as well as additional conductor losses.

Additionally, the array scanning characteristics have been evaluated numerically by combining the measured embedded radiation patterns for individual antenna elements. Figure 17 illustrates a strong agreement between the simulated and reconstructed measured beam-scanning properties at 28 GHz. A 3-dB scanning range of approximately 116° along the H-plane (−60° to 56°) and 96° along the E-plane (−47° to 49°) was experimentally demonstrated. These results closely match the simulated scanning ranges of 112°

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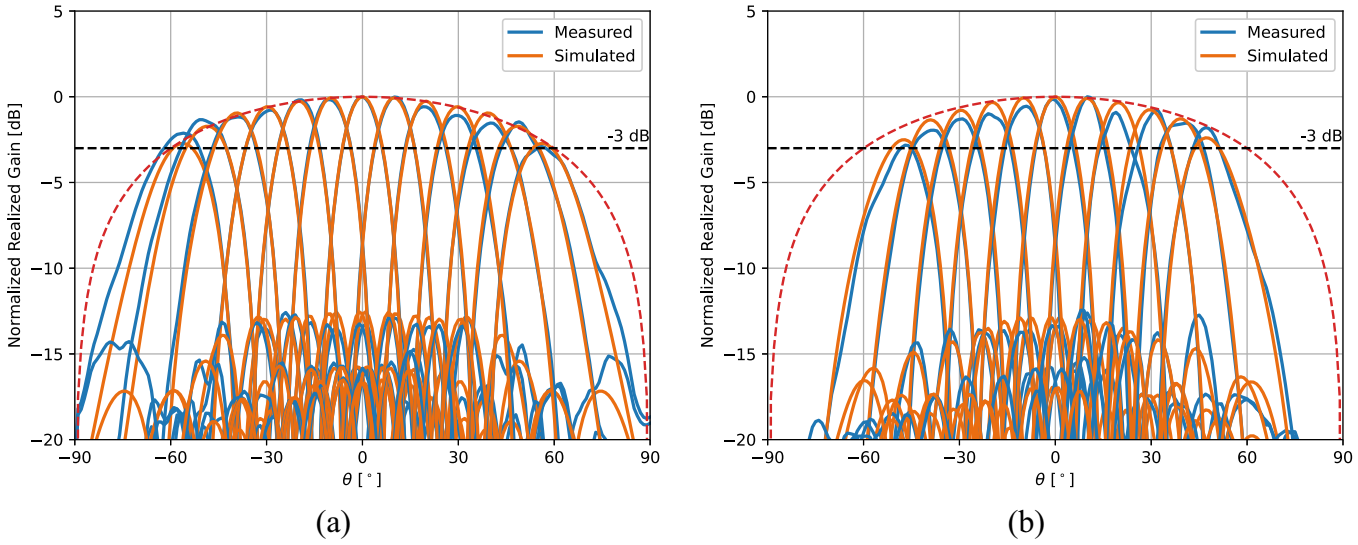


Figure 17. Measured scanning performance of the 8 × 8 EDA array prototype at 28 GHz compared with the simulation results for scanning angles along the (a) H-plane and (b) E-plane. The red, dashed line shows the scan loss as predicted by the cosine law. Broadside gain estimated from measurements at 21.41 dBi and simulated at 21.99 dBi.

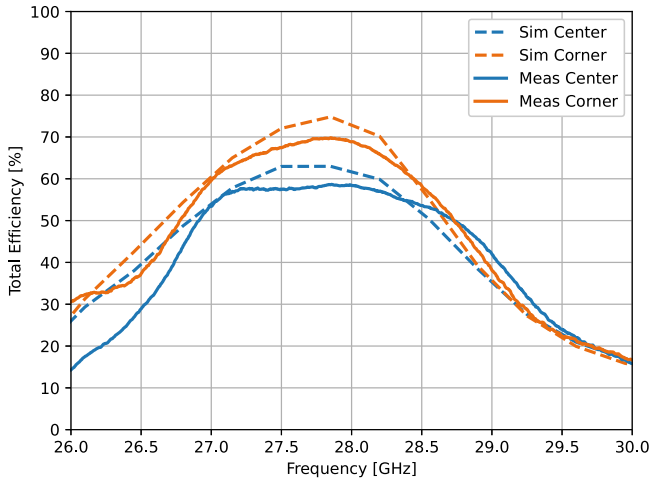


Figure 18. Measured total efficiency of the 8 × 8 EDA array prototype for a center and a corner element compared with simulation results.

(H-plane) and 98° (E-plane), with discrepancies within 4°. Finally, based on the measured performance of the individual antenna elements, the broadside array gain was calculated to be 21.41 dBi, which agrees well with the 21.99 dBi value predicted by numerical electromagnetic simulations.

Lastly, the total efficiency of the array elements was evaluated using the reverberation chamber setup shown in Figure 14(b). During these measurements, the non-active antenna elements were terminated with 50-Ω loads. Figure 18 compares the simulated and measured characteristics for both central and corner elements of the array, indicating excellent agreement with deviations below 5%. Higher efficiencies observed for corner elements compared to central elements highlight the influence of reduced inter-element coupling. Note that the actual efficiency values are likely slightly higher than presented due to additional connector losses included in the reported measurements.

Table 2 summarizes the measured array characteristics and compares them against state-of-the-art metal-based antenna arrays recently reported in the literature. This comparison highlights the competitive performance of the proposed EDA design. It should, however, be emphasized that the efficiency values cited from these references were obtained under conditions that are considerably more favorable. Specifically, in [11], the total efficiency is presented based solely on simulation results for a 4 × 2 sub-array, which naturally experiences reduced coupling losses compared to the full-scale array implementation assessed in our work. Additionally, it is noteworthy that our simulations explicitly incorporate realistic factors, such as surface roughness and connector losses, to provide the most accurate and practically relevant efficiency estimate.

Similarly, the efficiency reported in [17] is evaluated for a single, isolated antenna element, thereby neglecting coupling losses. As discussed earlier, coupling losses significantly contribute to the overall loss budget, making the isolated-element efficiency inherently higher and less representative of practical array scenarios. Furthermore, [26] provides only radiation efficiency obtained through simulation, inherently omitting critical matching and coupling losses, which results in artificially elevated efficiency values.

Finally, we wish to underscore once again the significance of performing comprehensive finite-array simulations. Figure 19 illustrates the scanning performance derived from the unit-cell radiation pattern simulations. It clearly demonstrates significant discrepancies between these unit-cell simulation results and the previously discussed measurement and finite-array simulation outcomes. This discrepancy strongly indicates that unit-cell-based simulations alone cannot reliably predict the true radiation patterns and performance characteristics of practical, full-scale antenna arrays.

Thermal characterization

In the preceding sections, the performance of the proposed EDA array has been analyzed from an electromagnetic perspective. However, one of the primary advantages of a metal-based antenna design lies in its enhanced thermal characteristics, which are especially critical for active array architectures. This section presents a

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Table 2. Performance comparison of state-of-the-art metal-based antenna arrays available in the scientific literature

Reference	Antenna technology	Frequency (GHz)	Impedance bandwidth (%)	Total efficiency (%)	Element spacing (λ_0)	3-dB Scan range (E-/H-plane)	Array size
[11]	Heatsink antenna	10	30	80[S*]	0.53×0.53	100° / 60°	2×4
[17]	Evanescent waveguide	14.25	6.7	93*	0.54×0.54	100° / 100°[S]	16×16
[27]	Slotted waveguide	9.4	2.1	N.A.	0.7	84° / 0°	1×8
[28]	Gap waveguide	28	10.7	N.A.	2.24×0.52	120° / 0°	4×16
[26]*	Open-ended gap waveguide	95	21[S]	89[S**]	0.5×0.6	102° / 100°[S]	Infinite
This work	**Ridged waveguide**	**28**	**4**	**60–70**	**0.5×0.5**	**96° / 116°**	**8×8**

[S] Only simulated result available.
* Achieved using a single standalone element or a smaller subset of the array.
** Radiation efficiency.

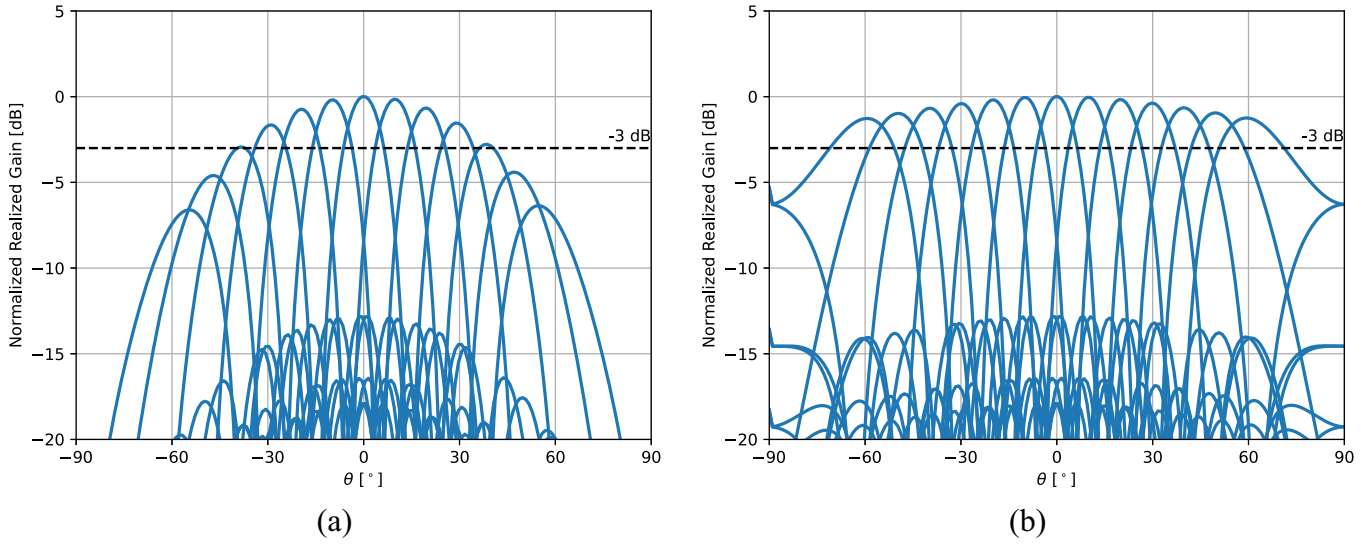


Figure 19. Simulated scanning performance of an 8×8 array at 28 GHz constructed from the unit cell radiation pattern along the (a) H-plane and (b) E-plane.

comprehensive thermal analysis of the EDA array, including both simulation and experimental validation. The thermal performance is also benchmarked against an equivalent patch antenna array structure.

To assess the thermal behavior of the EDA array, it is essential to understand the physical mechanisms governing heat dissipation in an active antenna array system. Active arrays typically rely on BFICs mounted on a PCB, which facilitate electronic beam steering and signal processing. These BFICs inherently generate substantial heat during operation. Efficient heat removal is crucial to maintaining safe junction temperatures and ensuring long-term reliability. The generated heat can dissipate through two primary paths: downward through the PCB to a dedicated heat sink, and upward through the antenna array itself through a dedicated via network. Figure 20(a) illustrates this dual-path thermal behavior.

A widely adopted model to describe this phenomenon is the *two-resistor thermal model* [29], which characterizes the thermal resistances of the top and bottom conduction paths as θ_{top} and θ_{bot}, respectively. These resistances quantify the effectiveness of each path in conducting heat, with lower values indicating superior thermal conduction. The equivalent thermal circuit is shown in Figure 20(b), where thermal resistances are modeled as electrical resistors, temperatures as voltages, and the heat source (with power dissipation P_D) as a current source. Following Ohm's law, the junction temperature T_J can be expressed as:

$$T_J = T_{\text{amb}} + P_D \frac{\theta_{\text{bot}}\theta_{\text{top}}}{\theta_{\text{bot}} + \theta_{\text{top}}}, \tag{9}$$

where T_{amb} denotes the ambient temperature.

To isolate the thermal contribution of the antenna path, both the simulations and the measurements presented in this section are deliberately configured without a bottom heatsink. In the equivalent thermal circuit of Figure 20(b), this corresponds to $\theta_{\text{bot}} \to \infty$ (i.e., an open circuit in the thermal network). Under this condition, (9) reduces to:

$$T_J = T_{\text{amb}} + P_D\theta_{\text{top}}. \tag{10}$$

Equation (10) shows that, in the absence of the bottom-side thermal path, the temperature rise above ambient is governed

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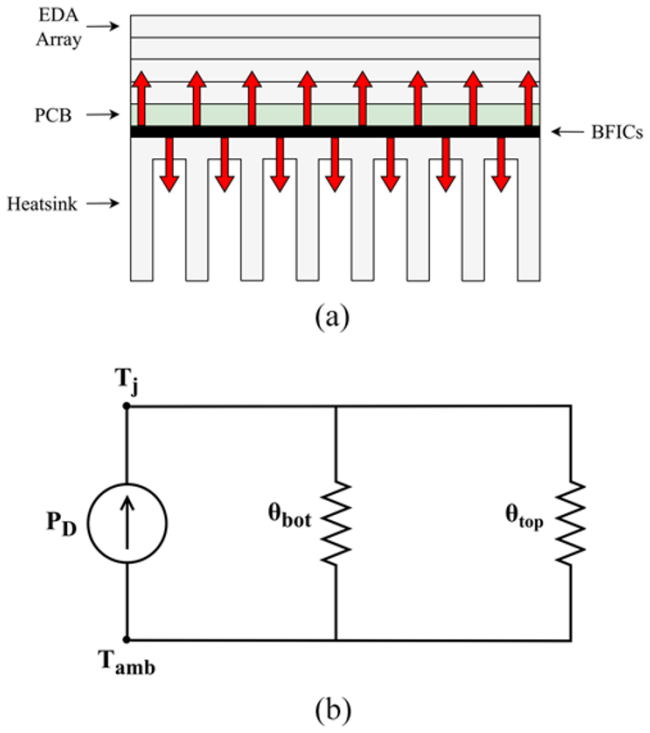


Figure 20. (a) Schematic view of the thermal paths and (b) equivalent circuit describing the thermal behavior of the 8 × 8 EDA array prototype.

entirely by θ_{top}. This open-circuit configuration provides a direct and unambiguous characterization of the thermal resistance of the antenna structure, without requiring any assumption regarding θ_{bot}. The thermal resistance θ_{top} therefore serves as a suitable figure of merit for evaluating the thermal performance of the antenna.

For the antenna path to provide a meaningful contribution to heat dissipation in an operational system, θ_{top} must be comparable to θ_{bot}. In densely integrated mmWave arrays, the bottom-side thermal path is often severely constrained by the limited PCB area and dense BFIC packaging, which can result in θ_{bot} values that are significantly higher than those encountered in conventional lower-frequency systems. Under such conditions, a low θ_{top} becomes critically important, as the antenna structure constitutes the primary parallel thermal conduction channel available for reducing the effective thermal resistance and, consequently, the junction temperature.

To quantify θ_{top}, thermal simulations were performed using COMSOL Multiphysics [30], following the methodology outlined in [31]. Consistent with the open-circuit condition described above, only the metallic portion of the EDA array was included in the model, with no bottom heatsink present. Previous studies have shown that an optimized network of thermal vias can render the thermal resistance of the circuit board negligible [32], ensuring efficient thermal energy transfer from the bottom of the PCB to the antenna structure. The simulation environment included a heat source positioned at the bottom of the array, mimicking the heat generation of BFICs with a heat flow rate equivalent to P_D, as well as a laminar airflow model incorporating natural convection and gravity effects. The thermal resistance was then calculated from (10) as:

$$\theta_{top} = \frac{\Delta T}{P_D}, \tag{11}$$

where $\Delta T = T_J - T_{amb}$ represents the temperature difference between the array and the ambient temperature.

Figure 21 presents the simulated steady-state temperature distribution of the EDA array. The maximum temperature was found to be 53.6°C. Substituting into (11) yields a thermal resistance of 11.67 K/W. For comparison, the same simulation procedure was applied to a commercial patch antenna array described in [33], resulting in a thermal resistance of 123.3 K/W. This highlights the superior thermal performance of the proposed EDA array, which achieves more than an order-of-magnitude improvement.

To validate the simulation results experimentally, a thermal measurement setup was developed. Figure 22 shows a photograph of the setup, which consists of two primary components. The first component is the EDA array prototype, thermally coupled to a resistive heating element and mounted on a 3D-printed fixture. The heating element is, in turn, connected to a controllable power source and generates heat by converting electrical power, effectively mimicking the physical mechanism modeled in the numerical thermal simulation. The heating element is a purely resistive load that converts all supplied electrical power directly into heat (Joule heating), so the generated thermal power equals the electrical input power ($P_D = V \times I = 2.88$ W). The second component is an overhead thermal camera mounted on a fixed platform, which captures the surface temperature distribution of the array, allowing for the evaluation of the relevant thermal resistance. As in the simulation, no bottom heatsink is present, so that the open-circuit condition $\theta_{bot} \to \infty$ holds and the measured temperature rise is governed entirely by (10).

Thermal measurements were performed by operating the heating element at a power of 2.88 W. Prior to each measurement, the array was cooled to ambient temperature to ensure repeatability. Figure 23 displays the thermal camera images from four separate measurement iterations. The maximum temperature across the measurements remained highly consistent, exhibiting a variation of no more than 0.3°C. Using the measured ΔT and known power dissipation level within the heating element, the thermal resistance of the EDA array structure was calculated using (11), yielding a value of 11.11 K/W. This result closely matches the simulated value (within 0.55 K/W), thereby validating the design methodology and confirming the superior thermal performance of the EDA array. The measured value is comparable to typical junction-to-board thermal resistances reported in the mmWave active array literature [9], further confirming that the antenna path provides a substantial parallel thermal conduction channel in practical array configurations.

Conclusion

This paper has introduced and experimentally validated a novel thermally enhanced EDA array tailored for mmWave wireless communications. The proposed design leverages a fully metallic, layer-based construction to enable improved heat dissipation, wide-angle scanning capabilities, and integration with planar electronics via a PCB-based launcher structure. This architecture addresses one of the critical bottlenecks in high-frequency active antenna systems: excessive temperature rise due to densely integrated, low-efficiency beamforming electronics.

An 8 × 8 EDA array prototype was rigorously evaluated through full-wave simulations and validated through comprehensive experimental characterization, including ARCs, embedded radiation patterns, beam-scanning characteristics, and thermal

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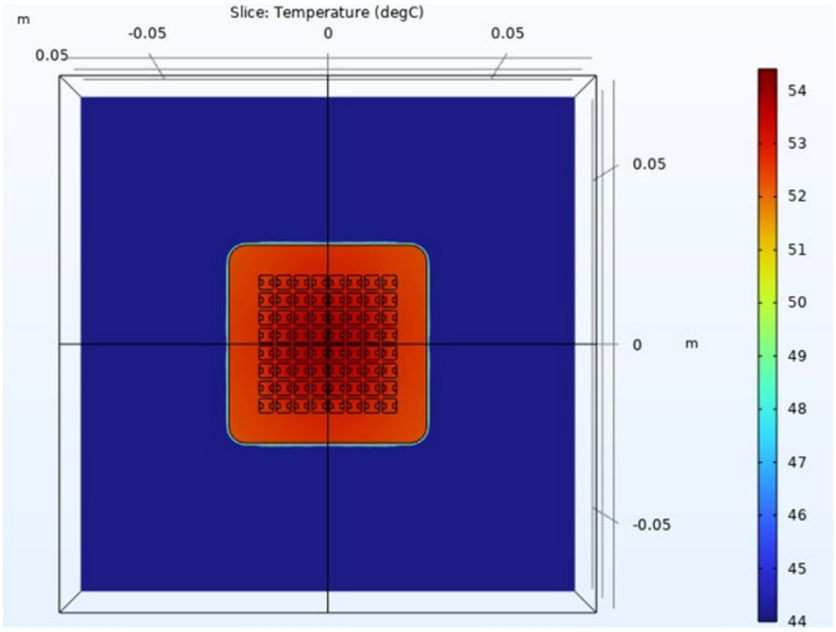


Figure 21. Simulated temperature of the EDA array using COMSOL Multiphysics.

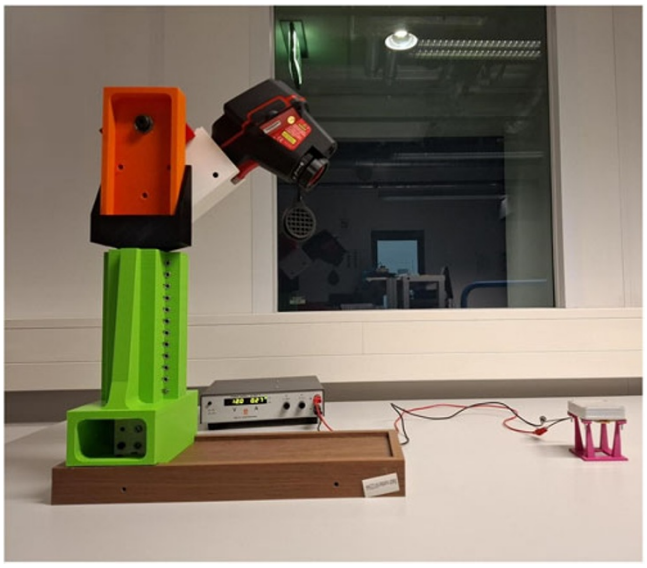


Figure 22. Photograph of the thermal measurement setup used to measure the thermal resistance of the EDA array prototype.

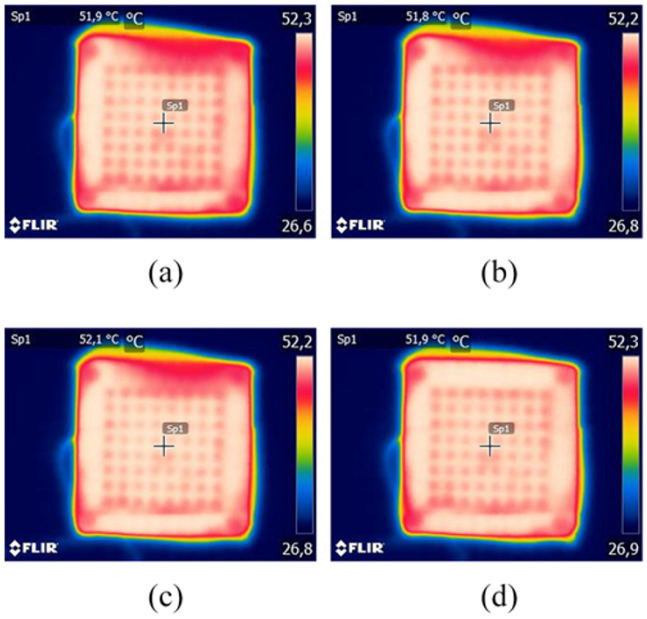


Figure 23. Measured steady-state temperatures of the EDA array for four separate measurements using the described measurement setup.

resistance measurements. Electromagnetic performance assessments revealed a wide scanning range of 116° and 96° along the H- and E-planes, respectively, with excellent agreement between simulated and measured results. The array demonstrated robust radiation properties even in the presence of manufacturing-induced deviations and bandwidth limitations imposed by the launcher structure.

From a thermal standpoint, the EDA array showcased a remarkable improvement over conventional patch antenna arrays. Thermal simulations and measurements confirmed a thermal resistance of 11.11 K/W, more than an order of magnitude lower than that of a standard PCB-based patch array (measured at 123.3 K/W). These findings validate the EDA array as a highly promising solution for thermally constrained mmWave active array systems, offering a viable pathway toward practical, scalable, and thermally efficient implementations.

Despite the promising results achieved in this study, several avenues remain open for further exploration:

- *Active array integration:* The current work has focused on passive measurements and thermal characterization. A logical next step is to integrate BFICs with the proposed EDA array to evaluate system-level performance in an active environment, including thermal behavior under realistic operating conditions and beam-steering accuracy under dynamic loading.

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- *Launcher optimization:* While the PCB-based patch launcher simplifies integration with planar electronics, it imposes limitations on the achievable impedance bandwidth. Future research may explore advanced launcher designs such as stacked or aperture-coupled patches, wideband ridge-to-microstrip transitions, or additive manufacturing-based feeds to extend the array's operational bandwidth.
- *Dual-polarization implementation:* Although the current EDA design supports only single polarization, the structure is inherently extendable to dual polarization. Implementing and characterizing a dual-polarized version would broaden the array's applicability to multiple-input multiple-output (MIMO) systems and polarization-diverse mmWave architectures.
- *Thermal management enhancements:* Further thermal performance gains could be achieved through advanced cooling strategies such as topology-optimized heat sinks. Additionally, co-design approaches that simultaneously consider RF and thermal constraints during the array design process may yield superior trade-offs.
- *Large-scale arrays and system-level evaluations:* Extending the EDA concept to larger array sizes and evaluating its impact on full 5G/6G transceiver systems, including link-level performance, electromagnetic interference, and robustness under varying environmental conditions, constitutes a critical direction for real-world deployment.
- *Manufacturing tolerances and reliability:* Although the proposed layered CNC-manufacturing approach is efficient and reproducible, further studies are needed to assess long-term mechanical reliability, tolerance to thermal cycling, and sensitivity to tolerances or manufacturing variations in large-scale production.

Through development along these lines, the presented EDA array design approach may evolve into an effective technology for next-generation mmWave networks, enabling high-gain, wide-angle scanning arrays that are not only electrically efficient but also thermally resilient.

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Competing interests. The author(s) declare none.

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Real-life environment effects

A.1. Impact of amplitude and phase errors

Until now, the EDA array performance has only been investigated under ideal feeding conditions. In practice, however, feeding networks will inevitably exhibit phase and amplitude errors due to component tolerances, manufacturing variations, and temperature-dependent behavior [34, 35]. To understand the impact of these non-ideal conditions on the radiation pattern characteristics of the proposed EDA array, a Monte Carlo sensitivity analysis was carried out by generating 500 independent realizations of per-element phase and amplitude errors. The errors were modeled as independent zero-mean Gaussian random variables applied individually to each of the 64 elements. The phase error was modeled with a standard deviation of $\sigma_\phi = 10^\circ$ and the amplitude error with a standard deviation of $\sigma_A = 1$ dB, representing realistic tolerances for a millimeter-wave feeding network operating at 28 GHz. Three test cases were evaluated independently: phase errors only, amplitude errors only, and a combined case in which both types of error were applied simultaneously. For each simulation scenario, the mean response and the envelope over all realizations are reported.

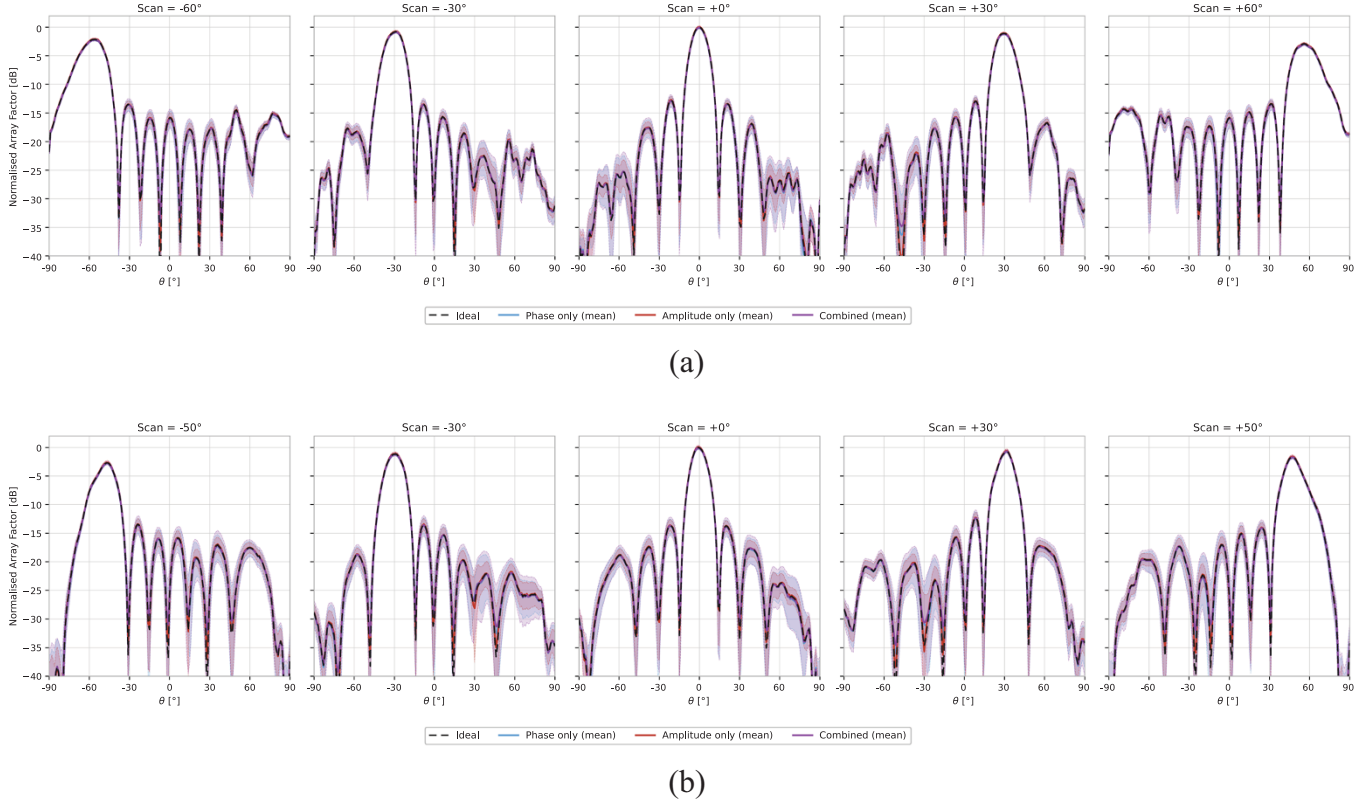


Figure A1. Monte Carlo analysis of phase and amplitude errors for the 8×8 EDA array at 28 GHz: (a) $\phi = 0^\circ$ cut plane; (b) $\phi = 90^\circ$ cut plane. The analysis assumes a phase-error standard deviation of $\sigma_\phi = 10^\circ$, an amplitude-error standard deviation of $\sigma_A = 1$ dB, and $N = 500$ Monte Carlo iterations.

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Figure A2. BINDER MKF 56 dynamic climate chamber used for the thermal cycling characterization of the EDA array prototype.

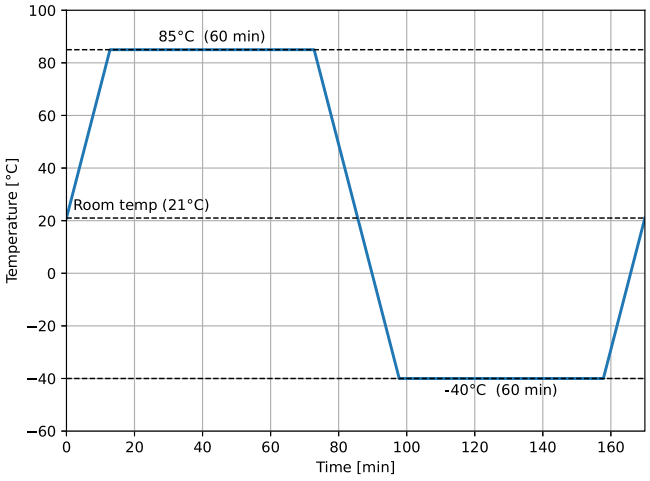


Figure A3. Time distribution of the individual thermal cycle in the mechanical reliability test of the proposed EDA array.

Figure A1 shows the resulting array radiation patterns for various scanning angles along both the $\phi = 0^\circ$ and $\phi = 90^\circ$ vertical cut-planes. As expected from the zero-mean Gaussian error model, the mean pattern across all realizations closely follows the ideal case for every scanning angle. The main beam is largely unaffected by the applied errors, which can be attributed to the spatial averaging effect of the large 64-element array, where uncorrelated element-level perturbations partially cancel in the far field. The sidelobe region, however, exhibits greater sensitivity to both phase and amplitude errors, with individual realizations showing sidelobe levels elevated above the ideal pattern. This behavior is consistent with established phased array theory, where random element errors are known to raise the average sidelobe level while leaving the main beam gain and direction largely intact [36].

Thermal cycling characterization

To further understand the robustness of the presented design against real-life environments, a thermal cycling test was performed on the EDA array in accordance with IEC 60068-2-14 [37]. This standard specifies procedures for assessing the ability of components and assemblies to withstand exposure to repeated temperature extremes with a controlled transition rate.

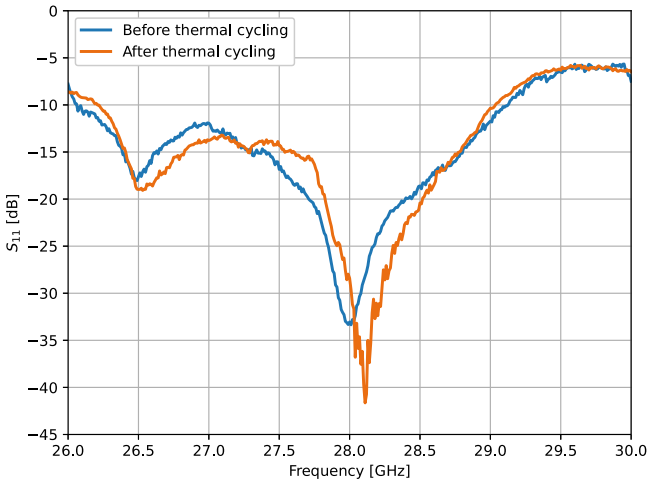


Figure A4. Magnitude of the reflection coefficient as measured at the input of the central EDA array element before and after the thermal cycling test.

The thermal cycling tests were carried out using a BINDER MKF 56 dynamic climate chamber [38], shown in Figure A2. This chamber features a 60-liter stainless-steel interior with internal dimensions of 400 × 420 × 348 mm, which comfortably accommodates the 8 × 8 EDA array prototype. The MKF 56 supports a temperature range of −40°C to +180°C with average heating and cooling rates of 5 K/min (per IEC 60068-3-5), a temperature fluctuation of ±0.1 to ±0.5 K depending on the setpoint, and a temperature variation of ±0.5 to ±1.5 K. The chamber employs APT.line™ preheating chamber technology to ensure homogeneous thermal conditions throughout the test volume, and is equipped with a controller that allows time-segment programming of custom thermal profiles with adjustable ramp functions. Temperature monitoring is performed by means of an internal Pt 100 sensor, while thermal insulation is provided by CFC-free PUR foam. These specifications ensure that the thermal cycling parameters prescribed by IEC 60068-2-14 are met with sufficient margin across the entire test volume.

The EDA array prototype was placed inside the chamber on a stainless-steel rack and subjected to five complete thermal cycles between −40°C and +85°C. Each cycle consisted of a controlled ramp from room temperature to the upper extreme of +85°C at a rate of 5°C/min, a dwell time of 60 minutes at +85°C, a controlled ramp down to −40°C at 5°C/min, a dwell time of 60 minutes at −40°C, and a final return ramp to room temperature. The time profile of a single thermal cycle is shown in Figure A3. This profile was programmed directly into the MKF 56 controller and executed automatically for five consecutive cycles without interruption.

To assess any degradation in RF performance caused by the thermal cycling, the S_{11} of a central array element was measured before and after the complete five-cycle sequence using a VNA. The results are compared in Figure A4. The measured response remains consistent after thermal cycling, with no significant frequency shift or impedance degradation observed. The minor differences between the two traces are attributed to measurement repeatability and connector repositioning between the pre- and post-cycling measurements. These results confirm that the layered CNC-machined aluminum construction of the EDA array, including the bolted assembly and the PCB-based launcher interface, is mechanically robust against the thermal stresses induced by repeated cycling over a 125°C temperature range.

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Guilherme Theis: Biography not available at the time of the publication of the paper.



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