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A 3-bit load-pulling digital power amplifier

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Abstract

A radio frequency (RF) 3-bit digital power amplifier (DPA) is described in this paper. It consists of three RF amplifiers connected at their outputs with a transmission line (TL) network. The three amplifiers are designed for different output powers (P_{OUT}). The TL network allows them to load-pull one other to achieve eight different amplitude states by alternatively enabling and disabling the amplifiers via their gate bias. A prototype was designed in the National Instruments' Microwave Office (MWO) for 500 MHz with the aid of a genetic algorithm to optimize the TL network for all seven active (on-) states. The optimizer efficiencies goals were based on data derived from load-pull simulation. The P_{OUT} goals were based on a 1 V_{rms} step-size. In simulation, ≥50% efficiency was achieved at all on-states with 29.7 dBm peak P_{OUT}. A practical prototype based on the simulation achieved an efficiency of ≥40% over all seven on-states. A peak P_{OUT} of 28.9 dBm was achieved, with the lowest state at 22.4 dBm.

Research Paper

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Introduction

In a transmitter system, the radio frequency (RF) power amplifier (PA) generally consumes most of the DC power. The high peak-to-average power ratios (PAPR) of modern digital communication and broadcast standards tend to reduce average PA power efficiency, as the PA spends most of its operating time at the average P_{OUT} while still needing an operating range that covers the peaks. It therefore becomes necessary to develop PA architectures which can achieve a high efficiency at the average P_{OUT} – a region often referred to as "back-off". Several techniques have appeared over the last 80 years to meet this requirement including Envelope Tracking/Modulation [1], Doherty [2], Outphasing [3], and Dynamic Load Modulation (DLM) [4]. These can all be classed as analog techniques, and although capable of good performance, are limited in their dynamic range, and hence ability to efficiently amplify high PAPR signals.

The limited dynamic range has led some researchers to investigate alternative architectures inspired by digital-to-analog converters (DAC). The majority of this though has focused on 1-bit architectures using sigma-delta-modulation [5]. Due to the high switching speed needed by the class D output stage, these must be integrated, limiting their P_{OUT}, which rarely exceeding 1 W [6]. An alternative to 1-bit architecture exists where multiple amplifiers operate in parallel to recreate the signal envelope. These also tend to be integrated, but this paper will discuss an architecture that can be implemented with discrete devices opening up possibilities of digital power amplifiers (DPAs) operating at transmit powers in excess of 1 W.

This paper is organized as follows: section "Parallel digital power amplifier" discusses the basic parallel DPA architecture and its operation including the target output powers for each state. The critical output transmission line (TL) network is discussed in its own subsection. Simulated results are presented in section "Simulated digital power amplifier results", including electromagnetic (EM) simulated results of the output network. The practical implementation is discussed in section "Practical implementation". Practical results are presented in section "Results" and conclusion given in section "Conclusion".

Parallel digital power amplifier

The basic structure of a DPA consisting of multiple amplifiers connected together with a TL network is composed as shown in Fig. 1. A constant amplitude phase-modulated RF signal is applied to all amplifiers simultaneously. A digital interface D_{1-3} enables and disables individual amplifiers for conveying envelope amplitude information to the output. The TL network allows the amplifiers to interact with one another as they are alternatively enabled and disabled. It can be of any arbitrary topology tailored to best suit the application; a vast number of possible topologies exist.

For efficient operation, the amplifiers should operate at or near their saturation point where their individual output voltage swing is at its maximum for a given supply voltage (V_{DC1-3}) and be maintained during all of their particular on-states. Figure 1 consists of three amplifiers with seven on-states and one off-state, resulting in a total of eight. The number of amplifiers

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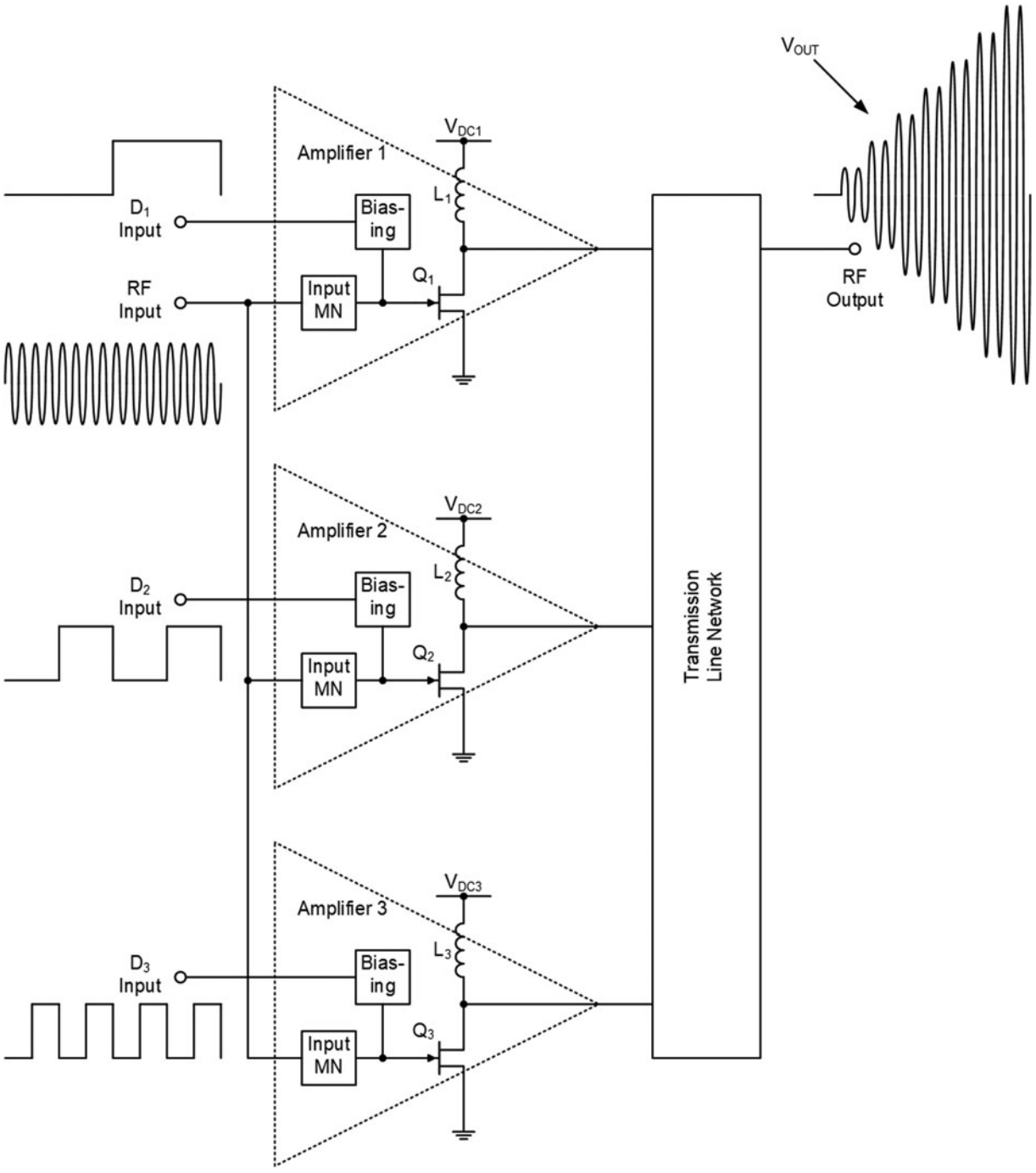


Fig. 1. Three-bit digital power amplifier schematic.

can be increased, resulting in a greater number of output states. An amplifier is enabled by applying a voltage just above its threshold voltage (v_{th}) to its gate. This allows it to supply current to the TL network in-phase with that produced by other enabled amplifiers. These currents add in the network and produce an RF voltage output across an RF load. An amplifier is disabled by applying a strongly negative voltage to its gate. A disabled amplifier appears to the TL network as a purely passive network composed only of its stray parasitic components. It is assumed that when disabled, the drain-source capacitance (C_{DS}) dominates, and hence the devices can be approximated as their C_{DS} only.

When an amplifier switches from supplying current to the TL network, to appearing as only C_{DS}, in this way, it will cause a change in the impedance presented to the output port of the other operating amplifiers, an effect which is known as load-modulation [7]. Load-modulation is the process that both Doherty [2] and Outphasing [3] PAs achieve high efficiency at back-off. By changing this impedance, the output current of an individual amplifier and therefore its own P_{OUT} will change. This mechanism enables the complete DPA to achieve its eight unique P_{OUT} states with only three amplifiers. Two possible states for the DPA are shown in Fig. 2. One advantage of this

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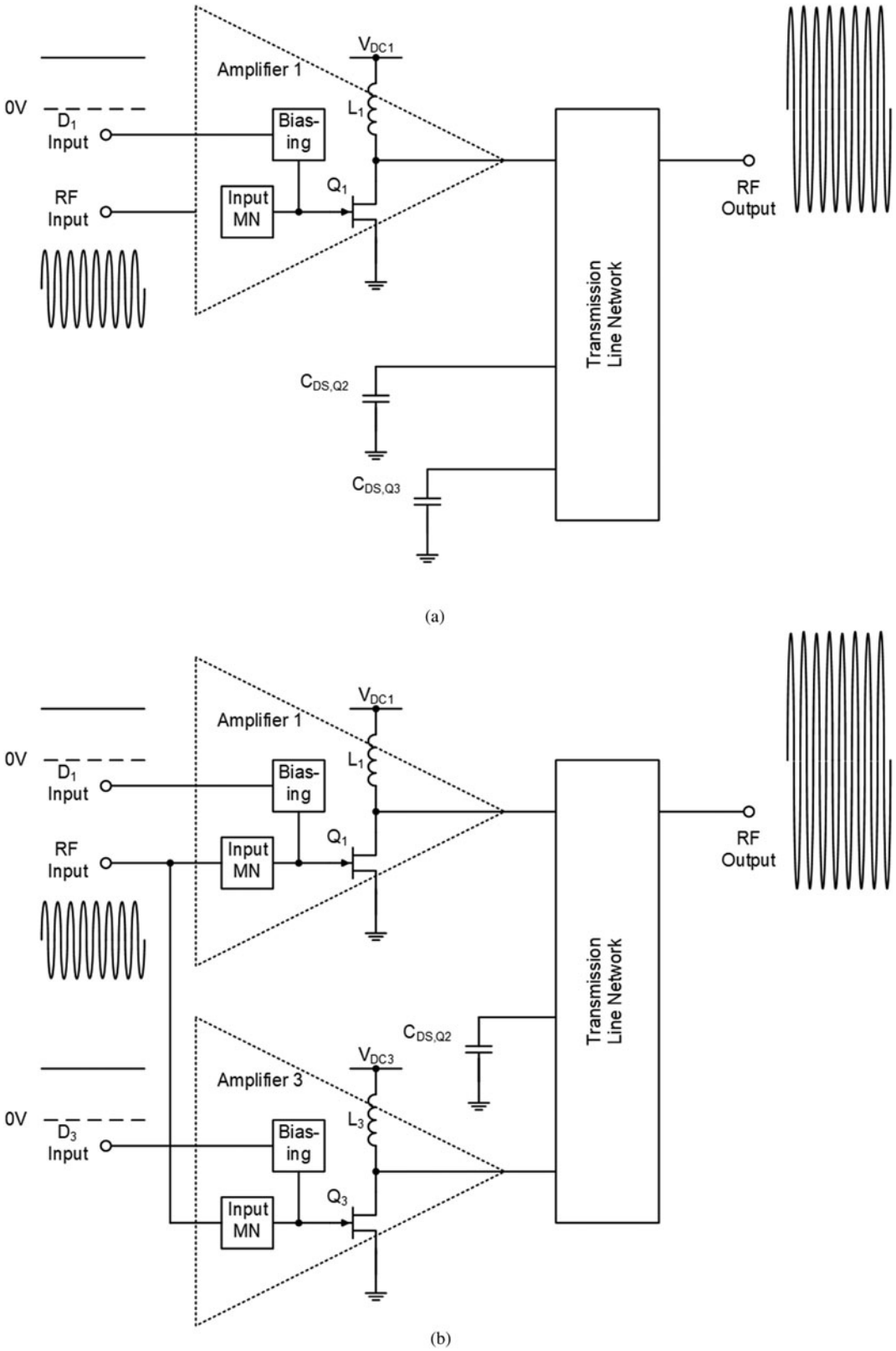


Fig. 2. Three-bit digital power amplifier (a) state 100 and (b) state 101.

architecture is that the digital inputs operate at baseband rate, as opposed to some DPAs where they operate at the RF carrier frequency [8]. Simulations in the National Instruments' Microwave Office (MWO) revealed that the C_{DS} of the GaAs devices remained fairly consistent between being enabled with a positive bias and disabled with a large negative bias.

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Table 1. Target P_{OUT} and V_{OUT} for each state

State	Amplifier 1	Amplifier 2	Amplifier 3	P_{OUT} (dBm)	V_{OUT} (V_{rms})
0	Off	Off	Off	N/A	N/A
1	Off	Off	On	13.0	1
2	Off	On	Off	19.0	2
3	Off	On	On	22.6	3
4	On	Off	Off	25.1	4
5	On	Off	On	27.0	5
6	On	On	Off	28.6	6
7	On	On	On	29.9	7

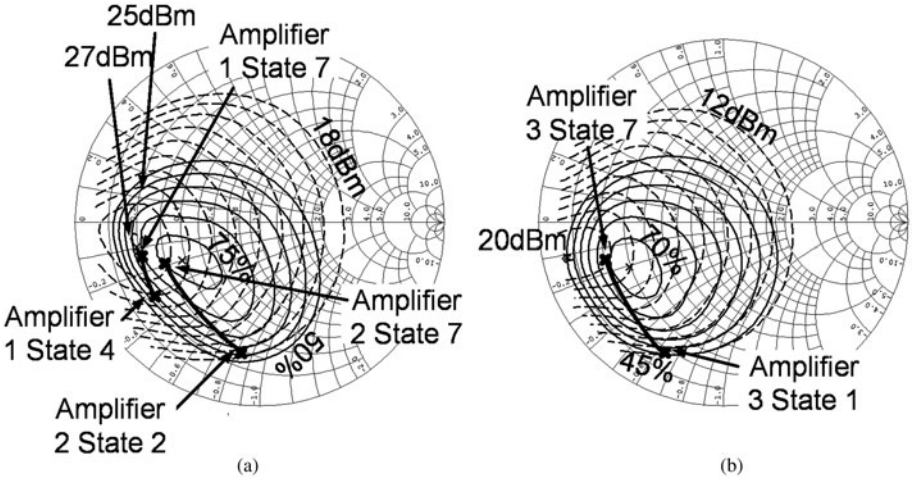


Fig. 3. Optimum load-pull trajectories, efficiency contours are solid thin lines, P_{OUT} contours dashed and the load-pull trajectories in thick black lines: (a) amplifier 1 and amplifier 2 (ATF50189) and (b) amplifier 3 (ATF54143).

To demonstrate the principle, a low-power prototype based around three GaAs FET devices manufactured by Avago/Broadcom was designed. The devices are: ATF50189 for amplifiers 1 and 2, and ATF54143 for amplifier 3. Although low power, these devices demonstrate the ability of this DPA architecture to use discrete devices and therefore the potential to extend it to higher peak P_{OUT}s with the right devices. This moves DPAs away from the worlds of mobile phones and WiFi to base stations and digital TV broadcast transmitters [9]. Since this work is inspired by DACs, a linear voltage step size is specified. A peak P_{OUT} of 1 W is specified which is approximately 7 V_{rms} and fits well with all seven on-states. The intended P_{OUT} and V_{OUT} of every state is shown below in Table 1.

It will be observed from Table 1 that each amplifier is load-pulled over a large P_{OUT} range. In state 7, all devices should operate near their saturated power and be capable of being load-pulled over a 7 dB P_{OUT} range. This is based on the expectation that amplifier 1 supplies 27 dBm, amplifier 2 26 dBm, and amplifier 3 20 dBm. Amplifier 1 has the easiest job since it needs to only operate over 1.9 dB, compared to the 7 dB of the other two. To prove this hypothesis, the GaAs devices were load-pull simulated in MWO at 500 MHz. The simulated results are shown in Fig. 3 which highlights the expected efficiency for each state.

Ideally, each device should trace a load-pull trajectory that bisects all of their required P_{OUT} states, while remaining within a high-efficiency region. The load-pull simulations suggest this is possible, with amplifier 1 staying above 65%, amplifier 2 above 55%, and amplifier 3 above 50%. This assumes that the TL network in combination with the enabling and disabling of the transistors provides enough load-pulling to present the ideal impedances to all amplifiers at all states. Producing a TL network capable of this is challenging, as it is not immediately obvious what topology should be adopted.

Output transmission line network

As a starting point, a TL network inspired by the Rat-Race coupler [10] was used. The development of the TL output network from the classic Rat-Race coupler is shown in Fig. 4. This is probably not the optimum network, but was well known to the author from previous work. The ideal load-pull trajectories shown in Fig. 3 track the imaginary impedance plane. How close the DPA tracks these trajectories depends on the topology of the output network and the C_{DS} presented by the amplifiers in their off-state.

A traditional Rat-Race coupler is shown in Fig. 4(a), where TL_{1-6} are a quarter wavelength in length and if the coupling ratio is equal to impedances of 70.7 Ω in a 50 Ω system. The difference port is removed in Fig. 4(b), to reduce the power lost at that port when the signals applied to input 1 and input 2 are not equal. A terminated difference port in Fig. 4(a) isolates input 1 and input 2. This is usually a desired feature of a power coupler. In this work though, we specifically want input 1 and input 2 to be non-isolated so that one can influence the other to provide load-pull. In Fig. 4(c), TL_7 and TL_8 of Fig. 4(b) are combined to form TL_{16} as are TL_{11} and TL_{12} into TL_{15}. The coupler of

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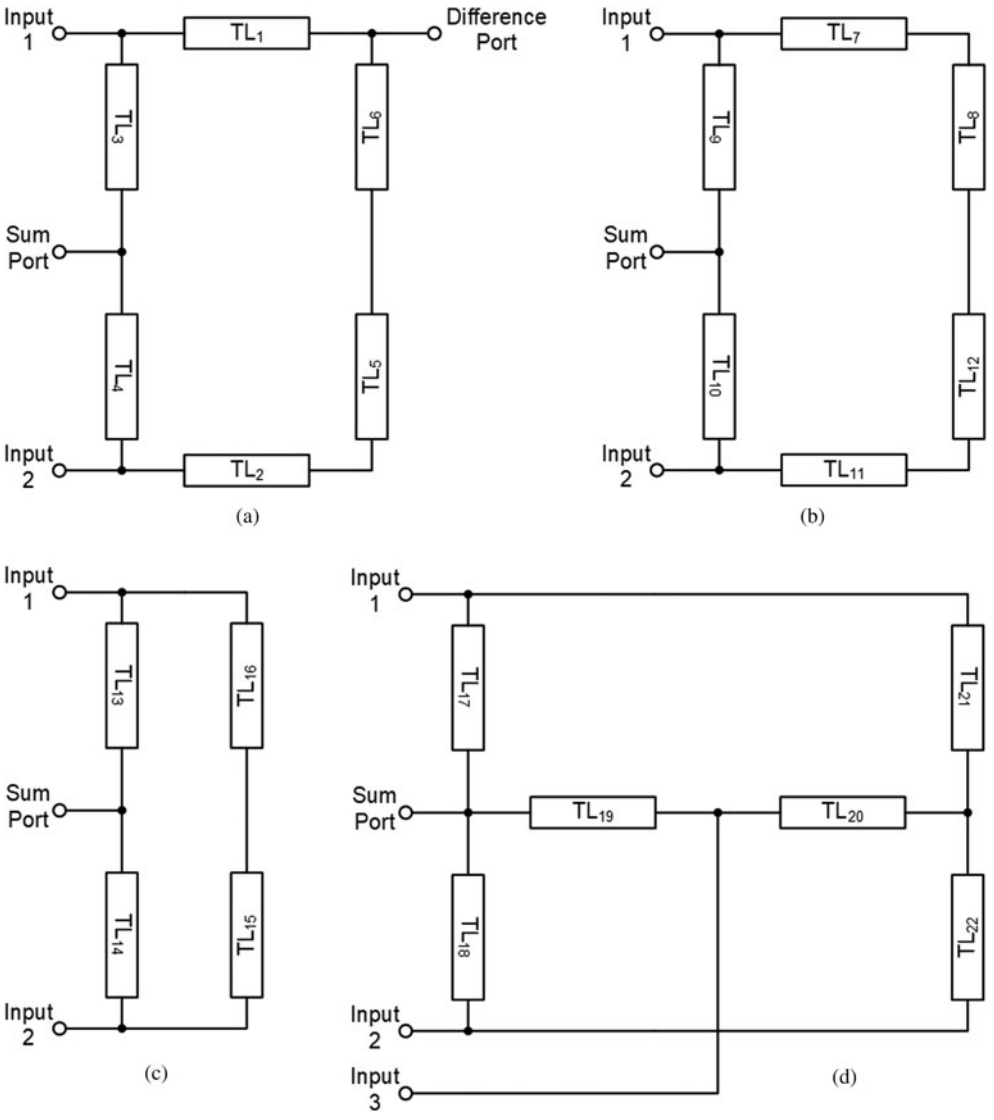


Fig. 4. TL output network development: (a) Rat-Race coupler, (b) Rat-Race coupler with difference port removed, (c) TL_7 and TL_8 combined into TL_{16} and TL_{11} and TL_{12} combined into TL_{15}, (d) 3-input Rat-Race coupler without difference port.

Fig. 4(c) is extended to the three-input network shown in Fig. 4(d) with the addition of TL_{19} and TL_{20}. This configuration maintains the sum port with only one TL between it and the additional input (input 3) and also one additional TL to the node between TL_{21} and TL_{22} which is equivalent to the node between TL_{15} and TL_{16} of Fig. 4(c). This arrangement maintains two paths between each amplifier to encourage load-pull between amplifiers 1–3 shown in Fig. 2. The network developed in Fig. 4 is just one possible topology for a discrete DPA like that described in this work. An almost infinite number of alternatives are available which may provide better performance and will be the subject of future work in this area.

Simulated digital power amplifier results

In the initial stages of the DPA, all TL lengths in the output network were set to a quarter wavelength. The genetic algorithm (GA) optimizer available in MWO was set to tune the lengths and widths of all TLs. GAs have previously been used successfully to optimize the output matching networks of multiband PAs [11] and dimensions of planar antennas [12]. The optimizer was also able to independently tune the supply voltages (V_{DS}) to the three amplifiers and a fixed delay between them. After tuning during optimization, a consistent delay between the paths was kept for all states. The P_{OUT} goals for the optimizer were set out as in Table 1 with efficiency goals set to >50%. The simplified layout in Fig. 4(d) was modified to include additional TLs between the drain terminal of each amplifier and output network to supply DC current, and bends and joints so that all loops could be maintained resulting in the layout shown in Fig. 5. It will be noted that the port connecting to amplifier 1 is in the middle of the board. This is a drawback of this architecture as it requires RF signal lines to cross over one another. After optimization, the results are presented in Fig. 6.

The results in Fig. 6 show that seven unique on-states can be achieved at ≥50% efficiency. V_{OUT} does not follow the linear relationship defined in Table 1, but does show a general progression with a positive gradient. This suggests that the output network proposed in this work provides a partial solution to the problem of trying to present the optimum impedances to the devices at all

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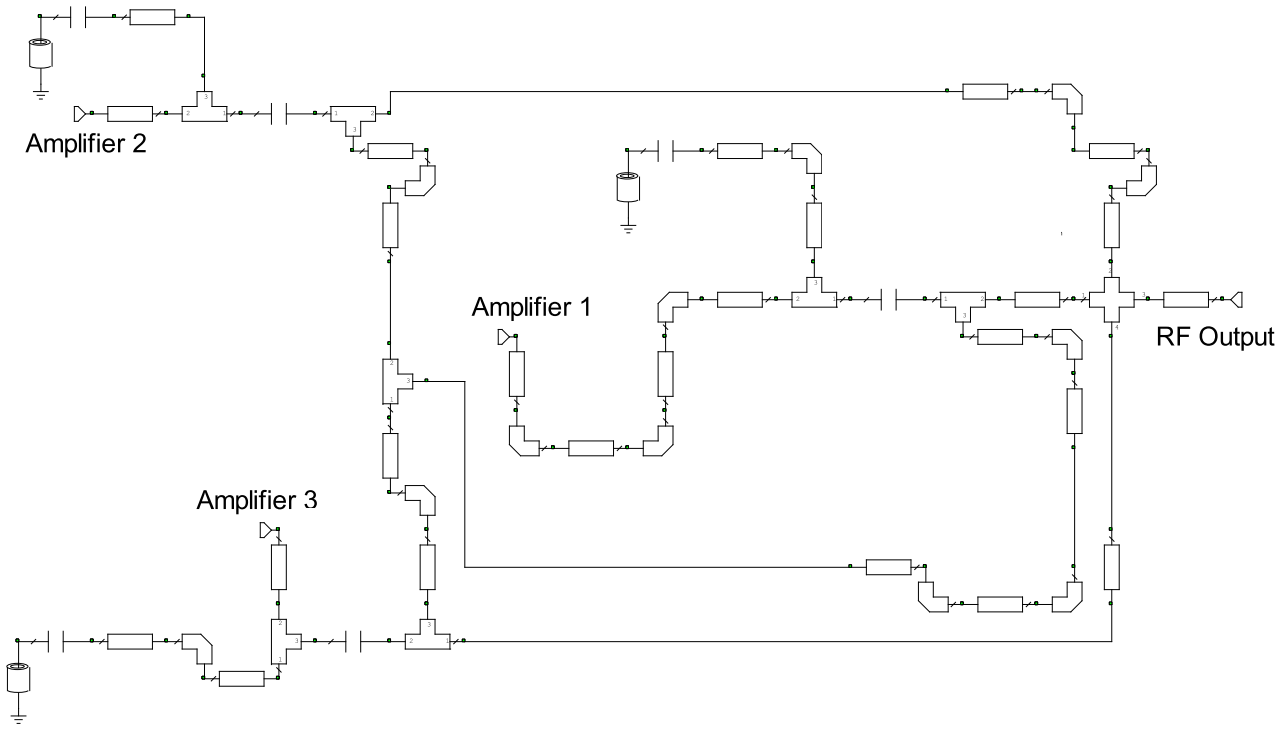


Fig. 5. Full layout for output network.

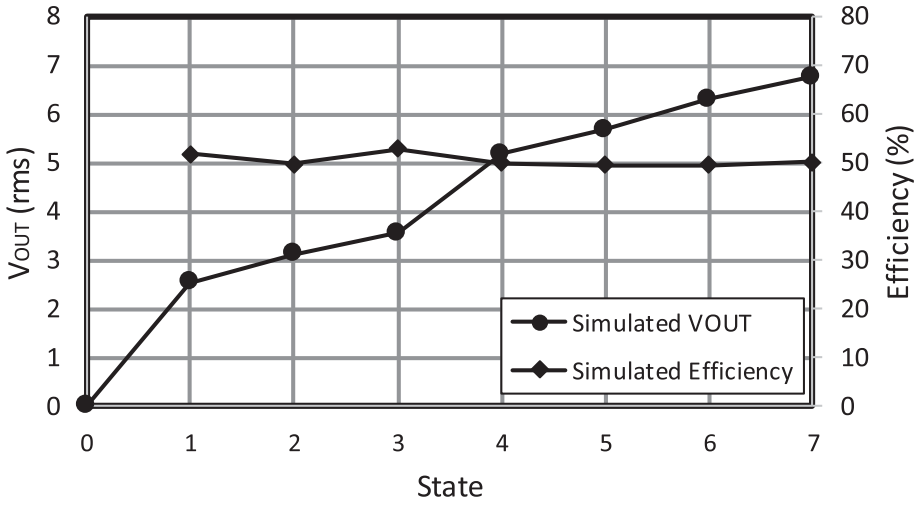


Fig. 6. Simulated results of load-pull DPA.

seven on-states. However, it does suggest that the concept is valid and that other networks may exist which can provide a more complete solution. Peak P_{OUT} is 1.2 W (30.6 dBm). The simulated phase response is shown in Fig. 7, where the phase response of the DPA varies by over 90° across the various states. This can either be compensated by applying the appropriate phase offset when mapping the signal onto the constellation diagram points or with digital pre-distortion (DPD). The variation in phase is likely due to the interaction between the currents generated by amplifiers 1–3 as they load-pull one another.

To further evaluate the DPA, its performance was simulated over the frequency band 450–550 MHz, a ±10% range of frequencies. The phase delay of the TLs will vary by the same amount as the frequency is varied, but no changes were made to the DPA from when it was optimized at 500 MHz. Under these conditions, the DPA was able to achieve a good level of performance as shown in Fig. 8. Both the average efficiency over all on-states and the minimum and maximum V_{OUT} for the on-states are recorded. Performance degrades at 450 MHz, where a minimum V_{OUT} of 0.3 V was recorded, not for state 1, but state 4 with a resulting efficiency was only 0.2%. In state 4,

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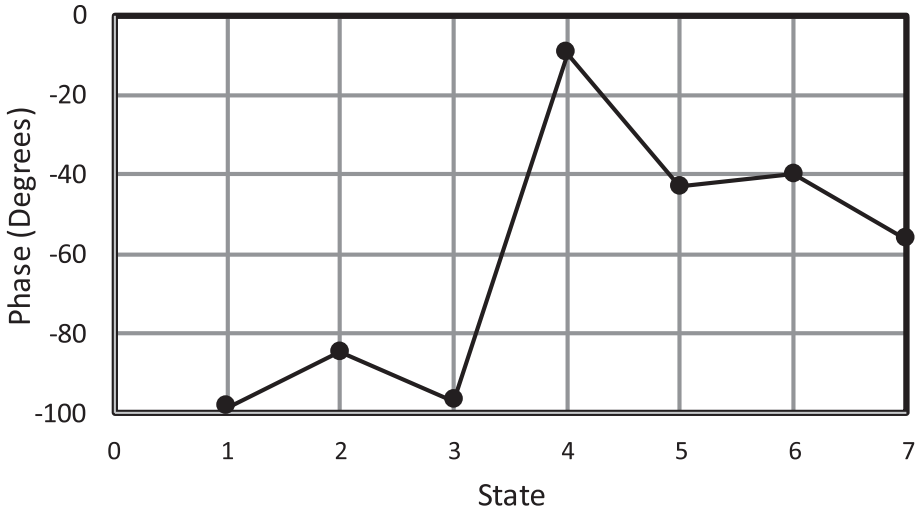


Fig. 7. Simulated phase response of DPA.

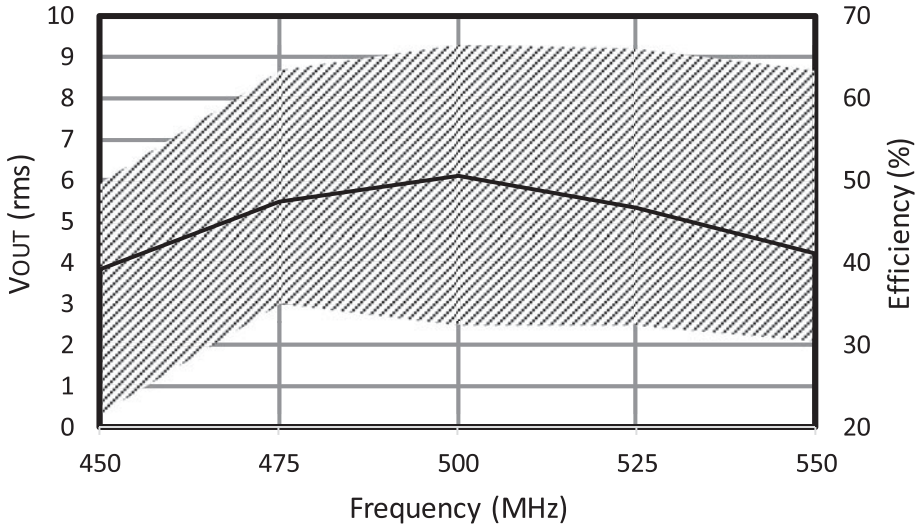


Fig. 8. Simulated frequency response, the hatched area is the minimum and maximum V_{OUT} and the black line the efficiency.

only the amplifier 1 is in use. This dramatic drop in performance was not due to the current from amplifier cancelling with another.

EM simulation of output network

During the design phase, it was found that some of the TLs had a larger impact on system performance than others. This led to the need for an EM simulation of the output network to ensure that the correct impedances were presented to the ports. The network shown in Fig. 6 was exported to MWO EMSight simulator as shown in Fig. 9.

The port *S*-parameter results from the EM simulation after tuning are shown in Fig. 10 where they are compared with the circuit-level simulation of Fig. 5. Simulations are only performed at three frequencies: fundamental (500 MHz), second harmonic (1 GHz), and third harmonic (1.5 GHz). The arrows indicate increasing simulation frequency from 500 MHz to 1.5 GHz. There is a good correlation between the circuit level and EM simulation.

Practical implementation

To further verify the operation, the prototype DPA was fabricated on an FR4 printed circuit board (PCB) substrate including the gate driver circuitry. A photograph of the fabricated DPA is shown below in Fig. 11. Due to the two loops of TL, amplifier 1 (port 1 in Fig. 4) was located in the middle of the PCB surrounded by one of the loops. Its RF input was mounted on the underside of the PCB; the cable connecting to it can be seen in Fig. 6 on the left side. The inputs to amplifiers 1–3 were attached to a three-way Wilkinson Power Splitter by a coaxial cable so that the delay between them can be adjusted with SMA adapters. The digital input is in the top left corner of the board. This was connected with jumpers to a set of dual-in-line package switches which could manually enable or disable amplifiers 1–3 for selecting the different states.

As stated in section "Parallel digital power amplifier", the devices are switched between their v_{th} and a strongly negative voltage to disable them. The gate driver circuitry translates standard 0 to +3.3 V logic levels to enable and disable voltage levels for the GaAs FETs. To achieve this, a Si8610BB digital isolator and MCP1402 MOSFET gate driver are used as shown in Fig. 12. The MCP1402 has a peak-to-peak output swing of 5 V. For the ATF-54143 driver, the output swings between 0.3 V, v_{th} of the ATF-54143, and −4.7 V to disable it. For the ATF-50189 v_{th} is 0.4 V, so the driver output swings between 0.4 and −4.6 V.

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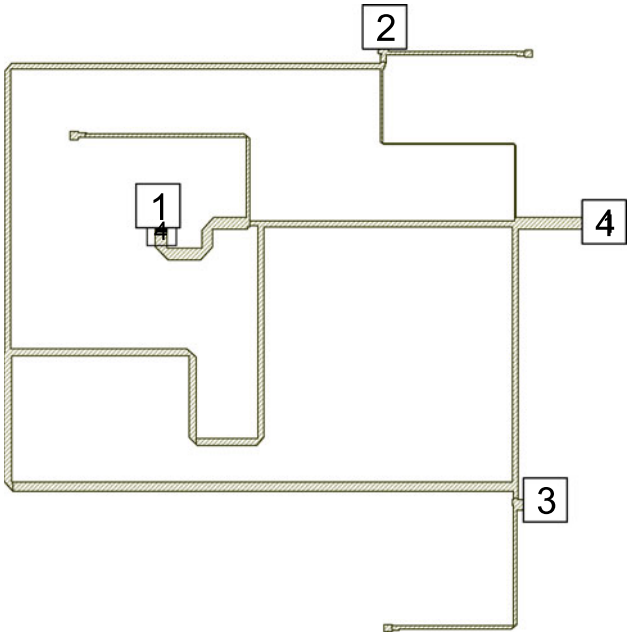


Fig. 9. EM model of output network of the DPA; port 1 connects to amplifier 1, port 2 to amplifier 2, port 3 to amplifier 3, and port 4 to the RF output.

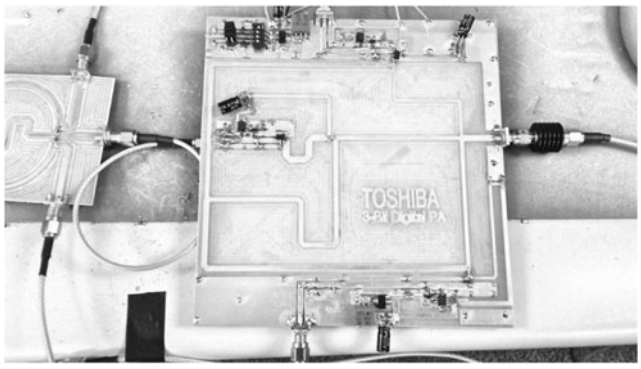


Fig. 11. Photograph of practical DPA.

Results

A Keysight N5172B EXG signal generator and Keysight N9010A EXA vector signal analyzer were used as a signal source and P_{OUT} monitor, respectively, for the measurements. A Minicircuits ZHL-1-2 W+ amplifier was also included to drive an equal three-way Wilkinson Splitter on the input. The measured results for V_{OUT} and the efficiency for each state are shown in Fig. 13. Seven unique on-states were achievable at ≥40% efficiency with a peak P_{OUT} of 28.9 dBm (780 mW) corresponding to a V_{OUT}

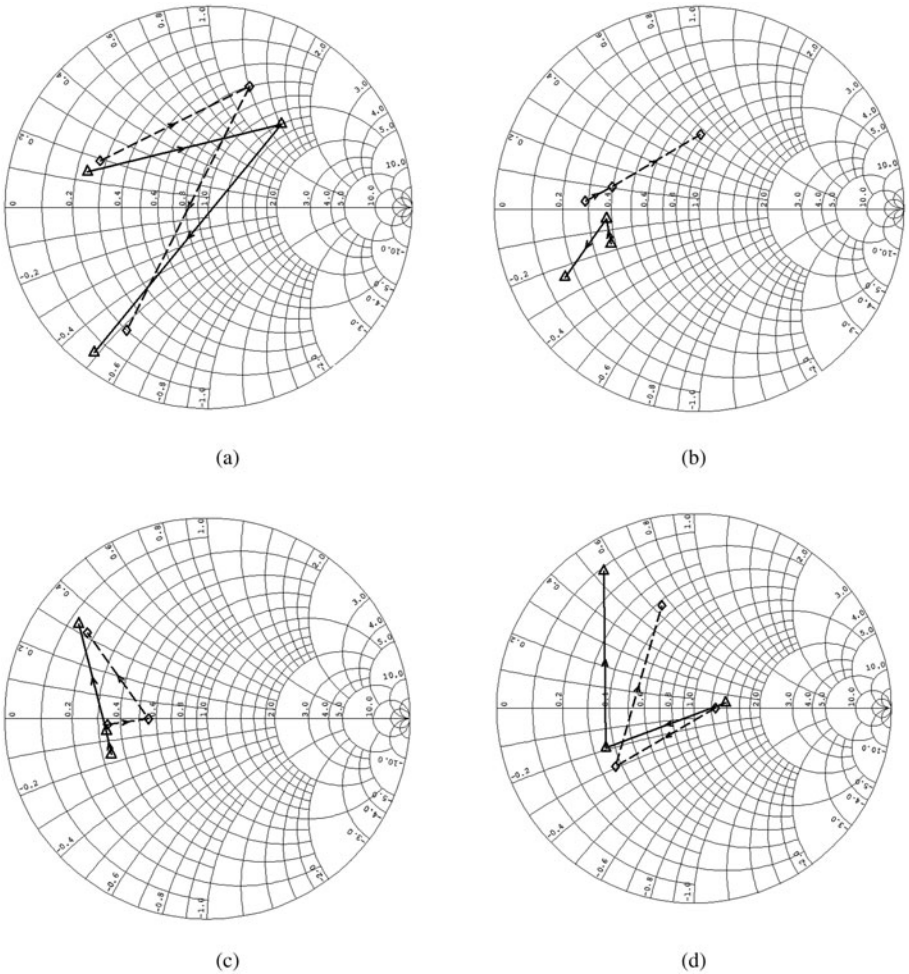


Fig. 10. Circuit (solid) and EM (dashed) simulations of the LT output network port impedances in a 50 Ω domain looking into ports for: (a) amplifier 1, (b) amplifier 2, (c) amplifier 3, and (d) RF output; arrows indicate increasing order of signal component: fundamental, second, and third harmonic zones.

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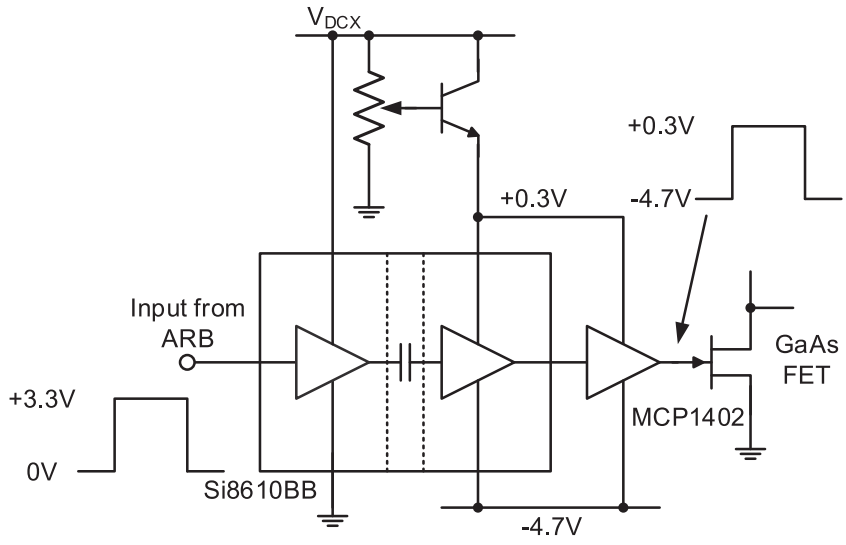


Fig. 12. Gate driver schematic for the ATF-54143.

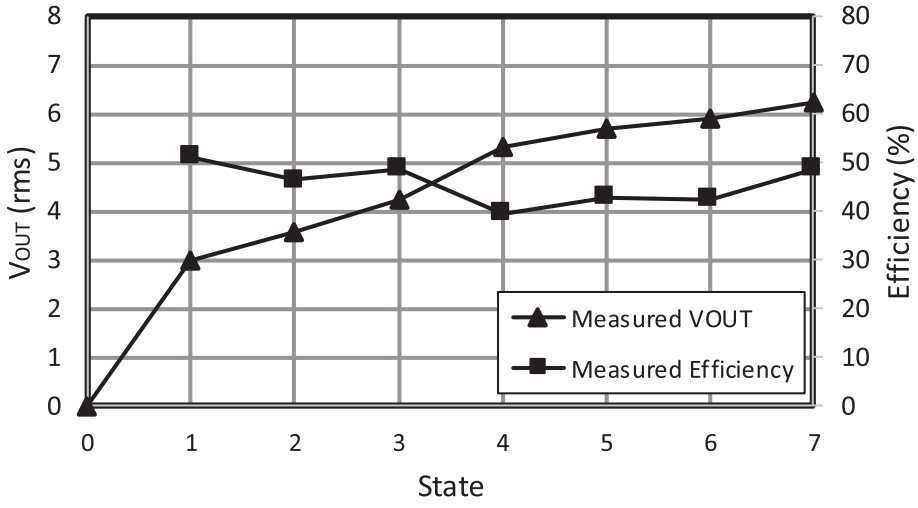


Fig. 13. Measured results.

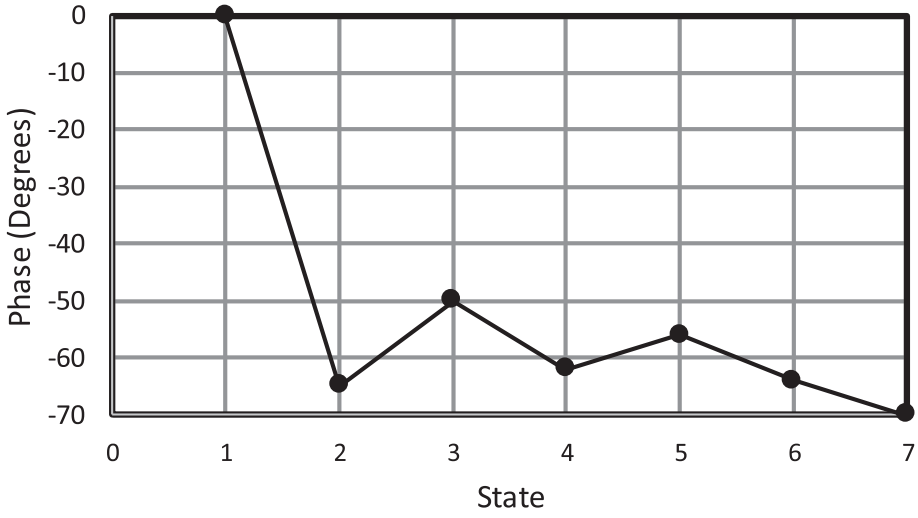


Fig. 14. Measured phase response.

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Table 2. Comparison of parallel DPAs ranked by peak P_{OUT}

Ref.	Frequency (GHz)	Peak P_{OUT} (dBm)	Peak η (%)	Backed-off η (%)	Technology
[17]	2.04	14.6	44	11 at 6.0 dB	9-bit CMOS
[18]	20–32	19.9	10 (PAE)	N/A	2 × 6-bit CMOS
[16]	1.5	20.3	46 (PAE)	50 (PAE) at 6.3 dB	1.6-bit GaAs
[8]	0.8	23.5	43 (PAE)	33 (PAE) at 6.0 dB	9-bit CMOS
[19]	2.4	28.8	31 (PAE)	22 (PAE) at 6.0 dB	2 × 9-bit CMOS
This work	**0.5**	**28.9**	**49**	**51 at 6.4 dB**	**3-bit GaAs**
[13]	2.25	29.1	42	20 at 6.0 dB	2 × 5-bit CMOS
[6]	2.3	32.1	62	22[a]	15-bit CMOS
[14]	7.0	33.4	39 (PAE)	15 (PAE)	3-bit GaN
[15]	3.5	35.2	40	NA	1-bit GaN

[a]Estimated from available information.

of 6.2 V_{rms}. Although V_{OUT} does not have the desired linear step size, it does have a positive trajectory. Input signal drive to the Wilkinson Splitter was 13 dBm under all states. The Splitter and cable loss when measured was approximately 5 dB, resulting in 8 dBm at amplifiers 1–3 input.

The measured phase response is shown in Fig. 14, where it can be seen to be relatively flat across states 2–7. This is different from the response shown in Fig. 7. The variation in the response is due to the summation and cancellation between the three amplifiers as they enter compression at different input powers, the amplifier whose output current dominates will dominate the phase response. The phase response can be compensated for either by the constellation diagram mapping or DPD as discussed in section "Simulated digital power amplifier results".

The minimum V_{OUT} at state 1 was 3.0 V_{rms}, representing a dynamic range of 6.4 dB. This state achieved the highest efficiency of 51%. The discrepancies between simulation and measurement were like due to limitations of the GaAs FET models and the port impedance discrepancies of the output network noted in Fig. 8. The performance achieved is compared to similar published architectures as shown in Table 2 where it performs favorably. References [6], [13], [14], and [15] achieved a higher peak P_{OUT}, but backed-off efficiency (η) was significantly lower. Back-off efficiency is more of a useful metric when modulated signals are used. This was even for the case of the two GaN MMIC implementations [14, 15], although these were operating at significantly higher frequencies. Comparing this work to the GaAs implementation of [16], there does not appear to be a significant impact by operating frequency on efficiency.

Conclusion

This paper describes a new parallel DPA architecture using discrete devices whose outputs are connected together with TL network inspired by a Rat-Race combiner. A 3-bit prototype was developed with a GA used to optimize the TL network. The simulation model achieved a peak P_{OUT} of 29.7 dBm with all seven on-states at ≥50% efficiency overall states. The practical demonstrator had a peak P_{OUT} of peak power of 28.9 dBm with on-state efficiencies ≥40%. This work represents the first discrete device DPA know to the author which makes it scalable to higher P_{OUT}, and therefore realizing applications like base-stations and digital TV broadcast transmitters with DPAs becomes a reality.

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