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Analysis of load mismatch effect compensation in Doherty power amplifier

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Research Paper

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Abstract

This paper presents a theoretical and experimental analysis of the capabilities of the dual-input Doherty power amplifier (DPA) architecture to mitigate efficiency and output power degradations when used in a mismatched load environment. Following a simplified linear piecewise approach, an analytical demonstration is proposed to derive optimal radio frequency drives applied to the Auxiliary path of the DPA to restore power performances while avoiding large signal voltage clipping of active cells. The proposed analytical study is corroborated with harmonic balance simulated results of a C-band, 20-W GaN DPA prototype. The fabricated dual-input DPA prototype has been measured under 1.5-VSWR mismatch configurations to validate the proposed analysis.

Introduction

Doherty Power Amplifier (DPA) has been now widely accepted as an off-the-shelf radio-frequency power amplifier (RFPA) solution to improve the energy efficiency of 3 G–4 G base stations and is on track to lead the competition in future 5 G transmitters [1]. Although it suffers from inherent limitations, mainly due to the frequency selective output combining circuit, several works have highlighted the DPA capabilities to accommodate a typical 20% fractional bandwidth [2–4], while advanced DPA structures have been demonstrated to operate over fractional bandwidth up to 80% [5], at a cost of a reduced load modulation effect, introducing the so-called Doherty-lite topology.

When implemented with a conventional analog input radio frequency (RF) splitter, the DPA AB-C topology suffers from several degradations, among which:

(i) Gain roll-off between low and high power regions, due to the deep class-C transistor operation of the auxiliary amplifier
(ii) Output power and efficiency discrepancy due to dispersive AM-PM and AM-AM conversions of transistors that combine their currents out-of-phase in a frequency-selective load.

Taking advantage of the low power, commercially available dedicated circuits (e.g. ASICs, DSP), the digital version of the DPA has been introduced and is now viewed as a potential competitive embodiment for future DPA [6–9]. In related implementations, the fixed input RF splitting circuit is advantageously replaced by a fully reconfigurable power-dependent RF distribution between Main and Auxiliary cells of the DPA. Doing so, this enables to optimize the beneficial load–pull interaction between power cells, and maximize linearity/efficiency DPA performances.

At the system designer level, (Massive) MIMO access techniques are widely envisaged as a potential breakthrough to mitigate harsh microwave/millimeter wave propagating conditions and to improve the capacity of future 5 G integrated RF systems. Because of high integration, the flip side is that severe constraints are reported on analog microwave front-end elements, leading to e.g. higher levels of coupling and a higher level of power density to dissipate. Highly integrated millimeter-wave active antenna (e.g. active electronically scanned array (AESA), for radar or communication applications), is of typical interest to exemplify this point. By suppressing the lossy and bulky isolators between RFPAs and radiating ports, RFPAs are subjected to significant voltage standing wave ratio (VSWR) values, degrading the overall linearity and efficiency performances [10–12].

This paper presents some theoretical backgrounds giving insight into the conventional DPA behavior when used in a realistic mismatched load environment. It is described how DPA power performances can be partially recovered by monitoring the magnitude and phase of the RF signal at the auxiliary path input. The paper is organized as follows. The section Theoretical assumptions presents the theoretical assumptions made on the active devices that will be used in the DPA structure. In the section DPA theoretical performances analysis

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under matched-load configuration, DPA performances are derived in a conventional 50-Ω system impedance reference. The section Dual-input DPA theoretical behavior under mismatched load highlights the degradations that occur when the output load impedance is pulled-away from its nominal value and shows how the DPA architecture is theoretically able to mitigate these degradations. The section Dual-input DPA prototype simulation presents a C-band, 20W GaN DPA prototype including dual-input capabilities, and simulated harmonic balance (HB) performances are discussed. Finally, measurement results of the fabricated prototype are presented in the section Dual-input DPA prototype measurement and validate the proposed study.

Theoretical assumptions

Transistor model used for the proposed analytical study is considered as a piecewise linear transconductive current source. The knee voltage (V_k) is neglected and the biasing voltage (V_{DD}) is chosen so that the avalanche phenomenon is avoided. No reactive part is considered (e.g. package effect and extrinsic device parasitics). This very simple model gives sufficient insight into the DPA behavior, provided that large-signal voltage clipping is avoided. The I-V characteristic is represented in Fig. 1. The maximum current of the device I_{max} is considered to be 1 Amp. The maximum sustainable drain-source voltage V_{max} is 80 V. These values are typical for a 6W, 1 mm-periphery GaN HEMT power device.

Considering class-B operation, transistor is sinking fundamental current I_{fund} and DC current I_{DC} that is given in (1), wherein the a coefficient is the normalized RF drive amplitude. We assume that harmonics of current are properly shorted.

$$\begin{aligned} I_{DC} &= \frac{I_{max}}{\pi} a \quad 0 \le a \le 1 \\ I_{fund} &= \frac{I_{max}}{2} a \end{aligned} . \tag{1}$$

Device's maximum active power is obtained at full current and voltage RF swings and is given in (2), where V_{DD} is the drain-to-source bias voltage of the device.

$$P_{main} = \frac{1}{4} I_{max} V_{DD}. \tag{2}$$

The associated optimum loading resistor R_{opt} is defined by:

$$R_{opt} = 2\frac{V_{DD}}{I_{max}}. \tag{3}$$

DPA theoretical performances analysis under matched-load configuration

The DPA architecture is presented in Fig. 2. Based on theoretical assumptions, previous Main and Auxiliary devices are directly implemented through current sources injecting fundamental currents I_{main} and I_{aux}. These currents are combined through a lossless output RF circuit, namely a $\lambda/4$ and a $\lambda/2$ composite transmission lines, in which the reactive parasitics of the transistors are absorbed, and a common (real) load R_c, defined as:

$$R_c = \frac{R_{opt}}{(1+n)}. \tag{4}$$

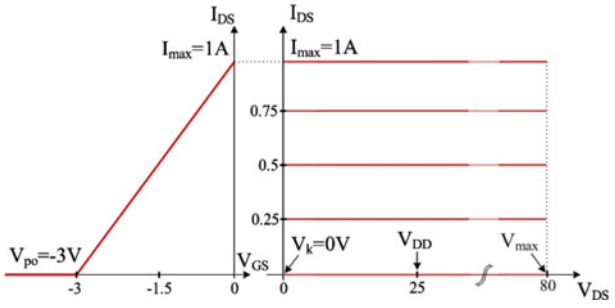


Fig. 1. Simplified I-V characteristic of transistor.

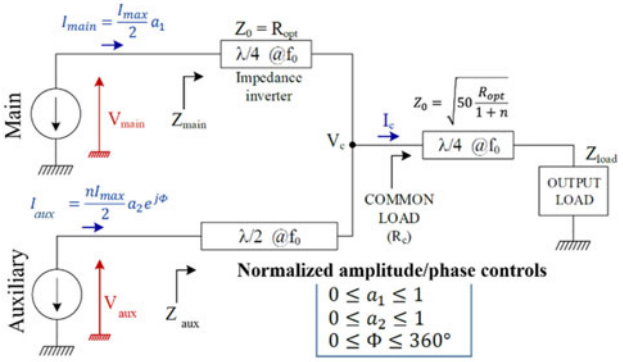


Fig. 2. Doherty power amplifier (DPA) topology.

This constitutes an inverted Doherty amplifier topology. The n factor is introduced to account for generalization in the DPA structure, in which the Auxiliary device could be n times larger than the Main one. This enables larger modulation ratios and thus larger OBO peak-efficiency operation for the DPA. Throughout this paper, I_{main} is considered as the phase reference, and is real. The phase offset Φ is thus defined as:

$$\Phi = \arg(I_{aux}) - \arg(I_{main}) = \arg(I_{aux}). \tag{5}$$

Using ABCD matrixes of $\lambda/4$ and $\lambda/2$ transmission lines, one can derive (6) that indicates that the output common node voltage V_c (i) is solely a function of the Main fundamental current I_{main} and the characteristic impedance Z_0, and (ii) is phase-inverted and copied at the intrinsic Auxiliary drain.

$$V_c = -jZ_0 I_{main} = -V_{aux}. \tag{6}$$

Thus, the intrinsic impedance presented to the Auxiliary device is not affected by any load mismatch that appears at the common node. From this simple ascertainment, it is of particular interest to evaluate the ability of the DPA structure to accommodate with output load mismatch by controlling the amplitude and phase of I_{aux}.

First, we suppose there is no load mismatch ($Z_{load} = 50\ \Omega$). The relationships between fundamental voltages and currents are derived from the ABCD-matrixes of the quarter-wave inverter, the $\lambda/2$ transmission line and the common load R_c, giving:

$$\begin{pmatrix} V_{main} \\ I_{main} \end{pmatrix} = \begin{pmatrix} -j(1+n) & -jR_{opt} \\ \dfrac{-j}{R_{opt}} & 0 \end{pmatrix} \begin{pmatrix} V_{aux} \\ -I_{aux} \end{pmatrix}. \tag{7}$$

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The active powers of the Main and Auxiliary devices are given in (8), in which a_1, a_2 represent the normalized amplitude controls and Φ represents the phase control of the two devices, as defined in Fig. 2 :

$$\begin{aligned} P_{main} &= \frac{1}{2} real(V_{main} I^*_{main}) \\ &= \frac{1}{8} a_1^2 R_{opt} (1+n) I^2_{max} \\ &\quad - \frac{1}{8} n R_{opt} I^2_{max} a_1 \; a_2 \sin(\Phi). \\ P_{peak} &= \frac{1}{2} real(V_{aux} I^*_{aux}) \\ &= \frac{1}{8} n R_{opt} I^2_{max} a_1 \; a_2 \sin(\Phi) \end{aligned} \tag{8}$$

Provided that the output combiner is lossless, these powers sum up to give the total active power transferred to Z_{load}:

$$P_{load} = P_{main} + P_{aux}. \tag{9}$$

The global DPA efficiency is thus given by:

$$Eff(a_1, a_2)(\%) = \frac{P_{main} + P_{aux}}{P_{DCmain} + P_{DCaux}} = \frac{\pi}{4} \frac{(1+n) a_1^2}{a_1 + n a_2}. \tag{10}$$

The efficiency function is plotted in Fig. 3 for different a_2 values and for $n = 1$ (symmetrical DPA).

To calculate the maximum achievable efficiency of the DPA, constraints must be added to account for the physical limitations of the devices, namely:

$$\begin{cases} max(|V_{main}|, |V_{aux}|) \le V_{DD} \\ 0 \le I_{main} \le \dfrac{I_{max}}{2} \\ 0 \le I_{aux} \le \dfrac{n I_{max}}{2} \end{cases}$$

Main and Auxiliary voltages are given by :

$$\begin{aligned} V_{main} &= V_{DD}((1+n)a_1 + jna_2 e^{j\Phi}) \\ V_{aux} &= jV_{DD} a_1 \end{aligned}. \tag{11}$$

The Fresnel representation of voltages (normalized to V_{DD}) $\overline{V_{main}}$ and $\overline{V_{aux}}$ is plotted in Fig. 4.

To ensure maximum efficiency operation within the $0 \le a_1 \le 1$ range, the auxiliary device remains off in the $0 \le a_1 \le a_{1th}$ range, with the threshold point defined as:

$$a_{1th} = \frac{1}{1+n}. \tag{12}$$

For $a_{1th} \le a_1 \le 1$, the auxiliary device comes into play to modulate the load impedance of the main transistor, producing a constant and purely real voltage V_{main} equal to V_{DD}. The corresponding value of a_2 to reach maximal efficiency is given by:

$$a_2 e^{j\Phi} = j \frac{1}{n} (a_1(1+n) - 1), \tag{13}$$

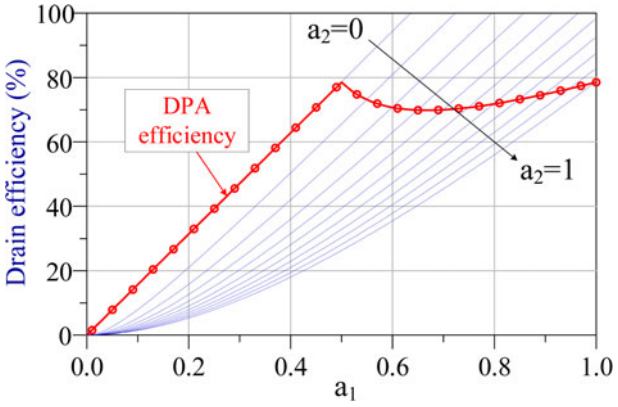


Fig. 3. DPA efficiency curves (dot – blue) calculated according to (10) ($n = 1$) and maximum realizable efficiency of the DPA (circle – red).

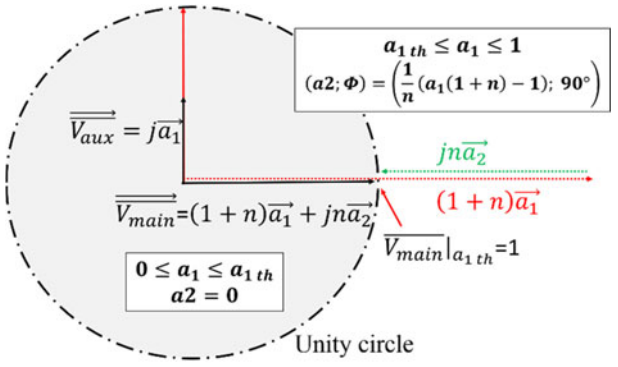


Fig. 4. Fresnel representation of fundamental voltages in DPA architecture (from (11)).

which can be written in polar form as:

$$(a_2; \Phi) = \left(\frac{1}{n} (a_1(1+n) - 1); 90^\circ \right). \tag{14}$$

Current, voltage, and load impedance variations versus a_1 are represented in Fig. 5, with $n = 1$. This corresponds to the well-known ideal symmetrical DPA operation.

Dual-input DPA theoretical behavior under mismatched load

Load impedance variations at intrinsic planes

We will extend the previous analysis to the case of mismatched load impedance. Z_{load} is now modified such that $Z_{load} = 50\ \zeta_{load}$ [Ω]; with $\zeta_{load} = (r + jx)$ being the normalized mismatched load impedance. Four typical cases will be studied, namely:

$$\begin{aligned} Z_{re+} &= 50(1,\ 5 + jO)[\Omega] \\ Z_{re-} &= 50(0,\ 667 + jO)[\Omega] \\ Z_{im+} &= 50(1 + jO,\ 408)[\Omega] \\ Z_{im-} &= 50(1 - jO,\ 408)[\Omega] \end{aligned}. \tag{15}$$

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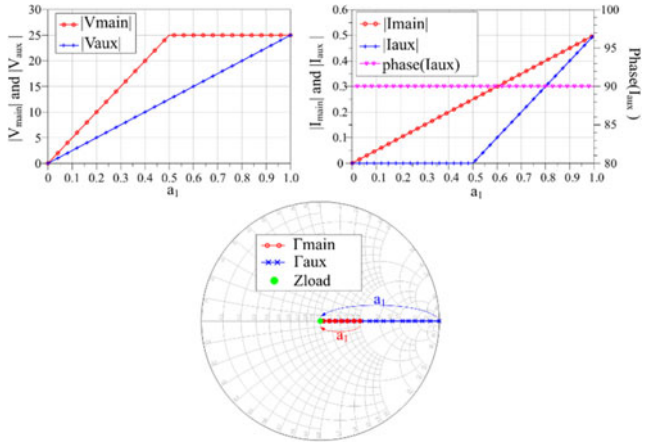


Fig. 5. Fundamental voltage, current and impedance variations versus a_1 in ideal DPA operation.

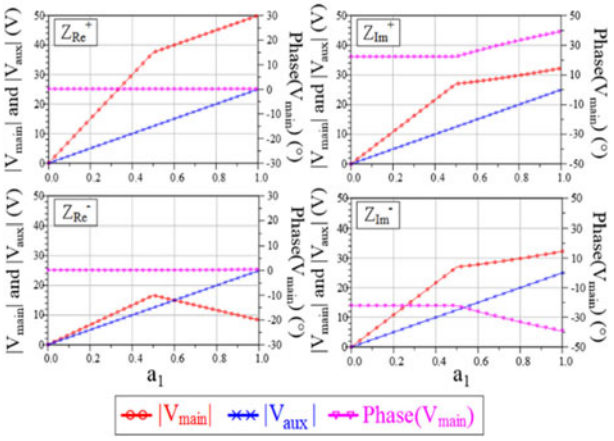


Fig. 7. V_{main} and V_{aux} variations versus a_1 in mismatched load configuration.

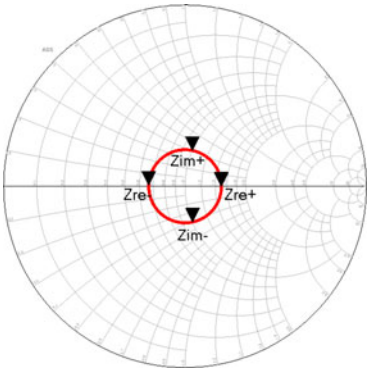


Fig. 6. Studied Z_{load} (constant 1.5-VSWR) in DPA realistic mismatched configuration.

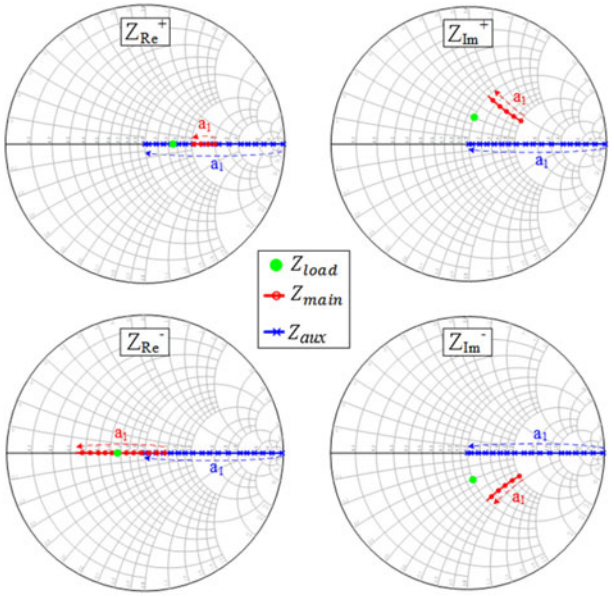


Fig. 8. Impedance trajectories at intrinsic planes of Main and Auxiliary devices; the Main impedance is modulated from $(1+n)\zeta_{load}R_{opt}$ (back-off operation) to $(1+n)\zeta_{load}R_{opt} - nR_{opt}$ (saturated power condition), Auxiliary impedance is modulated from Open Circuit (O.C) to R_{opt}/n.

These load impedances are located in a constant 1.5-VSWR locus, as illustrated in Fig. 6, and correspond to a mismatched environment that can occur in AESA applications.

The relationship between voltages and currents is given by

$$\begin{pmatrix} V_{main} \\ I_{main} \end{pmatrix} = \begin{pmatrix} -j(1+n)\zeta_{load} & -jR_{opt} \\ \dfrac{-j}{R_{opt}} & 0 \end{pmatrix} \begin{pmatrix} V_{aux} \\ -I_{aux} \end{pmatrix}, \quad (16)$$

V_{main} and V_{aux} are plotted in Fig. 7, along with associated load impedance variations in Fig. 8, for the four mismatched load conditions, and for the same optimum drives as derived in the 50-Ω nominal case. For the sake of clarity, arg(V_{aux}) is not reported, because it remains in quadrature with a_1, and is not altered by the mismatch effect, as described in the section Theoretical assumptions.

$$\begin{aligned} V_{main} &= V_{DD}(a_1(1+n)\zeta_{load} + jn\, a_2 e^{j\Phi}) \\ V_{aux} &= jV_{DD}a_1 \end{aligned}. \quad (17)$$

When the 50 ohms matched-configuration optimum RF drives are maintained (e.g. because of a fixed splitting configuration), efficiency and linearity performances of the DPA are strongly affected.

When a resistive load-pull occurs ($Z_{load} = Z_{re+}$), V_{main} can reach higher values than V_{DD}, potentially strongly affecting the linearity of a real-life DPA and even causing reliability issues to the Main device. When $Z_{load} = Z_{re-}$, V_{main} is always lower than V_{DD}, reducing the net active power delivered to the load, and impacting the overall efficiency of the DPA.

When a reactive load-pull effect occurs ($Z_{load} = Z_{im-}$ or Z_{im+}), V_{main} is no longer in phase with I_{main}, and has magnitude higher than V_{DD} above the threshold point a_{1th}, both contributing to produce a constant net active main power, and thus do not impact the global efficiency of the DPA. The active powers

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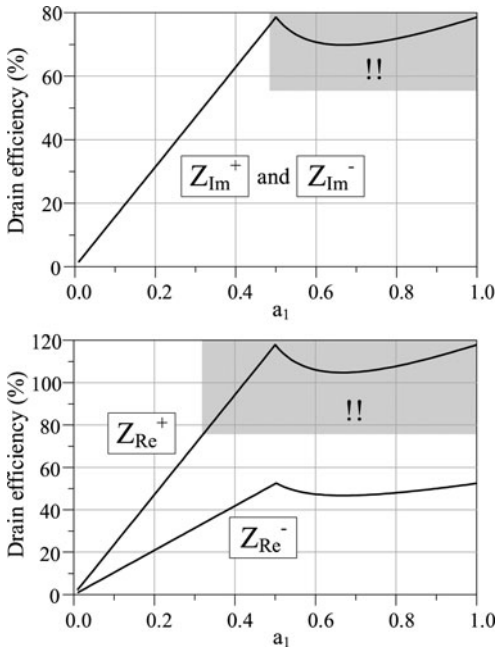


Fig. 9. Drain efficiency performances of the DPA when load-pull occurs at the output plane; !! annotation means that electrical constraints are not satisfied (e.g. $|V_{main}| > V_{DD}$).

injected by the Main and Auxiliary devices are given by:

$$\begin{aligned} P_{main} &= \frac{1}{2} real(V_{main} I_{main}^{*}) \\ &= \frac{1}{8} a_1^2 R_{opt} (1+n) a I_{max}^2 \\ &\quad - \frac{1}{8} n R_{opt} I_{max}^2 a_1 \; a_2 \sin(\Phi). \\ P_{aux} &= \frac{1}{2} real(V_{aux} I_{aux}^{*}) \\ &= \frac{1}{8} n R_{opt} I_{max}^2 a_1 \; a_2 \sin(\Phi) \end{aligned} \tag{18}$$

The active powers delivered by both transistors sum up to give the active power transferred to the load, which is independent of the Φ value and is a function of the real part of the mismatched normalized load impedance. The resulting efficiency function is given in (19) and is plotted in Fig. 9.

$$Eff(a_1, a_2)\ (\%) = \frac{P_{main} + P_{aux}}{P_{DCmain} + P_{DCaux}} = \frac{\pi}{4} \frac{(1+n) a_1^2}{a_1 + n a_2}\ r. \tag{19}$$

DPA performances with optimal-efficiency RF drives

The new maximum-efficiency driving conditions are sketched in the Fresnel representation of the voltage vectors V_{main} and V_{aux}. As it can be seen in Fig. 10, they are dependent on the load-pull presented at the output of the DPA structure. Again, to ensure maximum-efficiency operation, the auxiliary transistor is off in the $0 \le a_1 \le a_{1th}$ range, with:

$$a_{1th} = \frac{1}{(1+n)|\zeta_{load}|}. \tag{20}$$

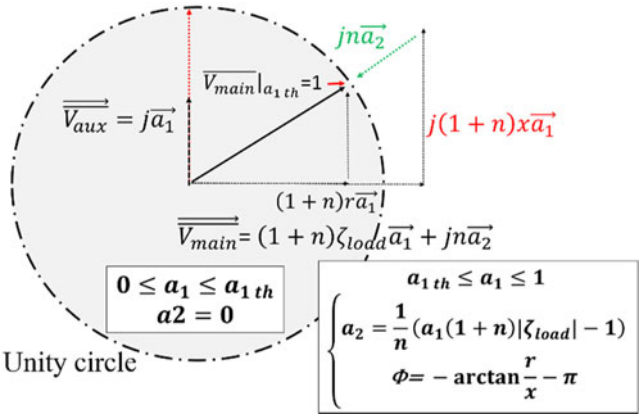


Fig. 10. Fresnel representation of the fundamental voltages V_{main} and V_{aux} for load mismatch conditions.

For $a_1 = a_{1th}$, the produced complex main voltage is:

$$V_{main_th} = V_{DD} \frac{\zeta_{load}}{|\zeta_{load}|}. \tag{21}$$

In the $a_{1_th} \le a_1 \le 1$ range, the auxiliary device comes into play to modulate the complex impedance presented to the main transistor, producing an out-of-phase drain-to-source voltage with a constant V_{DD} magnitude. The corresponding optimal efficiency drive is thus given by:

$$a_2 e^{j\Phi} = j \frac{1}{n} \zeta_{load} \left(a_1 (1+n) - \frac{1}{|\zeta_{load}|} \right), \tag{22}$$

which can be written in polar form as:

$$\begin{aligned} |a_2| &= \frac{1}{n} (a_1 (1+n) |\zeta_{load}| - 1) \\ \Phi &= -\arctan\left(\frac{r}{x}\right) - \pi \end{aligned}. \tag{23}$$

It can be inferred that when load-pull occurs such that $|\zeta_{load}| > 1$, the optimum drive implies $|a_2| > 1$ at full RF power in order to maintain the $|V_{main}| = V_{DD}$ condition. For this purpose, a larger auxiliary device should be used, even in a symmetrical DPA topology. The DPA optimum RF drives associated with the four impedance configurations are represented in Fig. 11. As shown in Fig. 12, associated optimal impedance loci move along constant Q trajectories, depending on the load mismatch (with $Q = x/r$).

When optimum RF drives a_1, a_2, and Φ are applied, maximum efficiency is recovered, taking into account the physical constraints of sustainable voltages V_{main} and V_{aux}. The optimal efficiency function is represented in Fig. 13 for the four cases of interest. The ratio κ_{Eff} between the efficiency for 50 Ω load ($\zeta_{load} = 1$)) and the efficiency for the mismatched load ($\zeta_{load} \ne 1$) with optimal RF drives at $a_1 = a_{1th}$ (at turn-on point) is:

$$\kappa_{Eff} = \frac{Eff_{\zeta_{load} \ne 1,\ with\ opt\ drives}}{Eff_{\zeta_{load}=1}} = \frac{r}{|\zeta_{load}|}. \tag{24}$$

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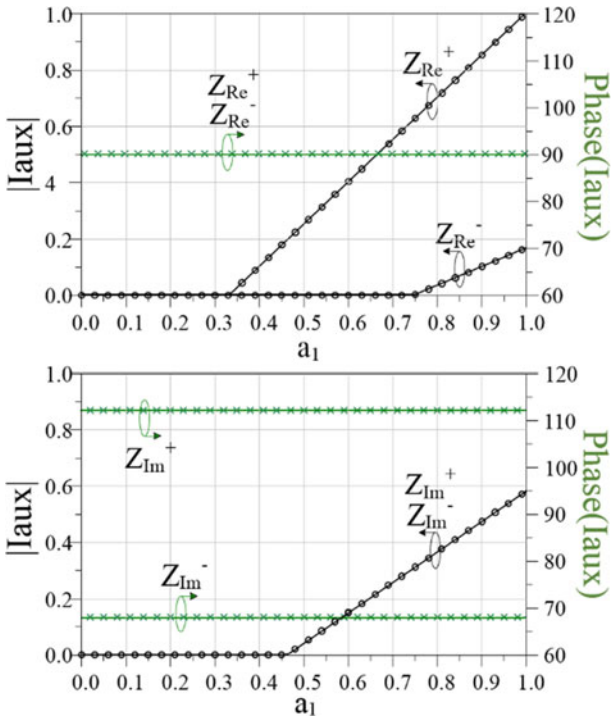


Fig. 11. RF drives for optimal efficiency of DPA ($n = 1$) for the studied mismatched loads.

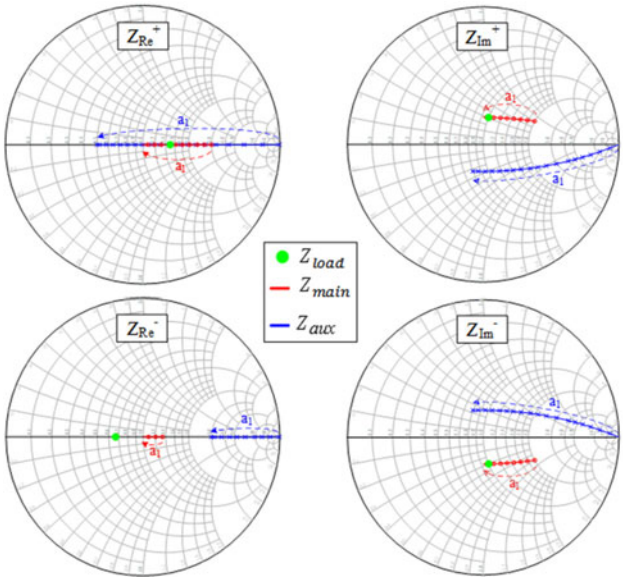


Fig. 12. Impedance trajectories when optimal RF driving conditions for maximum efficiency are applied (illustrated here for $n = 1$): Main impedance is modulated from $(1 + n)\,\zeta_{load}R_{opt}$ (back-off operation) to $R_{opt}\ \zeta_{load}/|\zeta_{load}|$(saturated power condition), Aux. impedance is modulated from Open Circuit (O.C) to $R_{opt}/\zeta_{load}(1 + n - 1/|\zeta_{load}|)$.

The corresponding auxiliary turn-on point shift is:

$$\kappa_{a_{1th}} = \frac{a_{1th}\zeta_{load} \neq 1,\ with\ opt\ drives}{a_{1th}\zeta_{load} = 1} = \frac{1}{|\zeta_{load}|}. \qquad (25)$$

These quantities are synthesized in Table 1. Non-physical results (e.g. when associated electrical constraints are not satisfied) are annotated with !!. For example, from Table 1 it is not possible to ensure the same maximum DPA efficiency of 78.5% when resistive load-pull occurs, with a shift of the turn-on point. On the contrary, it is not possible to maintain maximum efficiency performances while fulfilling the device's constraints when reactive output load-pull exists.

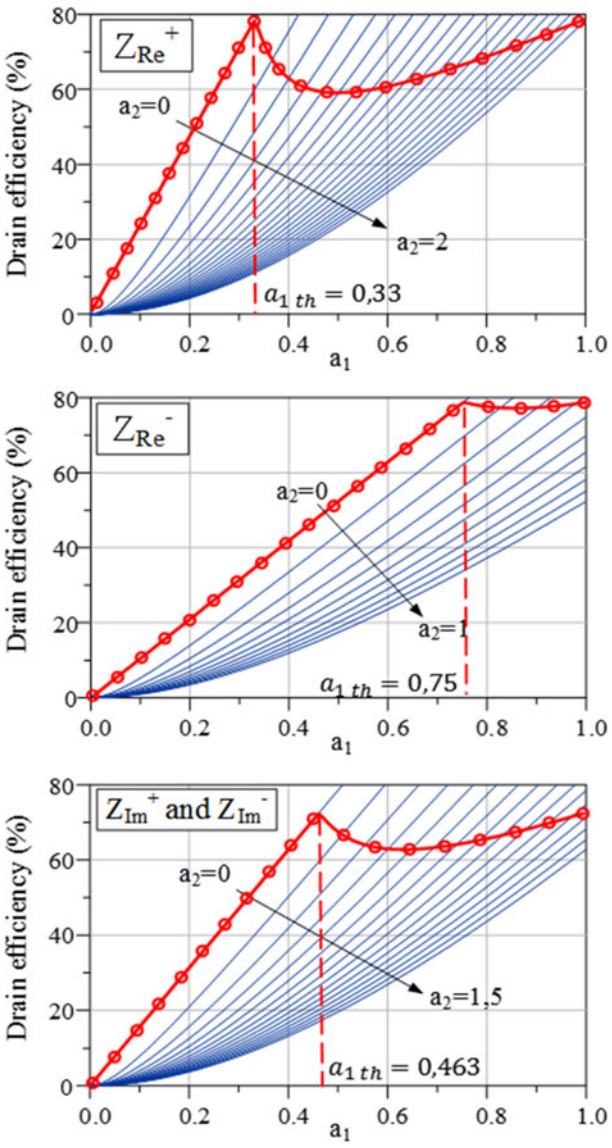


Fig. 13. DPA efficiency performances when optimal RF drives are applied for the studied mismatched load.

Dual-input DPA prototype simulation

DPA prototype performances under matched-load configuration

A 20 W, C-band, dual-input symmetrical DPA prototype has been built to validate the proposed theoretical study. Commercially available Wolfspeed GaN HEMT packaged components [13] and nonlinear transistor model have been used in HB simulation in Keysight ADS CAD environment. The layout of the final prototype is presented in Fig. 14.

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Table 1. DPA performances with and without optimal drives in mismatched environment. (!!) is put when circuit constraints are not satisfied.

	Fixed input splitter configuration		Dual-input distribution with optimal RF drives	
	$\kappa_{a_{1\,th}}(dB)$	κ_{Eff}	$\kappa_{a_{1\,th}}(dB)$	κ_{Eff}
Reference case: $Z_{load} = 50\Omega$	$\triangleq 0$	$\triangleq 1$	0	1
$Z_{load} = 50\zeta_{load}\Omega$	0	r	$-20\log(\lvert\zeta_{load}\rvert)$	$\frac{r}{\lvert\zeta_{load}\rvert}$
$Z_{load} = Z_{re+}\ \Omega$; $n = 1$	0	1.5 (!!)	−3.52	1
$Z_{load} = Z_{re-}\ \Omega$; $n = 1$	0	0.667	3.52	1
$Z_{load} = Z_{im+}\ \Omega$; $n = 1$	0	1 (!!)	−0.67	0.925
$Z_{load} = Z_{im-}\ \Omega$; $n = 1$	0	1 (!!)	−0.67	0.925

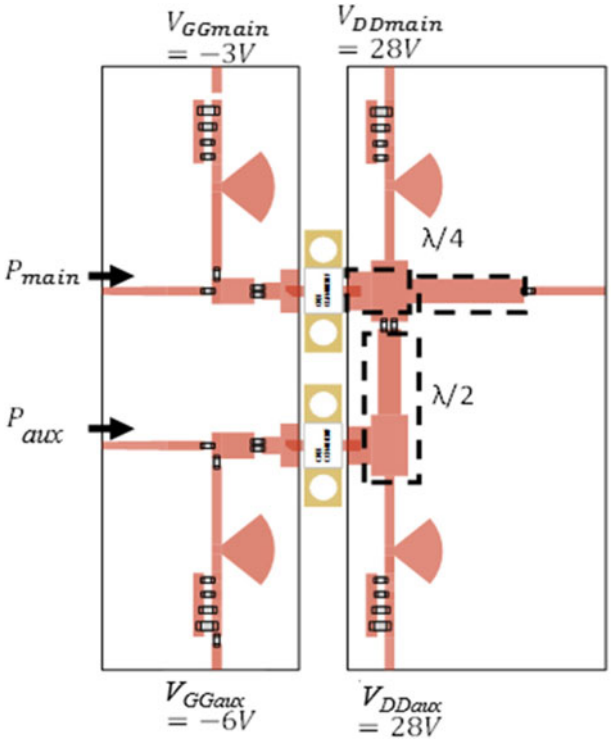


Fig. 14. Layout of the symmetrical dual-input GaN DPA prototype.

An optimum intrinsic load R_{opt} of 34 Ω at 41 dBm output power has been determined. Large-signal simulated performances of the DPA are presented in Fig. 15, at a center frequency of 3.9 GHz. Main and Auxiliary gate to source bias voltages has been adjusted to ensure the correct DPA behavior in nominal 50 Ω loading condition ($V_{GGmain} = -3V$ and $V_{GGaux} = -6V$).

We define the power and phase RF imbalances between Auxiliary and Main devices as ΔP and $\Delta\Phi$, respectively, as:

$$\begin{aligned} \Delta P &= P_{aux} - P_{main} \\ \Delta\Phi &= \Phi_{aux} - \Phi_{main} \end{aligned} \quad (26)$$

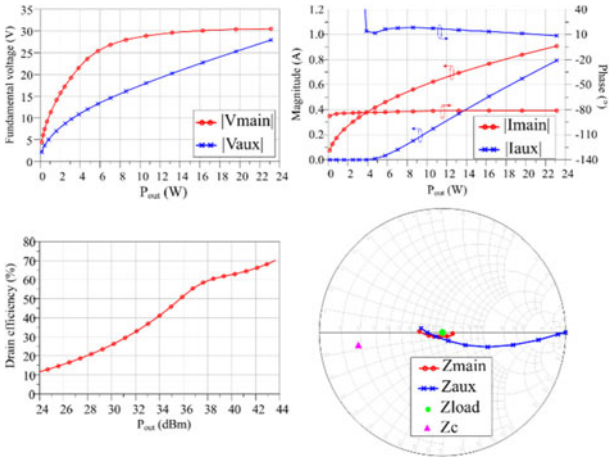


Fig. 15. DPA prototype simulation results at center frequency of 3.9 GHz in the nominal case ($Z_{load} = 50\Omega$).

In this case, optimum power and phase driving offsets ($\Delta P = 0dB$ and $\Delta\Phi = 80°$) are in good agreement with expected theoretical values in the section Dual-input DPA theoretical behavior under mismatched load. In the following, current and voltage quantities at the fundamental frequency will be analyzed and all phases will be referenced to I_{Main}, resulting phasors are denoted with the N subscript.

Load modulation effect is clearly observed, as the intrinsic Main device impedance is modulated from 59 Ω to 34 Ω, following a real-to-real impedance locus. Meanwhile, intrinsic Auxiliary device impedance is modulated from open circuit condition to 34 Ω. It can be shown in Fig. 15 (top left) that the Main device is effectively kept saturated in the load-modulation region, giving back-off efficiency improvements as it can be seen in Fig. 15 (bottom left).

DPA prototype performances under output mismatch configuration

The same load mismatch conditions studied in the theoretical section have been applied to the prototype DPA. First, the static CW optimum matched-case splitting conditions ($\Delta P = 0dB$ and $\Delta\Phi = 80°$) are maintained. Associated modified load impedance variations are reported on Fig. 16, and are in good agreement with theoretical trends shown in the section Dual-input DPA theoretical behavior under mismatched load.

Associated intrinsic voltages and currents are plotted in Fig. 17, to illustrate how mismatch conditions can adversely affect the DPA behavior. As predicted in the theoretical section, it can be clearly confirmed in Figs 16 and 17 that, as the output impedance is shifted from low value to high value along the resistive part (i.e. for Z_{re-} and Z_{re+} loading conditions, respectively), the net fundamental voltage produced across the main transistor increases.

This could potentially induce reliability and linearity issues in the DPA structure. In our case, thanks to the inverse class-F operation employed in the proposed design the net value of the fundamental frequency component of the drain voltage can reach higher values than the theoretical limit of 28 V (i.e in the order of 34 V).

When a reactive load-pull effect occurs (i.e. for $Z_{load} = Z_{im-}$ or Z_{im+}), the Main device impedance is shifted along a constant

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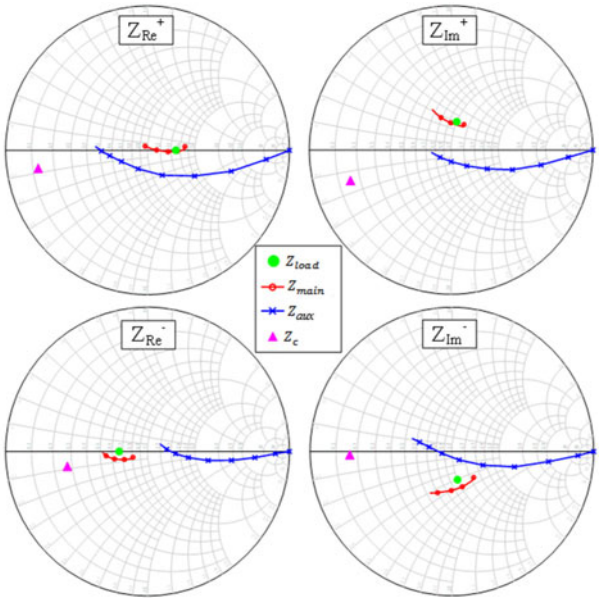


Fig. 16. Distorted intrinsic Main and Auxiliary impedances in mismatched load configuration.

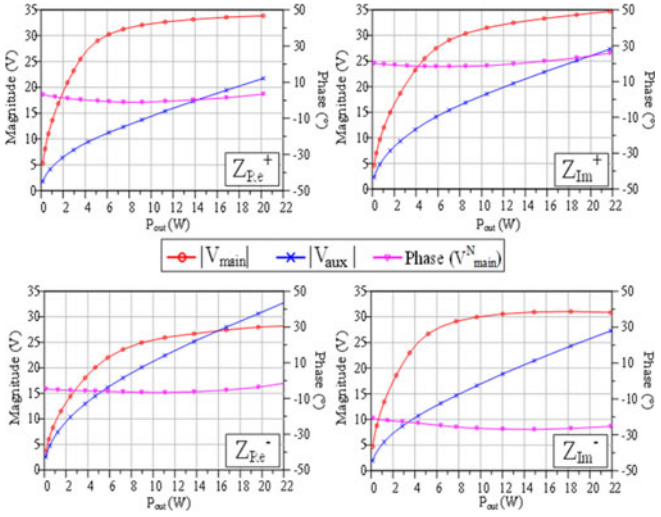


Fig. 17. Voltages produced across Main and Auxiliary devices. Reference 50 Ω case is plotted for comparison.

reactance locus, as theoretically predicted in Fig. 8. In this case, V_{main} is no longer in phase with I_{main}. Its phase depends on the RF drive level, while its magnitude is always higher than its nominal $V_{DD} - V_k$ value in the load-modulation range, causing linearity and reliability issues in the DPA structure. Drain efficiency profiles are plotted in Fig. 18 for the four tested impedances. It is verified that, in this typical case, DPA efficiency is strongly impacted in the case of a resistive load pull, and is only slightly dependent on a reactive load pull.

Optimum input splitting parameters ΔP and $\Delta\Phi$ have then been applied to mitigate efficiency power performance decrease. ΔP and $\Delta\Phi$ are derived according to the procedure described in the section Dual-input DPA theoretical behavior under mismatched load, so that:

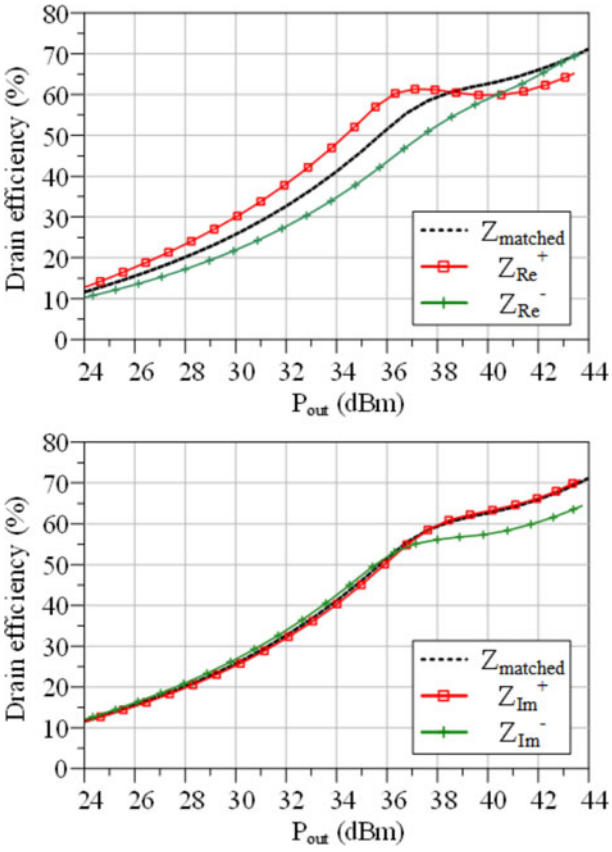


Fig. 18. DPA simulated PAE performances for mismatched load impedances.

- Fundamental voltage produced across intrinsic Main device is restricted by the $V_{DD} - V_k = 30$ V, defined as a target value, so as to ensure optimum safe saturated conditions of devices
- Associated impedance Z_{Main} is modulated along a constant Q trajectory. Q is defined according to the output load mismatch, as x/r.

Optimum Main and Auxiliary currents and intrinsic load impedances are plotted in Figs 19 and 20. They are consistent with theoretical profiles, as it is confirmed that:

(i) A resistive load-pull (Figs 19 and 20, top and bottom left), implies an Auxiliary device turn-on point shift and a maximum available current quantity modification, with no modification on the phase
(ii) A reactive load-pull (Figs 19 and 20, top and bottom right) implies only a phase shift.

It is worth noting that, to ensure a constant Q value, $\Delta\Phi$ has to be slightly modified versus the RF level, which is not predicted in the theoretical section. This is mainly to compensate for the difference of nonlinear AM-to-PM conversions of the devices.

Associated voltages produced across the Main and Auxiliary devices are plotted in Fig. 21. It is verified that a constant fundamental magnitude voltage of $V_{DD} - V_k = 30$ V is maintained for the Main transistor within the modulation range. Simulated best constrained-efficiency profiles at 3.9-GHz (center frequency) are reported in Fig. 22. For comparison, the efficiency profiles

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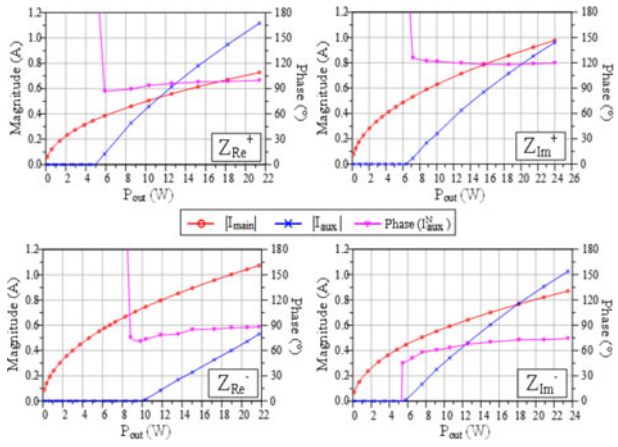


Fig. 19. Optimum dual-input DPA prototype fundamental current profiles. Reference 50 Ω case is indicated for comparison.

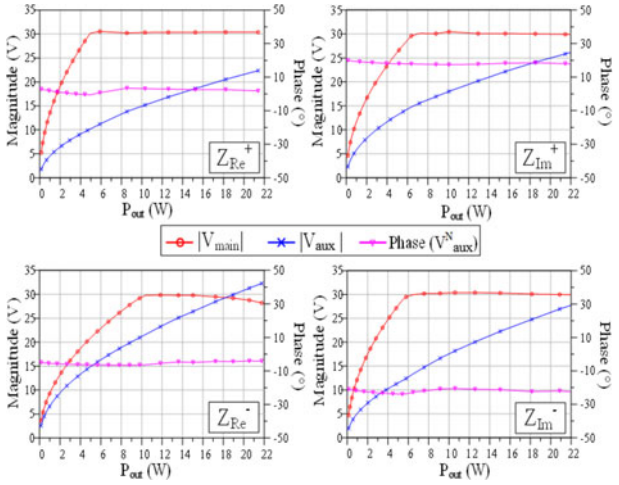


Fig. 21. Simulated voltages produced across Main and Auxiliary devices when optimal RF drives are applied.

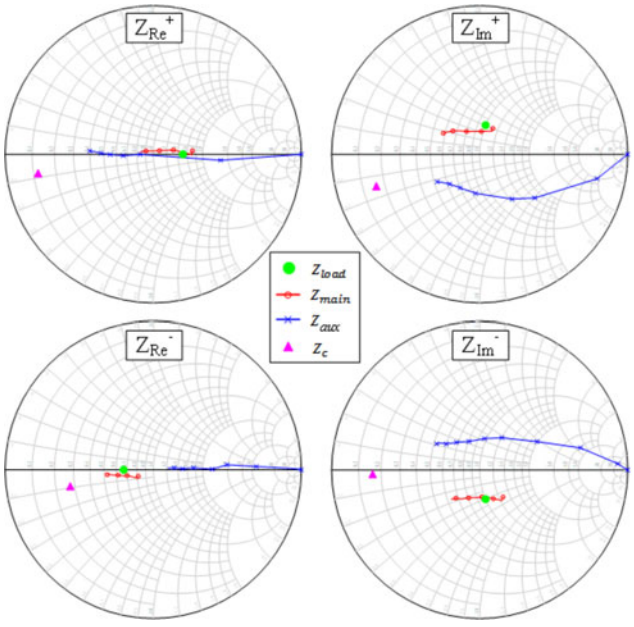


Fig. 20. Impedance trajectories at intrinsic planes of Main and Auxiliary devices when optimal RF driving conditions are applied.

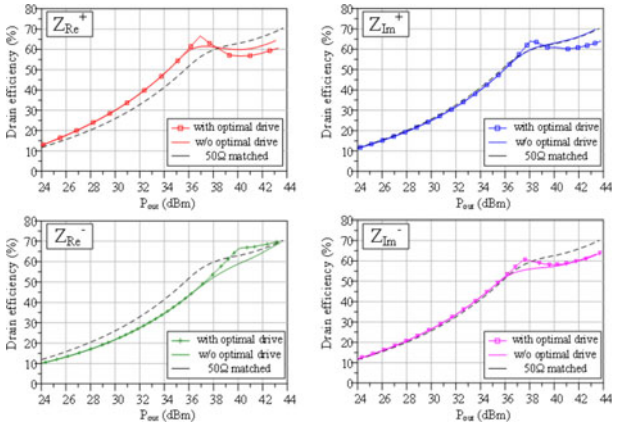


Fig. 22. Simulated DPA prototype efficiency at the center frequency of 3.9 GHz, with and without optimal RF drives simulated. Reference 50 Ω case is reported for comparison.

without optimal RF drives have been reported, along with the matched-configuration initial DPA performances. Simulated DPA efficiency performances when the working frequency is varied are reported in Fig. 23 (across 300-MHz of bandwidth, approximately 8% of fractional bandwidth, representing a typical use case). They are obtained while keeping the same (optimal) RF driving conditions, derived at the center frequency. It shows that, although the overall performances of the DPA are subjected to RF deviations, mainly because of the inherent dispersive nature of the output combiner, a quasi-static approach is sufficient for such moderate RF bandwidth.

Figure 24 shows the associated intrinsic Main and Auxiliary device load lines at the center frequency and at saturated power condition (around 43dBm of output power), and highlights related large-signal reliability issues. It is of particular interest to note the RF stress reduction of the Main device in Z_{re+}, Z_{im+} and Z_{im-} mismatched load condition thanks to the application of the appropriate RF drives (implying a larger Auxiliary device in Z_{re+} case, as it can be seen on the I-V trajectory, and as predicted in the theoretical section).

Dual-input DPA prototype measurement

To fully validate the proposed study, the DPA prototype has been fabricated and tested in a dedicated experimental test bench (Fig. 25). The set-up uses a tailored calibration procedure to ensure phase and amplitude consistency at the DUT input planes. Output load is varied thanks to a calibrated tuner, and DUT available RF powers and DC consumption are monitored. Detailed informations on the calibration procedure and set-up can be found in [14].

Thanks to the dual-input driving capabilities of the test set-up, optimal input RF splitting conditions are accurately extracted by sweeping the RF amplitude and phase distribution between Main and Auxiliary paths, as explained in the section Dual-input DPA prototype simulation. Measured DPA drain efficiency performances are plotted in Fig. 26. Measurements have been

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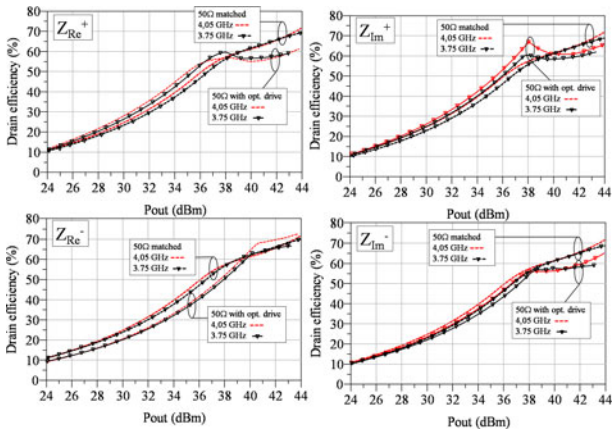


Fig. 23. DPA efficiency profiles when the frequency is varied ±150 MHz from the central frequency (8% of fractional bandwidth). Reference 50 Ω cases are reported for comparison.

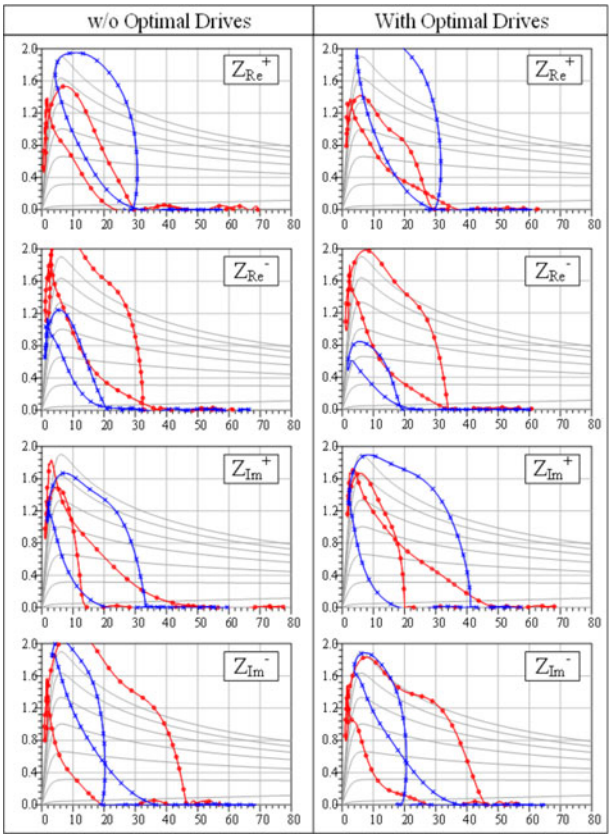


Fig. 24. Simulated intrinsic loadlines of the Main (red circles) and Auxiliary (blue crosses) devices in mismatched environment with and without optimal input RF drives.

carried out at a frequency of 3.6 GHz for the two most representative Z_{Re+} and Z_{Re-}.

It is experimentally confirmed that when the output load impedance is pulled-away from its nominal 50-Ω value, DPA efficiency and power performances are strongly affected, in the way defined in the theoretical section.

For the Z_{Re-} case (Fig. 26, up), backed-off efficiency is degraded whatever the ΔP-Δφ imbalance configuration compared

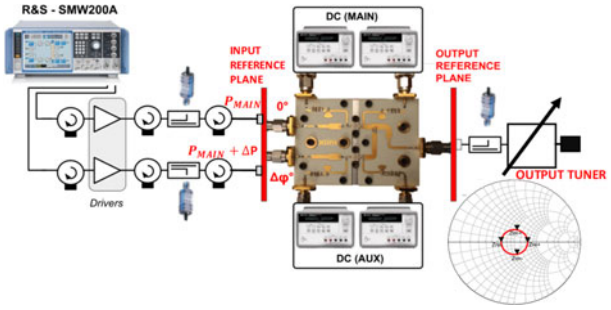


Fig. 25. Fully calibrated dual-input experimental test set-up.

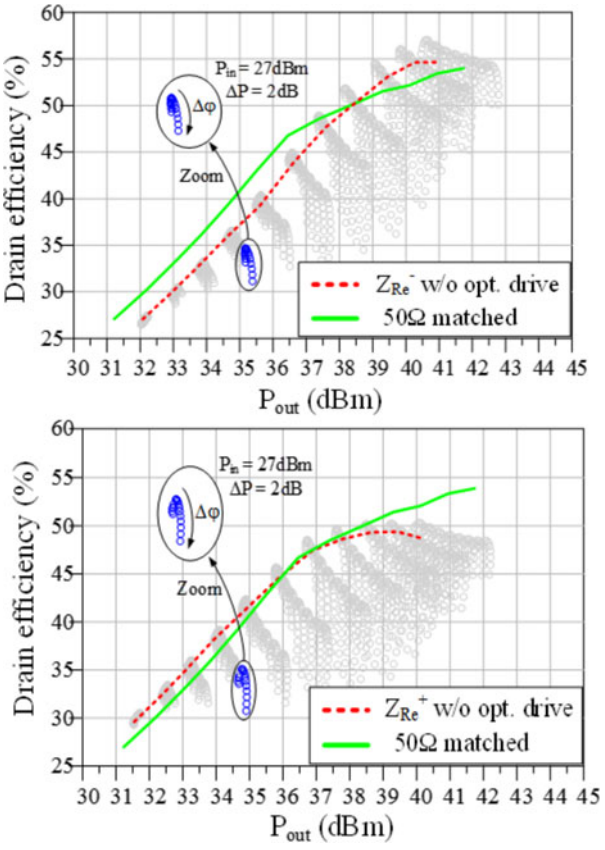


Fig. 26. Measured DPA prototype efficiency performances under mismatched load condition (upper: Z_{Re-}, lower : Z_{Re+}). Nominal 50-Ω matched performances are reported for comparison.

with the nominal 50-Ω matched case. As the RF input level is augmented, it becomes possible to mitigate such degradation, even having higher efficiency compared with the 50-Ω optimal drives. The useful modulating range is however reduced compared with the nominal case, as predicted in Table 1.

For the Z_{Re+} case (Fig. 26, bottom), efficiency at back-off is improved compared with the nominal 50-Ω case. However, due to the early saturation of the main active device peak-power efficiency is always degraded. Useful modulating range is augmented compared with the nominal case, as predicted in Table 1. As explained, in this typical configuration, flexible RF splitting capabilities can be advantageously used to reduce main device RF stress.

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Conclusion

This paper presents theoretical aspects of the DPA topology when used in load mismatch environment. Such conditions can occur in typical AESA RF/microwave subsystems, where DPA can be envisaged as a potential PA topology to mitigate power and efficiency performance degradations. Dual RF input DPA is envisaged as a promising embodiment of the DPA, allowing flexible amplitude and phase distribution of the RF signals to the active cells and thus optimizing their interaction through the non-isolated lossless combining circuit. From a simplified approach, it has been demonstrated how DPA can cope with VSWR thanks to its inherent load-pulling effect. Maximal realizable efficiency profiles have been derived for a single-stage symmetrical DPA configuration, but can be easily generalized for asymmetrical ($n \geq 1$) topologies. A dual-input DPA prototype has been built and experimental measurements corroborate the proposed theoretical study. Results give useful insights into optimal circuit selection (e.g. device periphery ratios, bias selection) and offer clear perspectives to design optimal DPA driver stages.

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