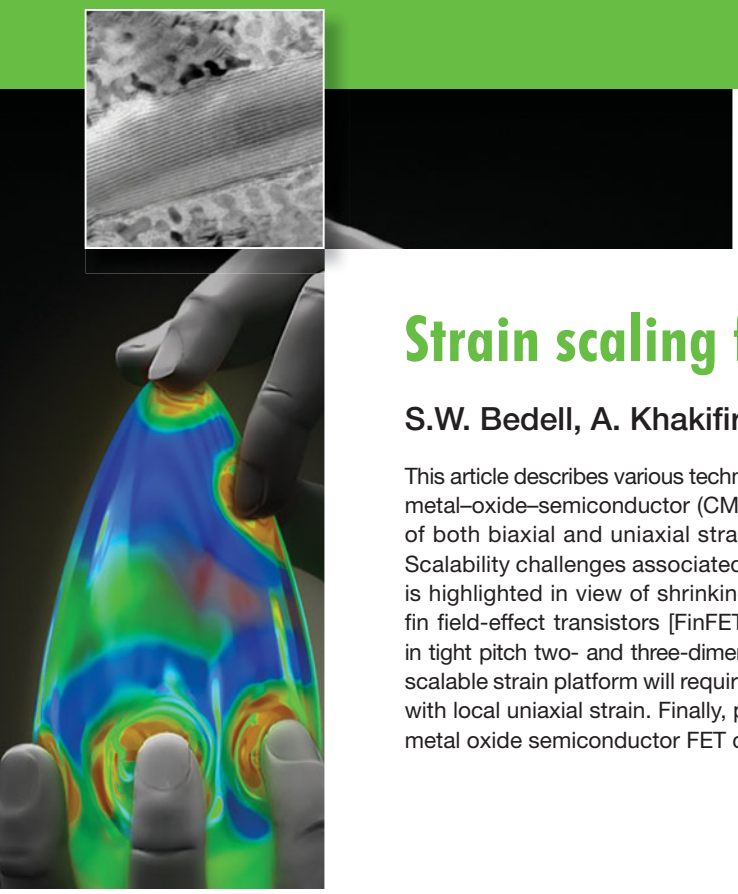


Strain scaling for CMOS

S.W. Bedell, A. Khakifirooz, and D.K. Sadana

This article describes various techniques for applying strain to current and future complementary metal–oxide–semiconductor (CMOS) channels to boost CMOS performance. A brief history of both biaxial and uniaxial strain engineering in planar CMOS technology is discussed. Scalability challenges associated with process-induced uniaxial strain in sub-22 nm CMOS is highlighted in view of shrinking device dimensions and 3D device architecture (such as fin field-effect transistors [FinFETs]). Non-uniform strain relaxation in patterned geometries in tight pitch two- and three-dimensional devices is addressed. A case is made that the future scalable strain platform will require a combination of biaxial strain at wafer level in conjunction with local uniaxial strain. Finally, potential application of strain engineering to advanced III–V metal oxide semiconductor FET channels will be examined.

Brief history of strain engineering in planar CMOS technology

Over the past few decades, a great deal of theoretical and experimental work has been carried out in the field of carrier transport in strained semiconductors;[1] however, it was not until the late 1990s that strained channels were viewed as requisite elements in complementary metal–oxide–semiconductor (CMOS) technology. Since then, a variety of innovative techniques have been devised and integrated as strain-inducing elements into existing CMOS technology. For example, compressive and tensile stressed silicon nitride liners,[2] wafer-scale biaxial strain,[3] local epitaxial stressors for uniaxial strain,[4] and even the strain fields surrounding defects[5] have been used to improve the current drive of modern field-effect transistors (FETs). Here, we explore the most successful of these strain-inducing approaches in planar FET technology, namely lattice-engineering by epitaxial growth. We begin by presenting some of the early work on biaxial strain engineering for FET applications that showed a promising path for drive current enhancement by improving the electron and hole mobility in Si. We then describe the introduction of process-induced uniaxial strain and its advantages compared to biaxial strain with respect to drive current in scaled FETs. Finally, the limitations of strain scaling and possible future strategies are explored.

The perfect miscibility of the Ge_x $Si_{(1-x)}$ alloy system permits control of the lattice parameter from that of Si (0.543 nm) to that of Ge (0.566 nm) by controlling the composition during epitaxial growth. Because the lattice parameters of these alloys are larger than that of Si, subsequent layers of Si grown on relaxed Ge_x $Si_{(1-x)}$ alloy layers will be under tensile strain. Early work[6] on thick, strain-relaxed compositionally graded Ge_x $Si_{(1-x)}$ layers grown on Si substrates demonstrated that although relaxation was dislocation-mediated, defect densities could be made relatively low ($\sim 10^6$ cm^{-2}). Shortly thereafter, some of the first strained-Si FET devices were fabricated using thin Si layers grown on these thick, relaxed Ge_x $Si_{(1-x)}$ graded buffer layers (GBLs) formed on Si substrates. The amount of (biaxial) tensile strain in the thin Si channel layer was varied by controlling the Ge content in the GBL. This process of engineering the lattice parameter directly on the starting substrate prior to device fabrication would eventually be referred to as "wafer-scale" or "global" strain. The main advantages to this approach were that the magnitude and uniformity of the strain could be well-controlled, and standard device fabrication steps could then be used. Both electron[3] and hole[7] mobilities were shown to improve significantly with increasing strain in long-channel FETs fabricated on biaxially strained Si using this approach.

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Based largely on these early results, and the prospect of both *n*- and *p*-type FET (nFET and pFET) drive current enhancement using the same strained Si layer, attempts were made to develop production-worthy relaxed $Ge_xSi_{(1-x)}$ buffer layers as the starting substrates for biaxial strained Si CMOS. IBM demonstrated functional strained Si (0.55% tensile strain) CMOS with an nFET drive current enhancement of 80% for long channel devices and ~20% for 60 nm devices compared to silicon-on-insulator (SOI) control devices using SiGe-on-insulator (SGOI) substrates. **Figure 1**a shows a cross-sectional TEM image of the biaxially strained Si nFET device.[8] The SGOI substrates represented a new way to integrate strain-relaxed SiGe buffer layers with SOI technology and were fabricated by high-temperature (~1250°C) oxidation of epitaxial SiGe layers grown on SOI wafers. This process allowed the formation of thin, high-quality SiGe layers directly on a buried oxide layer. Because the relaxation during oxidation was strictly dislocation-mediated for unpatterned wafers, both the Ge content as well as the final strain state of the SGOI (including fully strained) could be controlled independently.[9] Although the observed nFET drive current enhancement was notable, the pFET devices did not show any drive current enhancement.

By growing strained $Ge_x Si_{(1-x)}$ layers within the source/drain regions of the device, uniaxial compressive strain can be imparted to the channel region directly. The introduction of this "process-induced" or "local" channel strain using embedded SiGe in pFET devices[10] demonstrated the advantages of uniaxial compressive over biaxial tensile strain in hole transport. In that work, greater than 50% enhancement in hole mobility was reported as a result of both uniaxial channel strain and reduced access resistance due to the higher amount of substitutional B in the SiGe alloy and reduction of the Schottky barrier height between the silicide and the SiGe. Figure 1b shows a cross-sectional TEM image of a pFET device with uniaxial channel strain using embedded SiGe in the source/drain regions. The advantage of uniaxial compressive strain compared to biaxial tensile strain in hole transport is ascribed to the difference in the resulting band structure in the two cases.[11] The primary origin of hole mobility enhancement in biaxial tensile Si is the reduced scattering that results from strain-induced splitting of the heavy and light hole sub-bands. In the case of uniaxial compressive Si, the primary origin is valence band warping resulting in a lower effective mass in the channel direction. In devices with channel lengths in the tens of nanometers, scattering becomes less important than carrier mass, and therefore uniaxial compressive strain results in superior drive current enhancement in scaled pFETs. Additionally, valence band splitting due to confinement effects in biaxial tensile Si counteract the strain-induced splitting, leading to overall degradation of hole mobility at high vertical electric fields. For nFET devices, biaxial tensile and uniaxial tensile strains both led to mobility enhancement. The complete analysis is somewhat more complicated, and an excellent review can be found in Reference 11.

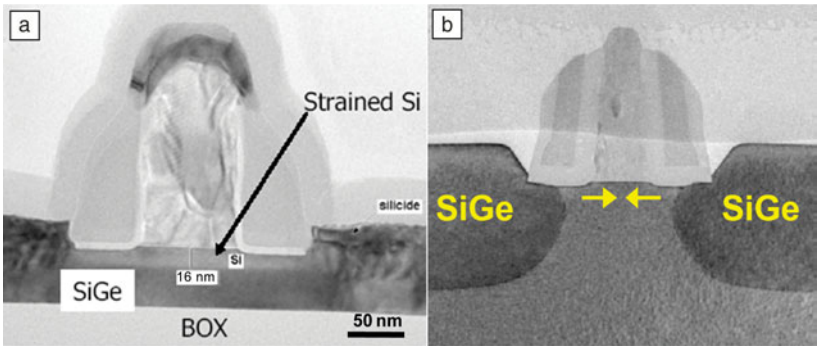


Figure 1. (a) Cross-sectional transmission electron microscopy (TEM) image of biaxial (tensile) strained Si *n*-type field-effect transistor (FET) fabricated using SiGe-on-insulator as a growth template. Reprinted with permission from Reference 8. © 2004 American Institute of Physics. (b) Cross-sectional TEM image of an uniaxial strained (compressive) *p*-type FET device using embedded SiGe in the source and drain regions. Reprinted with permission from Reference 10. © 2003 IEEE.

Scalability of process-induced strain

In subsequent technology generations, uniaxial process-induced strain was increased in a number of ways, including by (1) increasing the Ge content of the embedded SiGe (e-SiGe), (2) increasing the proximity of the SiGe stressor to the channel region (including thinner spacers and alternate recess geometry), and (3) taking advantage of replacement gate integration schemes to transfer more strain to the channel (including strained gate material).[12,13] In fact, the uniaxial strain engineering approach has been leveraged not only in pFETs but also in nFETs to increase effective strain in both types of channels in the latest 22 nm technology node.[14] A fourth generation of pFET e-SiGe (**Figure 2**a) and a novel *in situ* doped nFET e-Si:C (Figure 2b) have been introduced into IBM's 22 nm CMOS. Because nFETs require uniaxial tensile strain to enhance electron mobility, a material with a smaller lattice parameter than Si must be used in the source/drain region. Unfortunately, the perfectly miscible SiGe alloy system has no counterpart to enable lattice contraction. The very low solubility of C in Si (~10^{17} cm^{-3}) makes using the Si:C system as a stressor layer challenging. However, by incorporating ~1.5% substitutional carbon, the embedded Si:C (e-Si:C) applies ~340 MPa additional tensile strain to the nFET channel for improved electron mobility. The dual embedded source/drain modules are integrated with dual stress liners, with a resulting nominal strain enhancement of ~1.25× relative to 32 nm SOI (Figure 2c).

Limitations of process-induced strain scaling

Although strain scaling efforts have largely been successful so far, the continued shrinking

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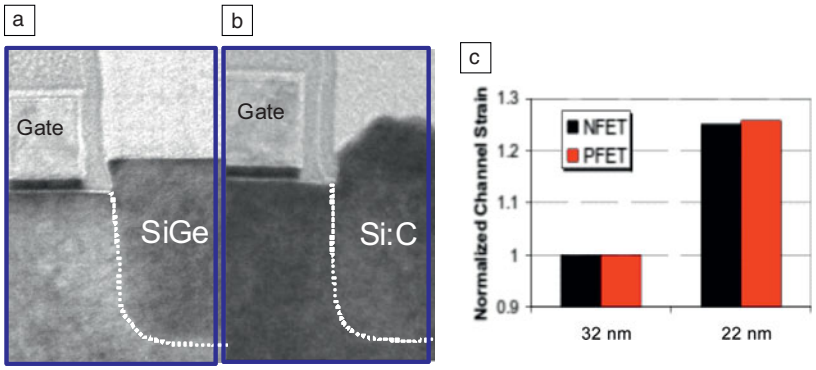


Figure 2. Cross-sectional TEM image of uniaxial compressive and tensile strain in (a) embedded SiGe (pFET) and (b) embedded Si:C (nFET) in the source and drain regions of 22 nm complementary metal–oxide–semiconductor. (c) *p*-type field-effect transistors (FETs) and *n*-type FETs using embedded SiGe in the source and drain regions. Reprinted with permission from Reference 14. © 2012 Institute of Electrical and Electronics Engineers.

of device pitch (feature density) at approximately fixed gate length is making localized stressors less effective at each technology generation. Due to the loss of embedded SiGe volume in pFETs, one has to increase Ge content and increase proximity simply to match the transistor performance benchmarks of the previous technology generation.[15] Similarly, C substitutional content has to increase from the current 1.5% to >2% in the future to maintain nFET performance scaling, and this is highly challenging. Even though both dimensional scaling and strain scaling in Si pose fundamental physical limitations, future strain scaling may end up having a more abrupt terminus in the form of material failure. For example, a high density of defects accompanied by stress relaxation is expected in pFETs with high Ge content in the embedded $Si_x Ge_y$ (e.g., >50%). Similarly, defects in high substitutional C are expected to create strain relaxation in nFETs in addition to lower *n*-doping. We next describe a potential path forward to continue strain scaling beyond 22 nm CMOS.

A scalable strain platform: Mixed bi- and uniaxial wafer-level strain

One of the strongest arguments in favor of wafer-level strain as opposed to process-induced strain has always been that the former is independent of device pitch. In other words, because the strained material is integral to the substrate itself, the magnitude of strain would be independent of patterned feature (mesa) size or device geometry. This is true for dimensions down to roughly the micron length scale, however, below this, elastic relaxation due to the free edges of the mesa becomes a significant fraction of the average strain across the mesa. Early work on elastic (non-dislocation mediated) relaxation of strained SiGe islands on borophosphate silicate glass layers[16,17] showed that if the oxide layer was above the reflow temperature, strained SiGe layers could relax by physical expansion. In early 2005, plan-view transmission electron microscopy (TEM) moiré analysis was used to map the two-dimensional strain fields in nFET devices formed on SGOI substrates.[18] Mixed biaxial and uniaxial strain components were shown to exist under the gate regions formed on asymmetric mesas, indicating that mesa geometry could be used to convert biaxial strained layers into mixed biaxial/uniaxial ones. **Figure 3** shows a plan-view TEM image of an nFET device with a fringe system (moiré pattern) resulting from the two-beam interference between the Si/SGOI above the buried SiO_2 (BOX) layer and the bulk Si below the BOX layer. By converting the fringe spacing into strain, it is concluded that 1.08% tensile Si strain is present parallel with the channel direction, while only 0.57% Si strain is present perpendicular to the channel.

Later, pFET devices were demonstrated[19] on elastically relaxed SGOI mesas. Mobility enhancement was measured as a function of device width, which essentially translates into pure biaxial strain for the widest mesas to nearly pure uniaxial. The results showed an astounding ~2× drive current enhancement for mesa widths below about 0.3 μm. Because nearly all modern CMOS technology features are at or below these dimensions, this approach may open up new opportunities for scalable strain engineering. The effect of biaxial-to-uniaxial conversion by elastic relaxation was studied on a number of different strained layer combinations for pFET devices,[20] and the results were consistent with the performance enhancement results in Reference 19. In the latter work, the simplest structure, namely SiGe/SOI, showed the highest drain current enhancement (2.7× for long channels and 2× for short channels).[20] Moreover, the SiGe/SOI devices with the smallest width demonstrated on–off current ratio (I_{ON}/I_{OFF}) characteristics

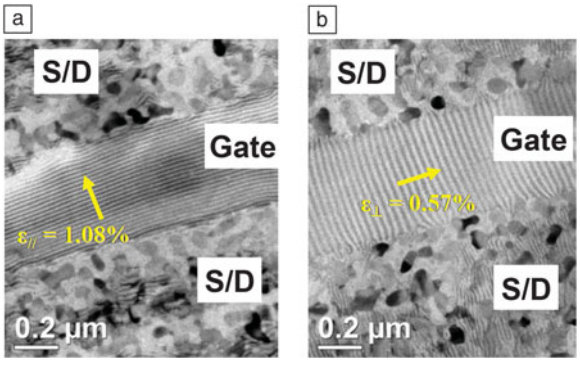


Figure 3. Plan-view TEM images of an *n*-type field-effect transistor (nFET) device fabricated on s-Si/SiGe-on-insulator showing a moiré fringe system. The asymmetric fringe spacing indicates that elastic relaxation occurred in the channel direction leading to mixed uniaxial and biaxial strain in the channel. The strain (ε) was 1.08% tensile in the channel direction (a) and 0.57% tensile strain perpendicular to the channel direction (b). S/D, source/drain. Reprinted with permission from Reference 18. © 2005 Springer.

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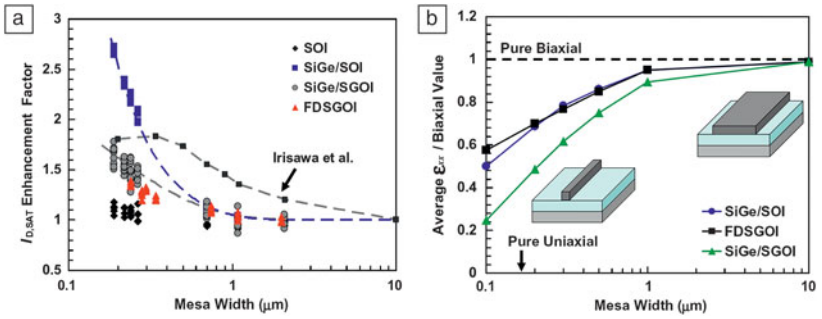


Figure 4. (a) Long channel mobility ($I_{D,SAT}$) enhancement factor as a function of device width for a variety of strained layer *p*-type field-effect transistor (pFET) devices. (b) Calculated average strain ε_{xx} along the channel direction as a function of device width showing the conversion from biaxial to nearly pure uniaxial strain due to the free edge relaxation. SOI, Si on insulator; SGOI, SiGe on insulator; FDSGOI, fully depleted SiGe on insulator. Adapted with permission from Reference 20.

comparable to published pFET data with process-induced uniaxial strain. **Figure 4** shows a summary of the effect of uniaxial strain conversion on a variety of device structures (long channel) compared to the calculated average strain along the mesa width.[20]

The above approach of mixed biaxial and uniaxial strain has recently been extended to enhance the drive current of fully depleted nFETs in extremely thin (ETSOI) substrates where the device layer contains strained Si.[21] These substrates are known as strained silicon on insulator (sSOI) substrates. **Figure 5**a[22] shows that at ~0.8% tensile strain in sSOI, an I_{ON} enhancement of ~25% is achieved in nFETs over those fabricated on virgin SOI despite 100 nm gate pitch. Most recently, similar results have been reported on FinFETs fabricated on sSOI substrates, with gate pitch down to 64 nm.[23] Similarly, the effectiveness of a compressively strained SGOI substrate[22] in enhancing the drive current of a pFET is apparent in Figure 5b. At ~0.9% strain in SGOI, I_{ON} enhancement of ~35% in pFETs is achieved over those fabricated on virgin SOI.

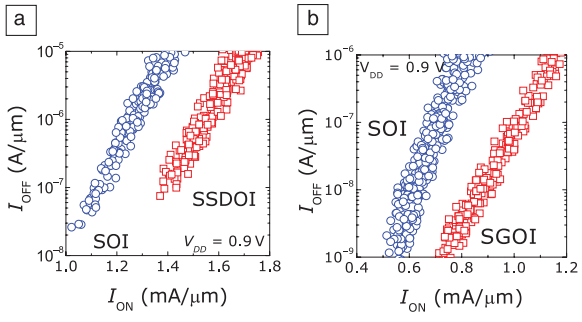


Figure 5. On–off current (I_{ON}–I_{OFF}) characteristics of extremely thin silicon-on-insulator (SOI) (a) *n*-type field-effect transistors (nFETs) formed on SOI and strained silicon on insulator (sSOI) substrates and (b) *p*-type FETs with Si and SiGe channels demonstrating the effectiveness of substrate strain engineering.

The effect of strain relaxation at the edges of a narrow ETSOI pFET is shown in **Figure 6**.[24] In a relatively wide device (e.g., 1 μm wide), the compressive strain in the SiGe channel is purely biaxial, and the I_{ON} enhancement is modest (<20%). However, as the devices are made narrower and strain relaxation at edges increases, part of the biaxial strain is converted to uniaxial strain (see earlier discussion, Figures 3 and 4), thus contributing to even higher I_{ON}. The conversion of predominantly biaxial strain to predominantly uniaxial strain in narrow devices bodes well for substrate engineering-based strain scaling for future CMOS.

Nevertheless, edge relaxation in small devices is still a concern. Proper process engineering is required to alleviate such stress relaxation. For example, recessing of source and drain regions, which is traditionally used to form embedded stressors, should be avoided and instead raised source drain structures should be used. Similarly, implantation in source-drain regions should either be avoided altogether, or implant conditions should be adjusted to minimize strain relaxation.

3D device architectures: FinFETs

It has been frequently argued that with a steeper subthreshold swing in a fully depleted device, such as a FinFET, strain may not be required as a performance booster. Smaller subthreshold swing and drain-induced barrier lowering in these devices compared to bulk CMOS are considered to be performance boosters.

At low I_{OFF}, better short channel control in FinFETs indeed provides a significant boost compared to the baseline, but this

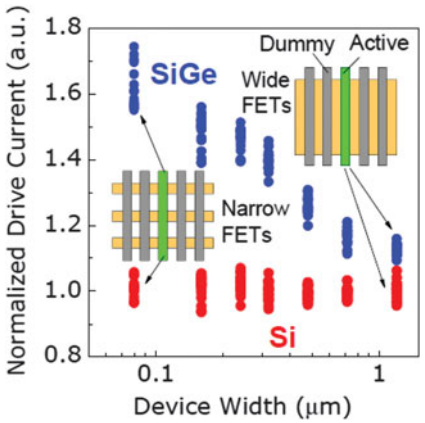


Figure 6. Drive current as a function of device width for relaxed Si and compressively strained SiGe channels with extremely thin silicon-on-insulator (SOI) *p*-type field-effect transistors (pFETs). As the device is made narrower, the component of the strain parallel to the gate is gradually relaxed, leading to a predominantly uniaxial strain in narrow devices. Reprinted with permission from Reference 24. © 2012 IEEE.

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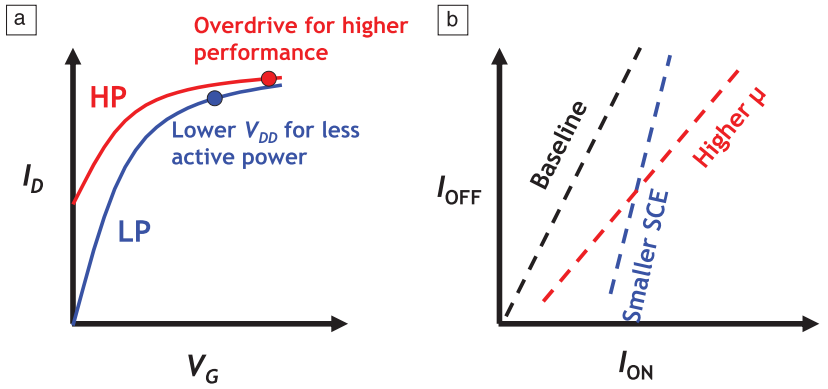


Figure 7. (a) Typical drain current–gate voltage (I_D–V_G) characteristics of low-power (LP) and high-performance (HP) transistors demonstrating why HP devices do not benefit as much from a steeper subthreshold swing. (b) A schematic comparison of the on current (I_{ON}) versus off current (I_{OFF}) characteristics for a baseline technology compared to a device with smaller short channel effect (SCE) and a device with higher mobility (μ).

benefit diminishes at higher $I_{OFF,}$ where high-performance devices typically operate. Low-power devices that operate at supply voltages (V_{DD}) smaller than 1 V with I_{OFF} in the low nA μm^{-1} range (to reduce active and leakage power) can benefit significantly from a smaller subthreshold swing (**Figure 7**). However, high-performance applications that operate at higher supply voltages (typically >1 V) with I_{OFF} in the hundreds of nA μm^{-1} range (for maximum performance) require both higher channel mobility (Figure 7) and improved short channel control.[25] Therefore, there is a drive to apply strain engineering even to FinFETs.

Strain engineering in FinFETs

Several theoretical and experimental studies have already been conducted to determine channel strain–carrier mobility correlation in FinFETs at the fundamental level. This includes carrier mobility measurements in FinFETs[26–28] under mechanical strain by wafer bending. However, since the magnitude of the maximum mechanical strain is limited to <0.1%, these experiments do not provide quantitative feedback that is required to accurately calibrate theoretical calculations and for an in-depth understanding of high-field carrier transport in short channel FinFETs. We next describe the role and limitations of strain engineering in FinFETs.

Technology computer aided design (TCAD) simulations have been used to study the effectiveness of process-induced stressors previously developed for planar devices, such as e-SiGe, SiN_x stress liners, gate electrodes, contacts, and device isolation in FinFET structures.[29–31] It was shown that strain transfer in FinFETs can occur in an analogous manner to planar FETs, albeit with a non-uniform strain distribution due to its three-dimensional nature. However, initial experimental data suggest that the magnitude of strain transfer in FinFETs is lower than that in planar FETs. For example, the I_{ON} data from 22 nm FinFETs, when normalized to the actual device width, are inferior to that from 32 nm planar FETs, suggesting that the effective channel strain is lower in FinFETs than in planar FETs. This occurs despite increased Ge content in e-SiGe and its closer proximity to the channel in FinFETs.

Figure 8a shows the strain profile along the fin height measured using nano-beam diffraction in a typical bulk FinFET with e-SiGe. The maximum strain occurs at the top of the fin where its magnitude is comparable to what is expected from a planar device with an equivalent e-SiGe. The strain decreases gradually from the top of the fin toward its bottom. Consequently, the average mobility boost is only a fraction (nearly half) of that in a planar device. This observation is in qualitative agreement with TCAD simulations,[29] shown in Figure 8b. It should be noted that non-uniform strain distribution occurs even in bulk planar devices; however, its impact on such devices is minimal because carrier transport is localized in the vicinity of the top surface.

Despite an overall reduction in strain, e-SiGe remains an upfront option for future high-performance pFinFETs because in addition to strain, e-SiGe provides much needed low series resistance to achieve high drive current. Another effective knob to enhance strain, particularly in FinFETs, is the gate electrode itself, as it wraps around the channel and can efficiently transfer its stress to the channel.[32] In fact, process conditions to produce gate electrodes with the desired strain level have already been identified, and direct coupling of the gate stress to the channel has also been confirmed by both physical (strain measurements) and electrical measurements. However,

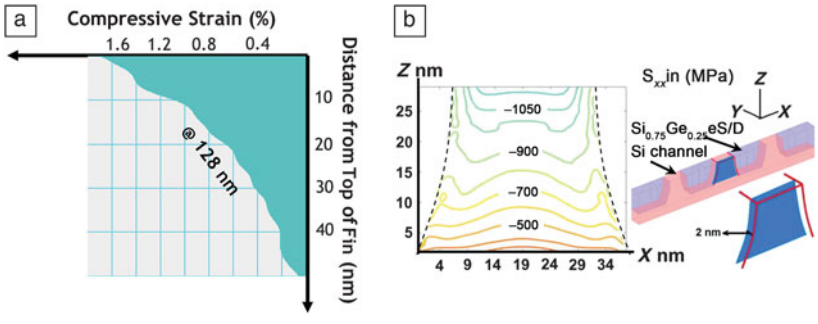


Figure 8. (a) A typical strain distribution in a bulk FinFET showing the maximum strain at the top of the fin and decreasing strain toward the bottom of the fin. (b) Contours of longitudinal stress (S_{xx}, in MPa) in a FinFET as a function of its height (Z). Typical fin height is ~30 nm, and the gate pitch is 76 nm. The strain is at its maximum at the top of the fin, and it diminishes toward the bottom of a fin. eS/D, embedded source/drain. Reprinted with permission from Reference 29. © 2012 IEEE.

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the choice of the stressor metal electrode is constrained by not only its work function, which impacts the threshold voltage, but also other factors, such as inversion capacitance, device reliability, and complexity of integration.

Substrate strain engineering for high-performance FinFETs

Although, performance gain in nFinFETs on sSOI and pFinFETs on SGOI with a relaxed pitch has been experimentally verified,[33] such gain and its magnitude in tight ground-rule (<100 nm pitch) devices has yet to be determined. Furthermore, co-integration of nFETs and pFETs will require two opposite kinds of strain (i.e., tensile and compressive) on the same substrate, which has not yet been demonstrated. It may be possible to convert tensile strain of sSOI to compressive strain locally via a combination of selective SiGe (>40%) growth and thermal mixing (or Ge condensation).

Strain effects in III–V devices

Even though III–V compounds can provide a wealth of strain engineering options for both n- and/or pFETs because of a variety of substrate/grown layer combinations, there is a surprisingly limited body of published literature on this topic.[34–37] For example, for *n*-channel devices, InGaAs can be grown with tensile or compressive strain by varying the In and/or Ga content on an InP or a GaAs substrate. Similarly, compressively strained AlGaSb can be grown on GaAs, or InGaSb can be grown on GaSb in multiple configurations (single or multiple quantum wells) for *p*-channels.

Unlike for electrons in III–Vs, where polar scattering is the only dominant scattering mechanism, both deformation potential and polar scattering mechanisms are important for hole mobility. The hole mobility can be significantly enhanced by varying the group V element while keeping the group III element fixed. For example, hole mobility increases from 200 for InP to 450 for InAs to 850 $cm^2\ V^{-1}\ s^{-1}$ for InSb. A similar pattern is true for holes in GaP (150 $cm^2\ V^{-1}\ s^{-1}$) to GaSb (900 $cm^2\ V^{-1}\ s^{-1}$).[35] On the other hand, varying the III element does not significantly impact the hole mobility. The impact of strain on *p*-type hole mobility is profound, especially that of compressive strain, which yields 2× mobility enhancement under a biaxial strain of 2%. The hole mobility enhancement for GaAs under uniaxial compressive strain is expected to be even greater (10).

The effect of strain on the quantized bandgaps of both 5 nm (001) and (111) GaAs and $In_{0.75}Ga_{0.25}As$ has been studied in detail.[34] The quantized bandgap narrows under compressive strain and increases under tensile strain. The observed bandgap modulation in conjunction with strain is very attractive for InGaAs based III–V metal oxide semiconductor FETs (MOSFETs) and can potentially be exploited to reduce band-to-band tunneling current while maintaining high channel mobility.

The latest MOSFETs fabricated on strained InGaAs-on-insulator indeed confirm that high strain up to 1.7% can be successfully introduced in the channels, and these channels exhibit 1.65× mobility enhancement compared to those without strain (**Figure 9**).[38] These results indicate that the thin body (<15 nm) III–V-on-insulator structure with highly strained channels is a promising way to realize ultimately scaled future III–V MOSFETs.

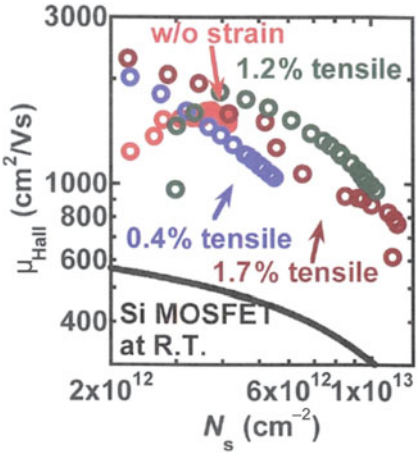


Figure 9. Hall mobility characteristics (μ_{Hall}, carrier mobility; N_s, carrier density) of strained $In_{0.53}Ga_{0.47}As$-on-insulator metal oxide semiconductor field-effect transistors (MOSFETs), with Si MOSFET at room temperature (R.T.) for comparison. Reprinted with permission from Reference 38. © 2013 Institute of Electrical and Electronics Engineers.

Concluding remarks

Implementation of strain as a performance enhancing element has been phenomenally successful and effective since 90 nm Si CMOS. Strain scaling has continued unabated through 22 nm CMOS via a combination of SiGe and Si:C epitaxial stressors, dielectric stressors, and crystallographic defects in the vicinity of the MOSFET channel. However, such strain scaling in future CMOS is becoming challenging due to the limited device footprint and device geometry (planar or FinFETs). We have demonstrated that a combination of wafer level biaxial strain in conjunction with local uniaxial strain can provide a plausible platform for continued strain scaling in Si. Advances in cost-effective SGOI and sSOI substrate manufacturing in conjunction with successful reduction in substrate defect density will be paramount for continued success of strain scaling in Si. The demonstrated performance benefit of strain in III–Vs should open yet another option for continued CMOS scaling beyond 2020.

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