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Multi-range 3.5 GHz rectifiers for WPT and RFEH applications

Mounira Ben Yamna[1], Nabil Dakhli[2] and Hedi Sakli[3,4]

[1]MACS Laboratory, National Engineering School of Gabes, University of Gabes, Gabes, Tunisia; [2]Innov'COM Lab, Sup'COM, University of Carthage, Carthage, Tunisia; [3]SYSCOM Laboratory, National Engineering School of Tunis, University of Tunis El-Manar, Tunis, Tunisia and [4]EITA Consulting, Montesson, France

Research Paper

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Corresponding author: Mounira Ben Yamna; Email: benyemnamounira@gmail.com

Abstract

This paper presents the design, optimization, fabrication, and measurement of three RF-to-DC rectifiers operating at 3.5 GHz for wireless power transfer and RF energy harvesting applications. A low-power rectifier achieves a peak efficiency of 50.5% at -2 dBm, while a high-power rectifier reaches 61.2% at 15 dBm. To extend the operating range, a wide-range rectifier based on a passive dynamic sub-rectifier selection architecture is proposed. The developed system achieves a maximum efficiency of 54.7% at 16 dBm and maintains over 20% efficiency across a 41 dB input power range. Experimental results validate the proposed designs and show good agreement with simulations.

Introduction

The rapid growth of wireless sensor networks and the Internet of Things (IoT) has created a strong demand for reliable and long-term energy solutions for distributed low-power devices. Conventional batteries suffer from limited lifetime, periodic replacement requirements, and environmental and logistical constraints, particularly in remote or inaccessible locations [1]. To overcome these limitations, energy harvesting techniques exploiting ambient sources such as light, heat, vibration, and radio-frequency (RF) signals have emerged as promising solutions for enabling energy-autonomous systems [2]. In parallel, wireless power transfer (WPT) allows energy delivery over distance without physical connections, further supporting sustainable device operation [3].

With the global deployment of fifth-generation (5G) wireless networks, particularly in the sub-6 GHz bands, new opportunities have arisen for RF energy harvesting (RFEH) and far-field WPT [4]. Owing to their widespread availability, relatively stable power levels, and favorable propagation characteristics, sub-6 GHz 5G signals constitute an attractive ambient energy source for low-power electronic devices [5, 6]. Moreover, research efforts are now extending beyond 5G toward millimeter-wave and terahertz bands, which promise higher available power density and wider bandwidths for energy harvesting applications [7, 8]. These advancements align with the vision of next-generation IoT networks, where ubiquitous connectivity and self-powered nodes are key enablers of smart environments.

A key component in both RFEH and WPT systems is the rectenna, which combines an antenna for RF energy capture with a rectifier circuit that converts the received RF signal into usable DC power [3]. The overall system efficiency is largely determined by the RF-to-DC rectifier, particularly at low input power levels where diode nonlinearity and impedance mismatch significantly degrade performance [9]. Recent advances in antenna design, such as circularly polarized dielectric resonator antennas (DRAs), have further improved RFEH efficiency by offering polarization diversity and robustness in dynamic environments. For instance, a recent work [10] introduced a circularly polarized MIMO wearable DRA addressing mutual coupling and integration challenges, providing valuable insights for compact and efficient rectenna design.

However, practical integration of rectennas into IoT and sensor networks remains challenging. Environmental variations, miniaturization constraints, and system-level integration with sensors and power management circuits introduce impedance mismatches and parasitic losses that limit RF-to-DC conversion efficiency [11–13]. These challenges motivate the development of rectifier architectures capable of maintaining high efficiency under variable RF input power conditions.

In practical scenarios, the received RF power depends on the transmitted power, operating frequency, antenna gains, and propagation distance, as described by the Friis transmission equation [14]. To maximize the harvested power, impedance matching between the antenna

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and the rectifier is essential, while low-pass filtering is typically employed to smooth the rectified DC output [15]. Nevertheless, the nonlinear behavior of Schottky diodes causes the rectifier input impedance to vary with frequency and input power, leading to significant efficiency degradation outside the design operating point [16]. As a result, conventional rectifiers optimized for specific frequencies or power levels often exhibit limited performance under fluctuating RF conditions [15, 17].

Beyond antenna optimization, recent studies have increasingly focused on rectifier design and system-level solutions to improve RFEH performance. Adaptive impedance matching, dynamic load modulation, and hybrid rectifier architectures have been proposed to extend the operational input power range and enhance robustness in practical IoT systems [18–21].

This work proposes a multi-range RF-to-DC rectifier approach operating at 3.5 GHz for WPT and RFEH applications. Three complementary rectifier architectures are designed and experimentally validated to efficiently cover low, high, and wide RF input power conditions. In particular, a passive dynamic sub-rectifier selection (DSRS) architecture is introduced to extend the operational input power range by dynamically directing the incident RF power toward the most suitable sub-rectifier through impedance adaptation only, without using switches or active control circuits. Compared to existing rectifiers, the proposed approach achieves an extended dynamic input power range while maintaining high conversion efficiency and low circuit complexity, making it well-suited for 5G-enabled IoT and energy-autonomous systems. The remainder of this paper is organized as follows. Section II reviews related work on RFEH rectifiers. Section III presents the rectifier architectures. Sections IV and V describe the low- and high-input-power rectifiers (HIPRs), respectively, including experimental validation and comparison with state-of-the-art designs. Section VI focuses on the wide-range rectifier based on the DSRS concept, and Section VII concludes the paper.

Rectifier architecture

The rectifier architecture, shown in Fig. 1, includes an input matching network, a high-frequency (HF) bandpass filter, a Schottky diode for RF-to-DC conversion, a low-pass filter for DC extraction, and a resistive load.

The three proposed rectifier architectures target different RF input power regimes: a low-power rectifier optimized for weak RF signals, a high-power rectifier designed for strong RF excitation, and a wide-range rectifier based on a passive DSRS dual-path architecture enabling efficient operation over an extended input power range.

At sub-6 GHz 5G frequencies, microstrip RF-to-DC converter design must account for substrate and conductor losses, impedance matching accuracy, and parasitic effects, requiring compact layouts and accurate electromagnetic modeling to maintain high efficiency.

HF filter

The HF filter in this rectifier design serves as a band-pass filter, strategically placed before the diode to attenuate harmonics generated during signal rectification from reflecting back toward the antenna, which could otherwise degrade system performance. As shown in Fig. 2, the filter is composed of a quarter-wavelength transmission line that is short-circuited to ground, creating a

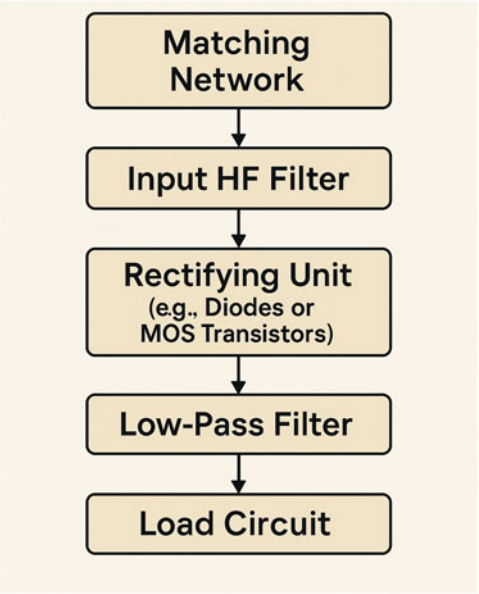


Figure 1. Typical RF-to-DC rectifier architecture.

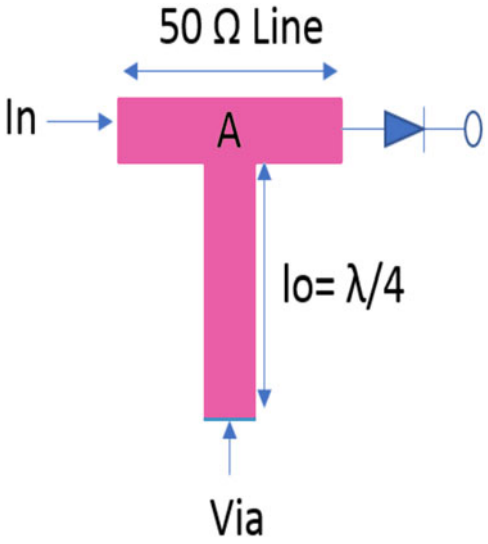


Figure 2. HF filter architecture.

structure that selectively allows desired frequencies to pass while suppressing unwanted signals.

DC filter

This element is designed to suppress the fundamental RF signal along with its harmonics, permitting only the rectified DC signal to reach the load. As illustrated in Fig. 3, the filter comprises four microstrip transmission lines (L1, L2, L3, L4) arranged to achieve the desired frequency-selective behavior. Each line is tailored to target specific unwanted frequency components while ensuring smooth DC output. L1 is a $\lambda/4$ open-circuited line that behaves as a short-circuit at the fundamental frequency and its odd harmonics, effectively attenuating them. L2, designed as a $\lambda/8$ open-circuited line, is responsible for blocking the $2^n d$, $6^t h$, $10^t h$, $14^t h$, and similar

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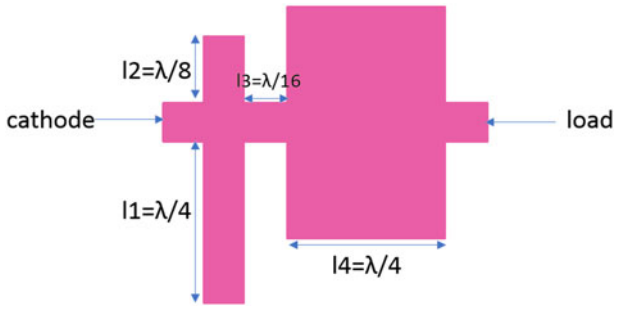


Figure 3. Typical RF-DC rectifier architecture.

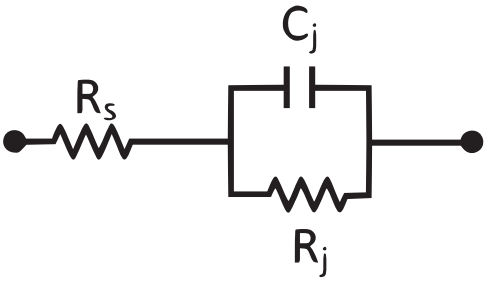


Figure 4. Electrical modeling of the Schottky diode.

even-order harmonics, as determined by its resonance characteristics. L3, a $\lambda/16$ line, is specifically tuned to suppress the 4th harmonic. Lastly, L4 is a wide $\lambda/4$ line that functions as a parallel capacitor, effectively smoothing out the output voltage ripple and stabilizing the rectified DC component supplied to the load.

Impedance matching network

In order to maximize the amount of power transferred to the diode, impedance matching is essential. In this context, several microstrip line matching techniques are employed.

- Impedance Matching Using a Single Transmission Line: In this approach, a single transmission line connects the antenna to the rectifying circuit whose impedance is characterized by a fixed power and load. The transmission line length l and its characteristic impedance Z_l must be determined. For effective matching, the reflection coefficients must have equal magnitude:

$$|\rho_{\text{ant}}| = |\rho_{\text{red}}|$$

Given:

$$\rho_{\text{ant}} = \frac{Z_{\text{ant}} - Z_l}{Z_{\text{ant}} + Z_l} \tag{1}$$

$$\rho_{\text{rect}} = \frac{Z_{\text{rect}} - Z_l}{Z_{\text{rect}} + Z_l} \tag{2}$$

where Z_{ant}, Z_{rect}, and Z_l are the antenna impedance, rectifier impedance, and line characteristic impedance, respectively. From these equations, Z_l can be determined. The line length l is given by:

$$l = \frac{\lambda}{4\pi}\left(\arg(\rho_{\text{rect}}) - \arg(\rho_{\text{ant}})\right) \tag{3}$$

This method offers advantages such as simplicity and compactness. However, it is only applicable when the resulting characteristic impedance Z_l is practical. For the line width to be manufacturable and to maintain a quasi-TEM mode, Z_l must satisfy the condition:

$$Z_{\text{inf}} < Z_l < Z_{\text{sup}}$$

where Z_{inf} and Z_{sup} are the lower and upper practical limits, respectively.

- Matching with Two Cascaded Transmission Lines: This method employs two consecutive transmission lines. The first transmission line with length l_1 and characteristic impedance Z_1, matches the rectifier impedance Z_{rect} to an intermediate impedance Z_A, according to:

$$Z_A = Z_1 \cdot \frac{Z_{\text{rect}} + jZ_1\tan(\theta_1)}{Z_1 + jZ_{\text{rect}}\tan(\theta_1)} \tag{4}$$

A second line, with characteristic impedance Z_2 and length $l_2 = \lambda/4$, is then used to match Z_A to the antenna:

$$Z_2 = \sqrt{Z_{\text{ant}} \cdot Z_A} \tag{5}$$

This technique may become impractical if Z_2 falls outside the realizable range:

$$Z_{\text{inf}} < Z_2 < Z_{\text{sup}}$$

- Stub Matching

This technique involves inserting a stub with characteristic impedance Z_s in parallel at a distance d from the rectifier. The admittance of the stub is adjusted to compensate for the reactive component of the input impedance seen from the rectifier.

This method is subject to fewer constraints, making it easier to implement.

Choice of the suitable Schottky diode

As a key component in RFEH circuits, the Schottky diode plays a critical role in determining the overall efficiency and performance of the rectifier. Its fast switching capability and low forward voltage drop make it particularly suitable for HF rectification. Consequently, careful diode selection is essential to ensure efficient RF-to-DC energy conversion. The electrical behavior of the Schottky diode is commonly represented using an equivalent circuit, as shown in Fig. 4, which provides insight into the diode operation and supports rectifier optimization.

A Schottky diode is characterized by several key parameters, including the breakdown voltage (V_{br}), series resistance (R_s), zero-bias junction capacitance (C_{j0}), and junction resistance (R_j), all of which significantly influence rectifier performance. The selection of a suitable diode is closely related to the expected RF input power level. In particular, the maximum power handling capability of the diode, given by (6), depends primarily on its breakdown voltage and the load resistance (R_L). Exceeding this limit may lead to diode breakdown and severe degradation of rectifier performance.

$$P_c = \frac{V_{br}^2}{4R_L} \tag{6}$$

The choice of Schottky diodes was driven by their low turn-on voltage, fast switching behavior, and suitability for microwave rectification. The SMS-7630 diode was selected for low-input-power operation due to its low barrier height and reduced junction capacitance, while the HSMS-2860 diode was chosen for

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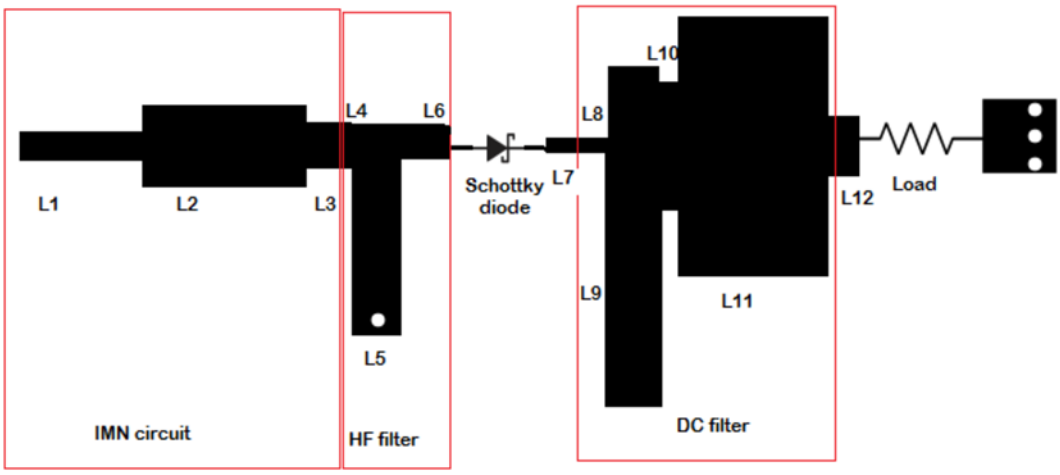


Figure 5. Low-input-power rectifier design.

high-input-power conditions because of its higher power handling capability. Other diode technologies were not considered, as they either require biasing networks or exhibit inferior performance at 3.5 GHz.

Low-input-power rectifiers (LIPRs) typically benefit from Schottky diodes with lower breakdown voltages and higher optimal load resistances, whereas HIPRs require diodes with higher breakdown voltages and lower load resistances to ensure reliable operation and high conversion efficiency.

Low-input-power rectifier

Geometrical description

A simple series rectifier is proposed for RFEH in the sub-6 GHz 5G band, specifically at 3.5 GHz, as shown in Fig. 5. The rectifier is optimized for efficient operation under low RF input power levels (below 0 dBm). The circuit is fabricated on an FR4 substrate with a thickness of 1.6 mm, a relative dielectric constant of 4.4, and a loss tangent of 0.02.

The simple series diode topology was chosen due to its ease of integration and higher conversion efficiency. Alternative architectures based on voltage multipliers or multi-stage topologies were not retained, as they generally introduce increased losses, larger circuit size, higher complexity, and reduced efficiency.

For the LIPR, the SMS-7630 Schottky diode manufactured by Skyworks is employed due to its suitability for low-power operation. This diode exhibits high sensitivity to weak RF signals owing to its low turn-on voltage of 0.34 V and a reverse breakdown voltage of 2 V. To further optimize the rectifier performance under low input power conditions, a high load resistance of 1400 Ω is selected.

To ensure optimal power flow from the antenna to the rectifier, a matching network based on transmission lines was developed and implemented. The input impedance of the rectifier was initially measured to be approximately $Z_{\text{in}} = 9.97 + j1.5\,\Omega$ at the operating frequency of 3.5 GHz. To transform this impedance to match the standard 50 Ω source impedance, a compact matching network consisting of three consecutive microstrip transmission lines in series was implemented (L1, L2, L3).

The impedance transformation using a lossless transmission line of characteristic impedance Z_0, electrical length θ, and terminated with a load Z_L, is governed by the well-known transmission line equation:

$$Z_{\text{in}}(\theta) = Z_0 \cdot \frac{Z_L + jZ_0 \tan(\theta)}{Z_0 + jZ_L \tan(\theta)}$$

Each of the three transmission lines was selected to progressively rotate the impedance toward the central region of the Smith Chart. To evaluate the impedance matching performance of the proposed rectifier, Smith Charts were used to visualize the input reflection coefficient (S_{11}) under two conditions; frequency sweep and input power variation. As shown in Fig. 6(a), the impedance is well-matched to 50 Ω at 3.5 GHz, where the normalized impedance is approximately 1.085+j0.068. This confirms that the matching network ensures efficient energy transfer at 3.5 GHz. Figure 6(b) illustrates the impact of varying input power from -20 dBm to 0 dBm on the input impedance. Despite slight variations, the impedance remains close to the central region of the Smith Chart, demonstrating the stability and robustness of the matching network for low RF power.

The optimized dimensions (lengths and widths) of the transmission lines used in the rectifier design are summarized in Table 1.

Simulation performances

Performance assessment of the designed rectifier was performed via simulation tools at 3.5 GHz, focusing on the reflection coefficient, PCE, and the resulting DC voltage spanning multiple input power values. The simulation results, as depicted in Fig. 8 reveal that the rectifier exhibits good impedance matching at 3.5 GHz (S_{11} <-30 dB). Furthermore, it is evident that LIPR presents a peak efficiency of 52.2% at –2 dBm, accompanied by a DC output voltage of approximately 0.7 V. Moreover, the PCE remains consistently above 30% over a wide RF power range (from –13 to –1 dBm), highlighting the circuit's suitability for low-power RFEH applications.

Experimental validation

To validate the performance of the proposed LIPR, experimental measurements were conducted at 3.5 GHz using a dedicated RF test setup.

The rectifier was directly connected to the measurement apparatus, and the reference plane for all measurements was defined

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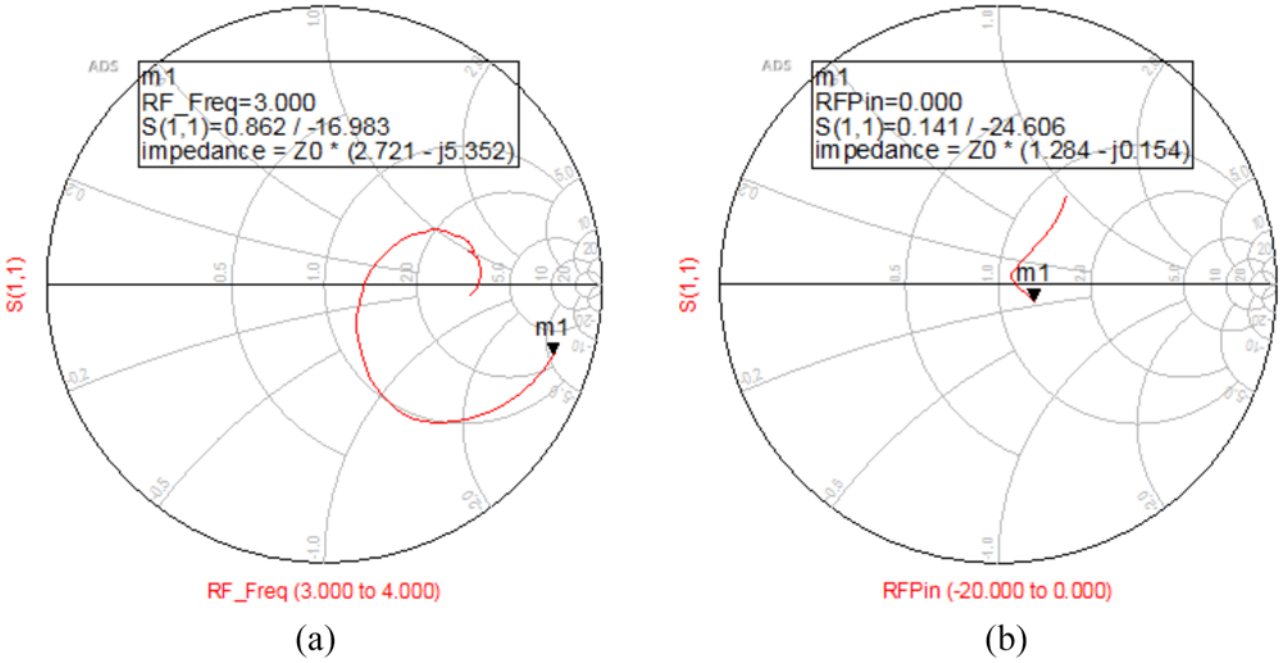


Figure 6. (a) S_{11} on a Smith Chart vs. frequency. (b) S_{11} on a Smith Chart vs. input power.

Table 1. Optimized dimensions of the transmission lines forming the proposed rectifier

Transmission line	Width (mm)	Length (mm)
L1	1	13
L2	4.8	8.6
L3	4.7	2.3
L4	3.1	3
L5	3.3	11
L6	1.8	5.7
L7	1	6.8
L8	3.4	6.6
L9	3.8	13
L10	3	3.2
L11	17	10
L12	3	3

at the SMA connector interface of the input port. No fixture de-embedding was applied. S-parameter measurements were performed using a Keysight FieldFox N9925A vector network analyzer calibrated at the SMA reference plane, while the RF input signal was generated using a Keysight N5171B RF signal generator.

The measured RF-to-DC conversion efficiency was calculated as the ratio between the DC output power and the RF input power set on the signal generator. The RF input power was swept from −20 dBm to +20 dBm in 1 dB steps. At each input power level, the DC output voltage was recorded using a digital multimeter, and the corresponding DC power was computed as $P_{DC} = V_{DC}^2/R_L$.

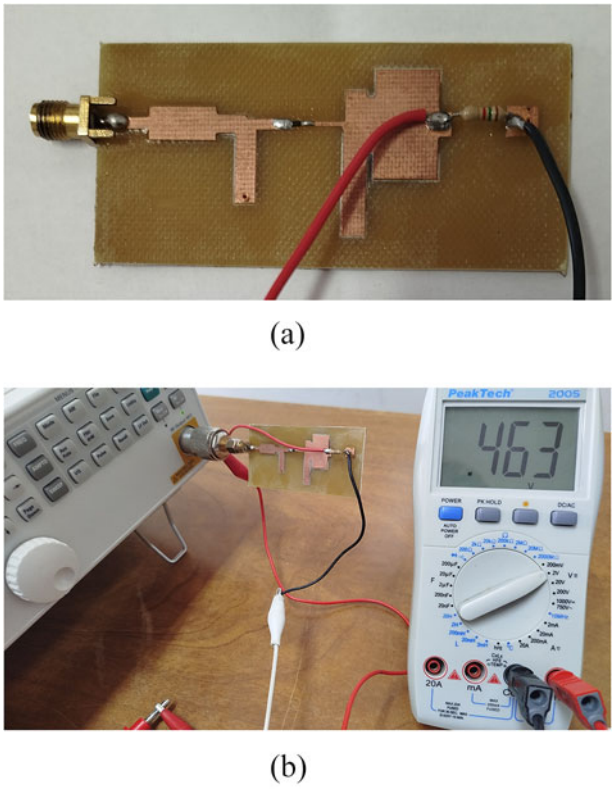


Figure 7. (a) LIPR prototype. (b) Measurement setup.

The prototype was fabricated on an FR4 substrate and experimentally evaluated under varying input power conditions, as shown in Fig. 7.

The measured results depicted in Fig. 8 confirm the trends observed in simulations. A peak RF-to-DC conversion efficiency

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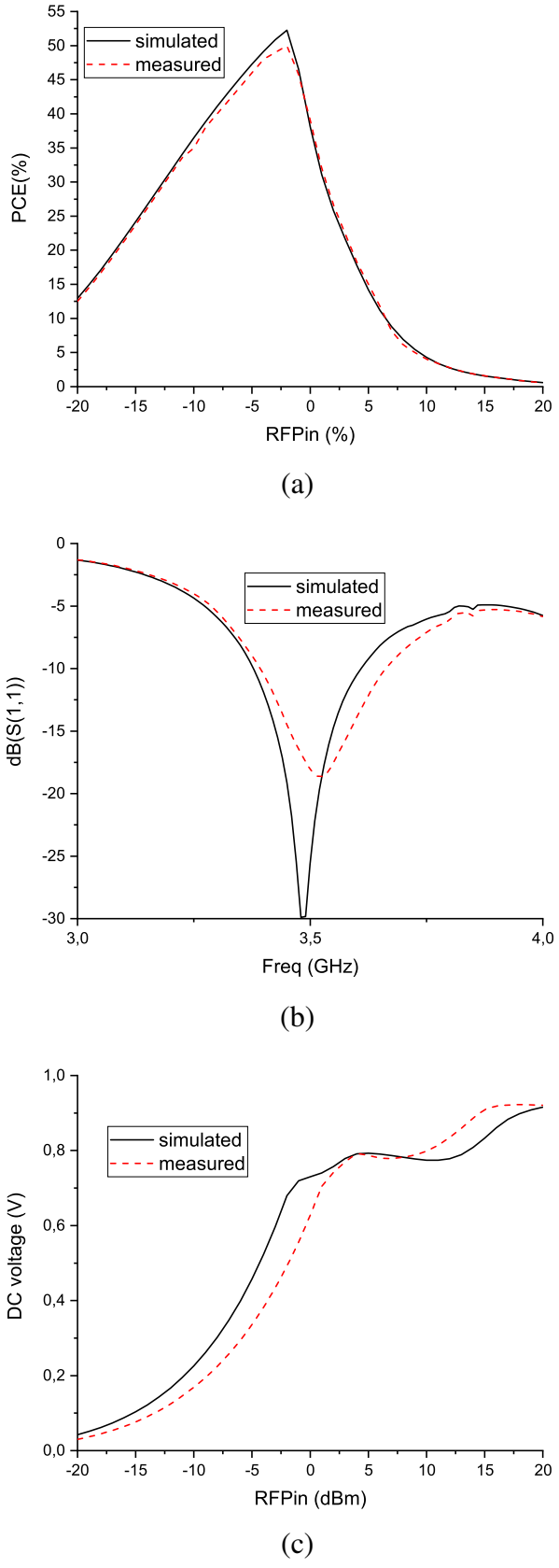


Figure 8. Simulated and measured results of the LIPR: (a) RF-to-DC conversion efficiency, (b) input reflection coefficient S_{11}, and (c) DC output voltage.

of 50.5% was achieved at an input power level of −2 dBm, corresponding to a DC output voltage of 0.7 V.

The measured results show close agreement with simulations in terms of peak efficiency and operating power range, validating the accuracy of the proposed design approach.

Minor discrepancies between simulated and measured results are mainly attributed to substrate losses, fabrication tolerances, including microstrip line dimension variations, diode parameter dispersion, fluctuations in substrate thickness and dielectric constant, as well as connector imperfections. Overall, the experimental validation confirms that the proposed rectifier operates reliably and efficiently, making it well-suited for low-power wireless energy harvesting and WPT applications targeting battery-free IoT devices and sensors.

Performance comparison and discussion

To evaluate the performance of the proposed LIPR, a comparison is conducted with representative state-of-the-art designs operating at a single frequency. Table 2 summarizes key performance metrics, including operating frequency, input power level, maximum power conversion efficiency (PCE), rectifying element, topology, and substrate. As summarized in Table 2, the proposed LIPR exhibits competitive conversion efficiency compared to state-of-the-art designs operating at similar frequencies. In particular, the proposed rectifier achieves a higher PCE at comparable or lower input power levels. This improvement is mainly attributed to the optimized series topology and the use of the SMS-7630 Schottky diode, which is well-suited for low-power rectification.

This comparison demonstrates that the proposed LIPR offers a favorable trade-off between conversion efficiency, input power sensitivity, and implementation simplicity at 3.5 GHz. The fully distributed microstrip-based design enables a compact layout and facilitates fabrication on low-cost FR4 substrates. These combined characteristics make the proposed rectifier a strong candidate for low-power RFEH applications, especially where size, cost, and integration constraints are critical.

High-input-power rectifier

Geometrical description

This rectifier (Fig. 9) is designed for WPT application. It employs the same substrate and structural configuration as used in LIPR. After evaluating the Schottky diode rectifier circuit based on the SMS-7630 for low-power systems, it becomes clear that this diode is unsuitable for high-power applications. Therefore, we propose using the HSMS-2860 diode instead. The datasheet of the HSMS-2860 diode indicates a high series resistance of 20 Ω, and a low zero-bias junction capacitance of 0.18 p. Compared to other diodes, it offers better efficiency at high power levels at the operating frequency of 3.5 GHz. It is combined with a lower load resistance of 300 Ω to ensure effective power handling and conversion efficiency at higher input power levels. Therefore, it is well-suited for high-power WPT applications.

Matching a rectifier is challenging due to the nonlinear behavior of the rectifying diode, which causes the overall circuit impedance to vary with the input power level. As a result, the output power no longer changes linearly with the input power. The maximum efficiency of a rectifier depends on both the incident power and

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Table 2. Performance comparison of state-of-the-art low-power rectifiers

Ref	Feq (GHz)	$PCE_{max}(\%)@P_{in}$	Rectifier element	Topology	Substrate
[22]	2.45	20 @ -20	HSMS-2852	Voltage doubler	FR4
[23]	3.5	43.5 @ 0	SMS-7630	Series doubler	–
[24]	0.915	20 @ -5	Two HSMS-2852	2 stage voltage multiplier	TLX8
[25]	3.5	45 @ -2	SMS-7630	Series	FR4
This work	3.5	50.5 @ -2	SMS-7630	Series	FR4

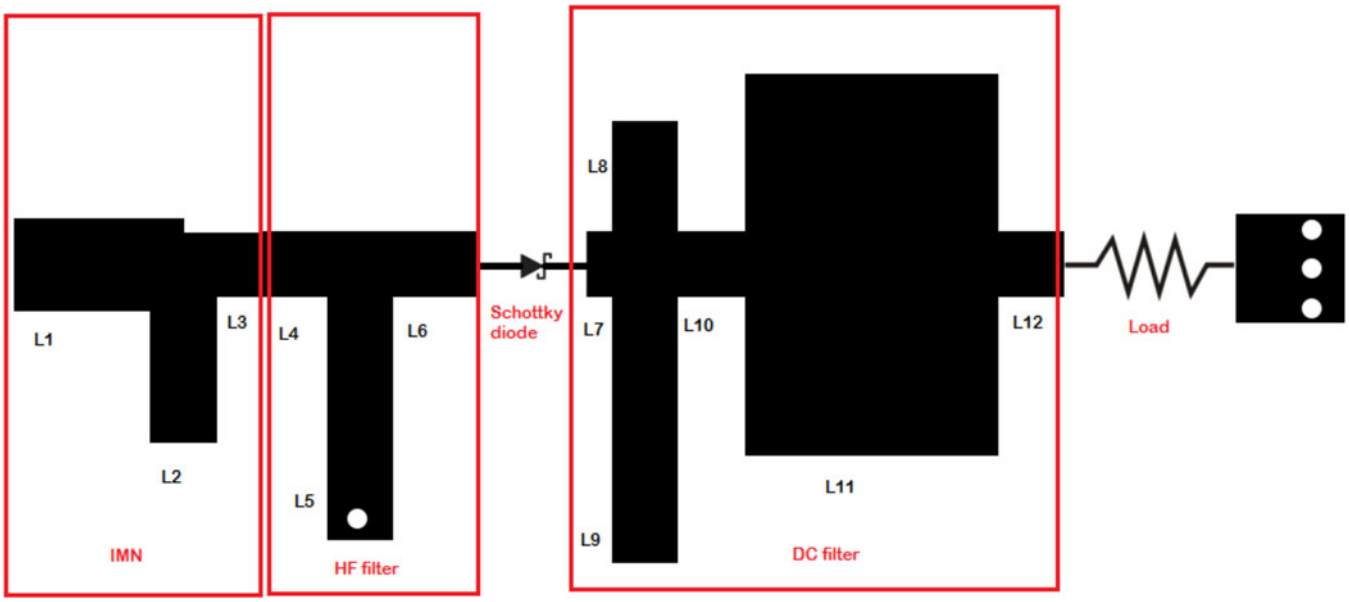


Figure 9. High-input-power rectifier design.

the load, and is achieved at a specific operating point. The matching network was designed using the "Smith Chart." The input impedance Z_{in} of the complete system (HF filter + diode + DC filter + load) was first determined. The matching circuit was then designed to transform the complex input impedance $Z_{in} = (11 + j1.5)\,\Omega$ to 50 Ω. The selected matching network consists of an open-circuited stub with a length of 6 mm and a width of 3 mm, placed at a distance of 10 mm from the HF filter.

Simulation performances

The simulation results shown in Fig. 10 confirm the effective performance of the rectifier at its operating frequency of 3.5 GHz under high input power conditions. The reflection coefficient S_{11} reaches a minimum of approximately −19 dB at 3.5 GHz, indicating excellent impedance matching between the antenna and the rectifier. This low reflection ensures that most of the incident RF power is transferred efficiently into the circuit with minimal loss. Regarding the RF-to-DC conversion, the rectifier achieves a peak efficiency of approximately 64% at an input power of 15 dBm. This high efficiency demonstrates the circuit's ability to convert a significant portion of the RF energy into DC power when subjected to strong RF signals. Additionally, the output DC voltage increases progressively with the input power, reaching a maximum of about 2.9 V at 20 dBm. This voltage level is sufficient for powering low-power electronic components or charging energy storage elements in WPT systems. These results validate the suitability of the rectifier design for high-power energy harvesting at 3.5 GHz, with optimized impedance matching, high RF-to-DC efficiency, and appropriate DC output voltage.

Experimental validation

An experimental prototype of the rectifier was fabricated to validate the simulation results (Fig. 11(a)). The circuit was manufactured using standard microstrip technology on the same substrate as used in the simulation model. The Schottky diode HSMS-2860 was selected due to its favorable characteristics for high-input-power operation.

The output DC voltage was measured across a resistive load of 300 Ω using a digital multimeter. The measured reflection coefficient exhibits a minimum of approximately −17 dB at 3.5 GHz, which is in good agreement with the simulated result, confirming effective impedance matching in the fabricated prototype. In terms of power conversion performance, the maximum measured RF-to-DC efficiency reached 61.2% at an input power of 15 dBm, closely aligning with the simulated peak efficiency. The DC output voltage increases with input power, reaching 2.68 V at 20 dBm.

These results confirm the accuracy of the simulation model and the effectiveness of the proposed rectifier design for high-input-power scenarios at 3.5 GHz. The small differences observed between simulation and measurements can be mainly attributed to dielectric losses of the FR4 substrate, conductor losses in the microstrip lines, SMA connector losses, and parasitic effects of the Schottky diodes, which are not fully captured in simulation models. At 3.5 GHz, the relatively high loss tangent of FR4 limits the

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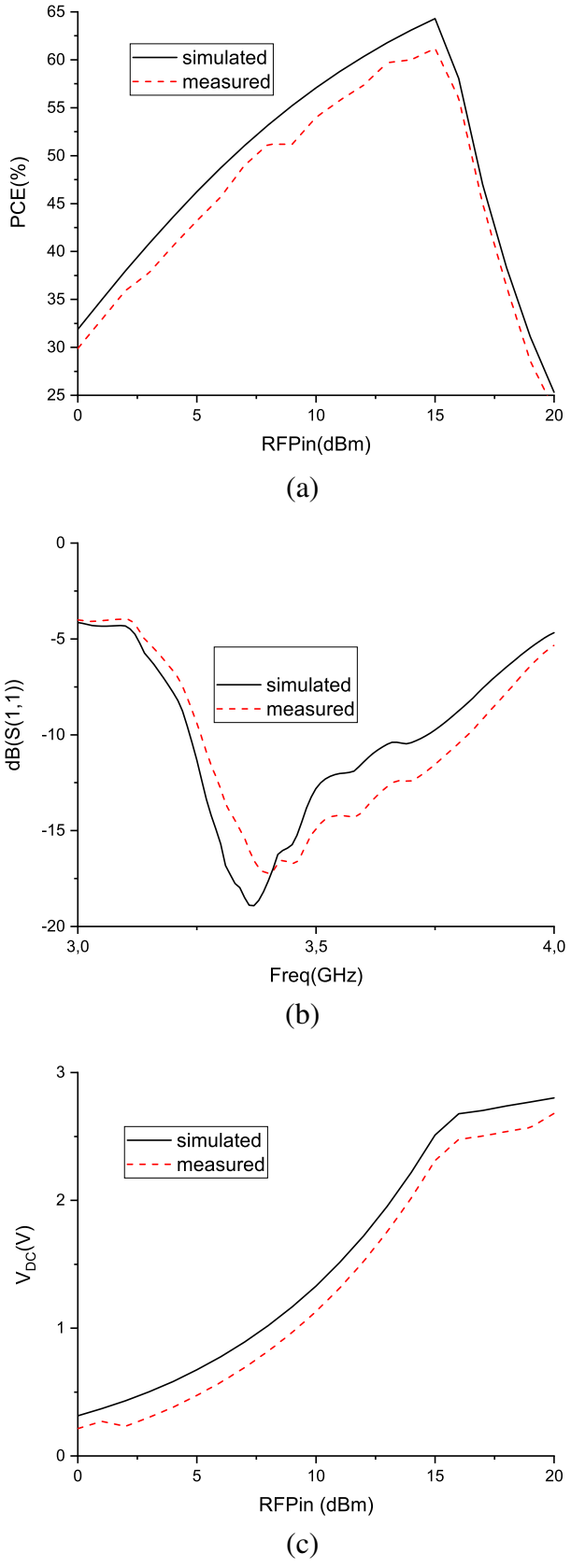


Figure 10. Simulated and measured results of the HIPR: (a) RF-to-DC conversion efficiency, (b) input reflection coefficient S_{11}, and (c) DC output voltage.

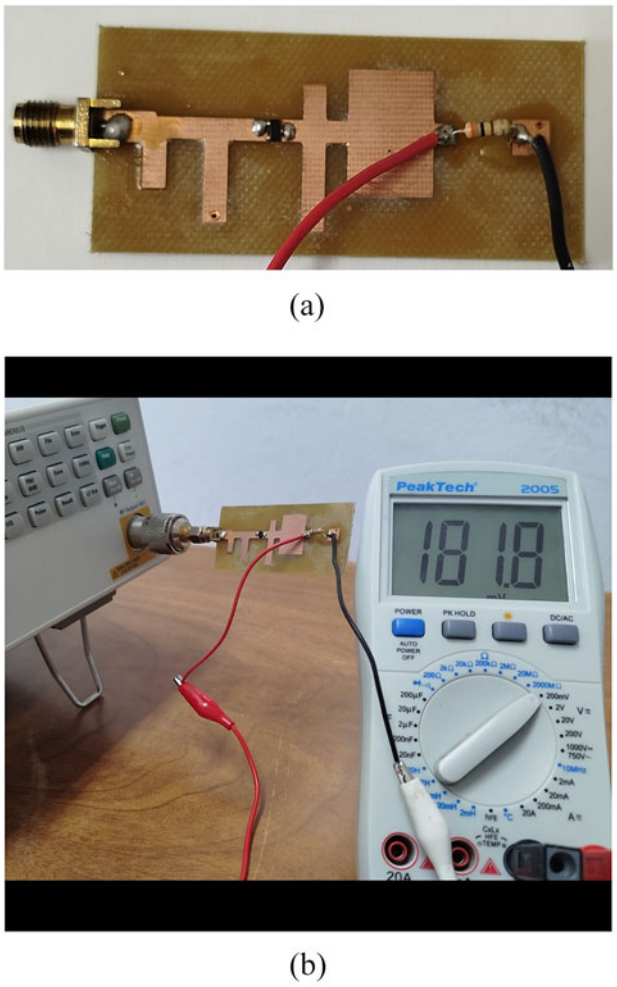


Figure 11. (a) HIPR prototype. (b) Measurement setup.

achievable peak efficiency. Future improvements could be achieved by employing low-loss substrates such as Rogers RO4350B or RO4003C, optimizing the layout to reduce parasitic inductances, and minimizing connector-related losses.

In this work, good agreement with simulations refers to the close correspondence between simulated and measured power conversion efficiency, DC output voltage, and operating input power range. The measured peak PCE values deviate from simulated results by only a few percentage points, while the overall efficiency trends versus input power are well preserved, confirming the validity of the proposed designs.

Performance comparison and discussion

To evaluate the performance of the proposed rectifier in high-power conditions, Table 3 presents a comparison with several recent high-power rectifier designs from the literature. Key parameters such as operating frequency, maximum PCE, rectifying elements, topology, and implementation details are highlighted. This comparison allows for a clear assessment of how the proposed design stands relative to other state-of-the-art solutions.

From the comparison study in Table 3, it can be clearly concluded that this rectifying circuit designed at 3.5 GHz offers several

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Table 3. Performance comparison of state-of-the-art high-power rectifiers

Ref	Feq (GHz)	PCE(%)@P_{in}	Rectifier element	Topology	Substrate
[26]	0.9	50.2 @ 14	HSMS-2850	Single stage voltage multiplier	FR4/
[27]	2.45	31.16 @ 20	HSCH-9161	Voltage doubler	–
[28]	2.4	45.22 @ 10			
	3.6	29.89 @ 5	HSMS-2820	Single stage voltage multiplier	FR4
	5	33.8 @ 25			
[24]	0.815	52 @ 10	Two HSMS-2852	2 stage voltage multiplier	TLX8
[29]	3.5	29 @ 18	–	μm GaAs and 0.18 μm Si CMOS	–
[30]	3.5	29.7 @ 6	HSMS-2860	Voltage doubler	–
This work	3.5	61.2 @ 15	HSMS-2860	Series	FR4

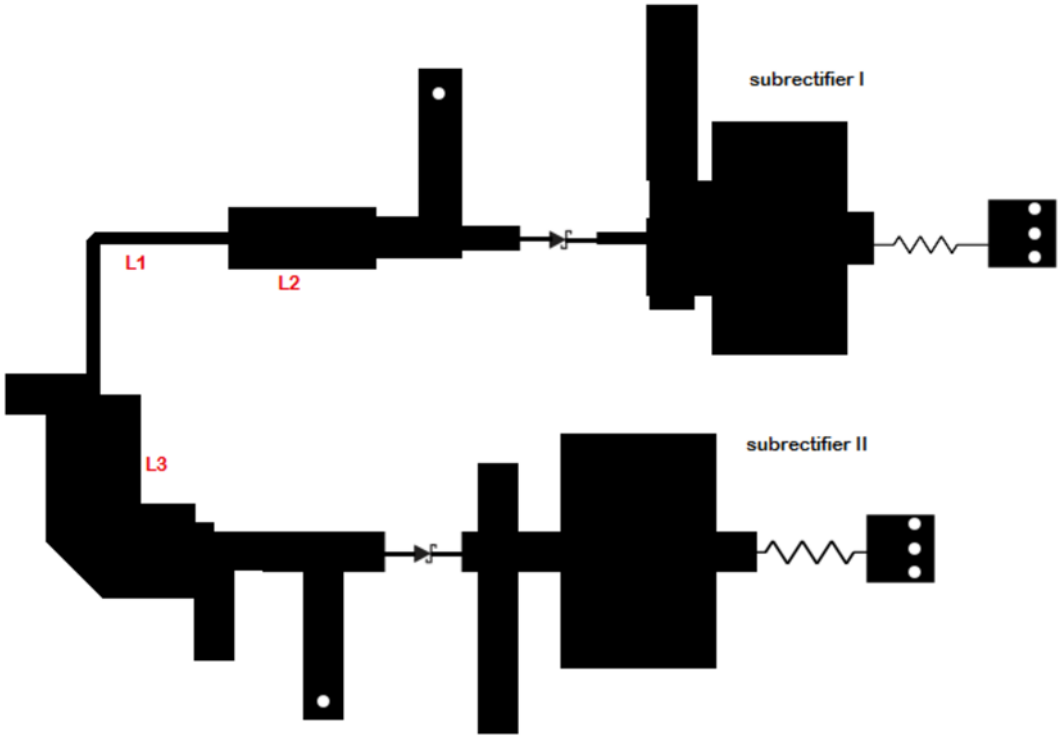


Figure 12. Wide input power range rectifier design.

key advantages for energy transfer and harvesting applications, particularly within the 5G frequency band. Implemented using microstrip technology on a low-cost FR4 substrate, the circuit employs a simple single-diode series topology, which minimizes complexity, size, and component losses. The rectifier achieves a high peak efficiency of 61.2% at 15 dBm input power with a 300 Ω load and delivers a practical DC output voltage of 2.68 V, suitable for powering low-power electronics. These characteristics position the circuit as a cost-effective and high-performance solution for 5G-enabled WPT systems.

Wide input power range rectifier

This section introduces a wide input power range rectifier (WIPRR) based on a passive DSRS concept. Unlike most wide-dynamic-range rectifiers reported in the literature, which rely on active switches, power splitters, or reconfigurable biasing networks, the proposed architecture operates fully passively. The dynamic selection of the most suitable sub-rectifier is inherently achieved through impedance adaptation, enabling efficient RF-to-DC conversion over a wide range of input power levels while preserving a simple and compact circuit topology.

The DSRS dual-path architecture consists of two sub-rectifiers optimized for different RF input power levels and directly connected to the input port. Due to their distinct impedance behaviors, the sub-rectifier best matched to the incident RF power level is naturally activated, while the other remains weakly coupled. This passive self-selection mechanism enables efficient operation over a wide input power range without the need for RF switches, power splitters, or external control circuits.

Geometrical description

In this section, a rectifier designed to operate over a wide range of RF input power levels is presented (Fig. 12). The circuit is implemented using microstrip technology and consists of two parallel sub-rectifiers, labeled I and II, directly connected to the

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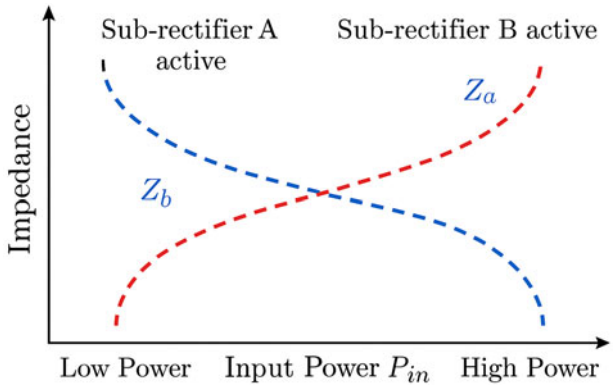


Figure 13. Impedance variation of sub-rectifiers I and II versus input RF power.

input port without any switching elements. Sub-rectifier I operates at 3.5 GHz and is optimized for low input power levels, while sub-rectifier II is designed to efficiently handle high input power conditions. Although both sub-rectifiers are based on architectures similar to those discussed in previous sections, their impedance matching networks (IMNs) have been specifically modified, and an additional matching network has been introduced to enable DSRS operation.

The IMN consists of three transmission lines, denoted as L1, L2, and L3. Transmission lines L1 and L2 are used to match sub-rectifier I to 50 Ω under low input power conditions, while presenting a high impedance at higher power levels. In contrast, transmission line L3 matches sub-rectifier II to 50 Ω at high input power and presents a high impedance under low-power operation. The impedances Z_1, Z_2, and Z_3 represent the input impedances after each respective transmission line, while Z_{in}, Z_I, and Z_{II} denote the input impedances of the overall system, sub-rectifier I, and sub-rectifier II, respectively.

Using transmission line theory, the following equations are derived:

$$Z_2 = Z_{\text{L2}} \cdot \frac{Z_I' + jZ_{\text{L2}} \tan(\theta_{\text{L2}})}{Z_{\text{L2}} + jZ_I' \tan(\theta_{\text{L2}})} \tag{7}$$

$$Z_I = Z_{\text{L1}} \cdot \frac{Z_2 + jZ_{\text{L1}} \tan(\theta_{\text{L1}})}{Z_{\text{L1}} + jZ_2 \tan(\theta_{\text{L1}})} \tag{8}$$

$$Z_{II} = Z_{\text{L3}} \cdot \frac{Z_{II}' + jZ_{\text{L3}} \tan(\theta_{\text{L3}})}{Z_{\text{L3}} + jZ_I' I \tan(\theta_{\text{L3}})} \tag{9}$$

The input power P_{in} represents the total RF power delivered to the rectifier network, while P_I and P_{II} denote the power allocated to sub-rectifiers I and II, respectively. The DSRS consists of activating only one sub-rectifier depending on the input RF power level, and delivering the maximum available power (P_{in}) to it, as illustrated in Fig. 13, which depicts the variation of input impedance for sub-rectifiers I and II as a function of input RF power.

At low power levels, the primary objective is to direct the maximum input power to the low-power sub-rectifier I. To achieve this, the input impedance Z_I must be matched to the source impedance Z_G, while the input impedance Z_{II} must present a very high value. Conversely, at high power levels, the goal is to route the entire input power to sub-rectifier II. In this case, Z_{II} must be matched to the source impedance, effectively deactivating sub-rectifier I, which now presents a high input impedance.

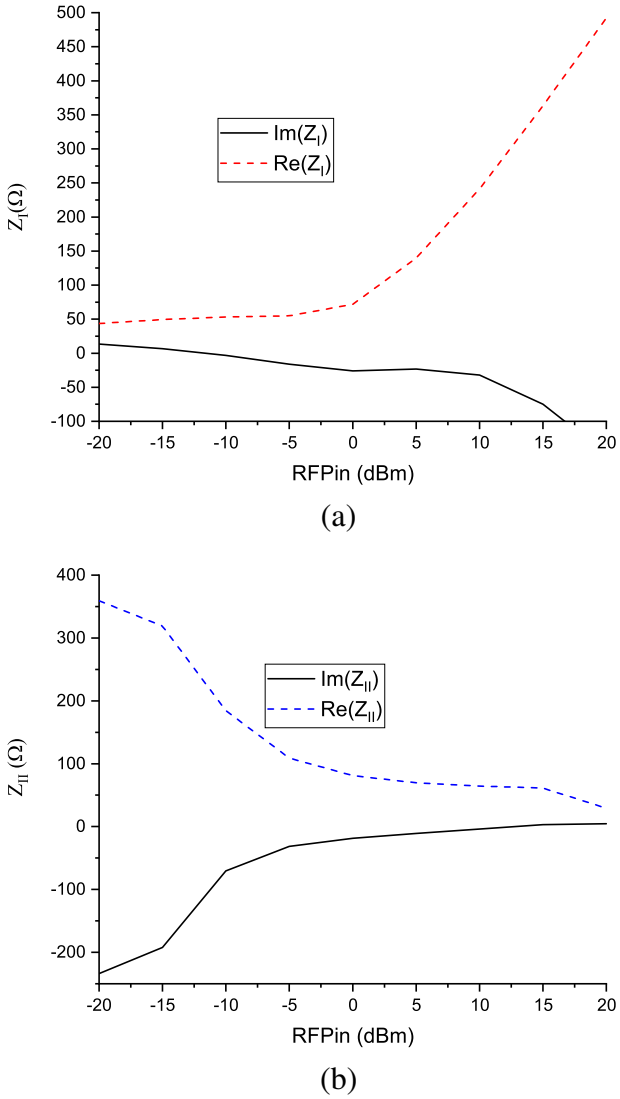


Figure 14. Simulation results of WIPRR. (a) Z_I vs P_{in}. (b) Z_{II} vs P_{in}.

Simulation performances

The performance of the proposed WIPRR is evaluated in terms of input impedance (Z_{in}), reflection coefficient (S_{11}), and RF-to-DC conversion efficiency.

Input impedance

The input impedances as a function of the RF input power for sub-rectifiers I and II are shown in Fig. 14(a) and 14(b), respectively.

Between -20 dBm and 0 dBm of RF input power, the input impedance Z_I remains approximately equal to 50 Ω; however, it behaves as a high impedance for $P_{\text{in}} > 0$ dBm. Conversely, the input impedance Z_{II} of sub-rectifier II is nearly 50 Ω for P_{in} above 0 dBm, while it becomes very high for input power levels between -20 dBm and 0 dBm. These simulation results confirm that DSRS aligns with the behavior of the proposed rectifier. Depending on the RF power level, one sub-rectifier serves as the main energy harvester while the other is effectively deactivated.

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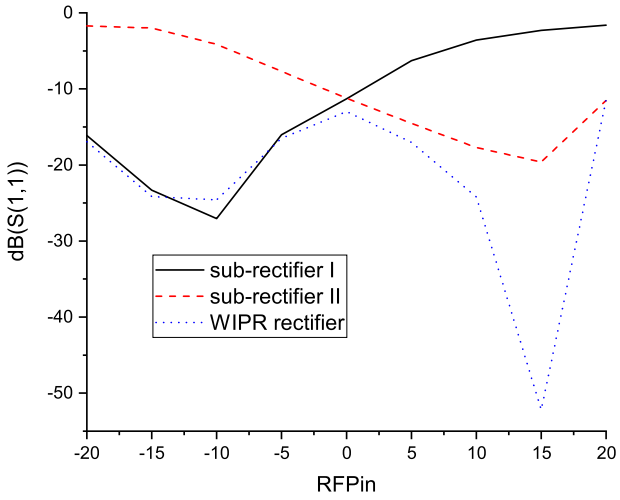


Figure 15. Reflection coefficient S_{11} versus input RF power.

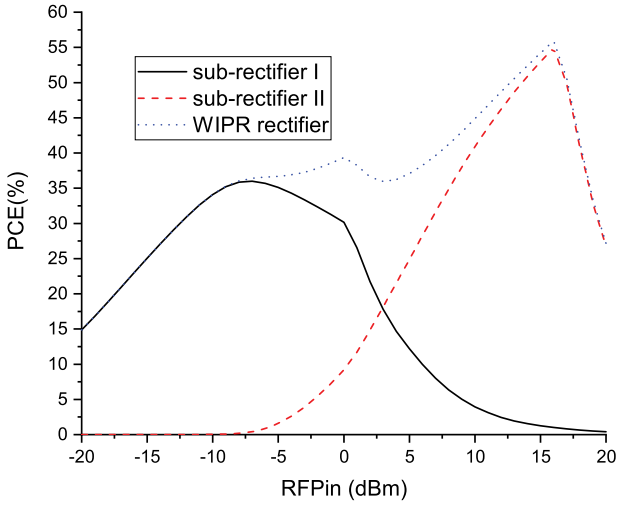


Figure 16. RF-DC power conversion versus input RF power.

Reflection coefficient

Figure 15 illustrates that sub-rectifier I is well matched for input power levels between -20 dBm and 0 dBm. Conversely, sub-rectifier II shows good matching for input powers above 0 dBm, where S_{11} consistently remains below -10 dB. Overall, the proposed WIPRR achieves good impedance matching across both low and high power levels.

RF-to-DC conversion efficiency

Figure 16 shows the RF-to-DC conversion efficiency as a function of the RF input power at 3.5 GHz. Sub-rectifiers I and II achieve peak efficiencies of 35% at -7 dBm, 40% at 0 dBm, and 56% at 16 dBm, respectively. The proposed WIPRR maintains an efficiency above 20% over a 38 dB range (from -16.5 dBm to 21.5 dBm), reaching 56% and 40% at 16 dBm and 0 dBm, respectively. In addition, the reflection coefficient remains below -10 dB across a 42 dB input power range.

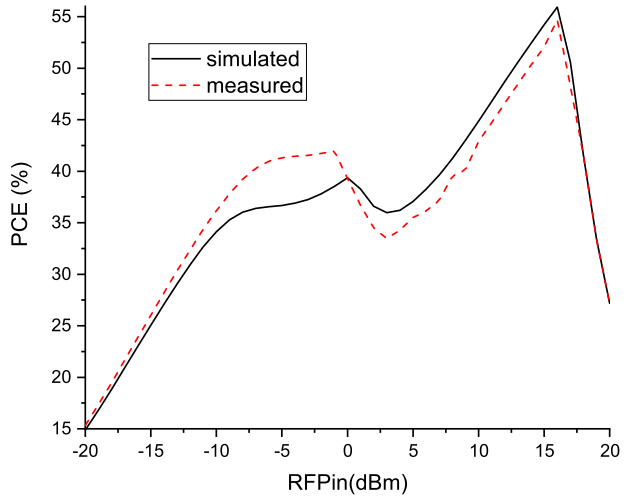


Figure 17. Simulated and measured PCE of the proposed WIPRR at 3.5 GHz.

Experimental validation

The proposed WIPRR was fabricated using microstrip technology on a FR4 substrate. Precision connectors and ground vias were implemented to ensure accurate measurement and stable RF performance. The prototype (Fig. 18) was tested using VNA to measure the input reflection coefficient (S_{11}), and a power source combined with a digital multimeter to evaluate the DC output voltage and compute the RF-to-DC conversion efficiency. All measurements were carried out at a frequency of 3.5 GHz.

The experimental results are in good agreement with the simulation data, validating the design approach and the effectiveness of the DSRS technique. Figure 17 compares the simulated and measured RF-to-DC conversion efficiency across a wide range of input power levels at 3.5 GHz. The measured results closely follow the simulated curve, with minor discrepancies attributed to fabrication tolerances and measurement setup losses. The measured maximum PCE is 54.7% at 16 dBm, and it remains as high as 42% at -2 dBm. The rectifier exhibits an extended input power range of 41 dB (from -18 dBm to 23 dBm), over which the PCE consistently remains above 20%. The overall trend confirms the rectifier's ability to maintain high efficiency over a broad input power range, validating the effectiveness of the proposed design.

Performance comparison and discussion

As shown in Table 4, the proposed design achieves a peak RF-to-DC conversion efficiency of 54.7% at 16 dBm and maintains an efficiency above 20% over an exceptionally wide 41 dB input power range, from −18 dBm to 23 dBm, at 3.5 GHz.

Beyond peak efficiency values, a normalized comparison highlights the effectiveness of the proposed approach. When considering the trade-off between the achieved RF input power range and circuit complexity, the proposed DSRS-based rectifier offers a superior balance compared to previously reported designs summarized in Table 4. While several state-of-the-art rectifiers achieve high peak efficiency, their efficient operation is typically confined to a much narrower input power window. In contrast, the proposed rectifier maintains competitive efficiency over a significantly wider dynamic range at a comparable operating frequency, providing a more robust solution for practical RFEH applications.

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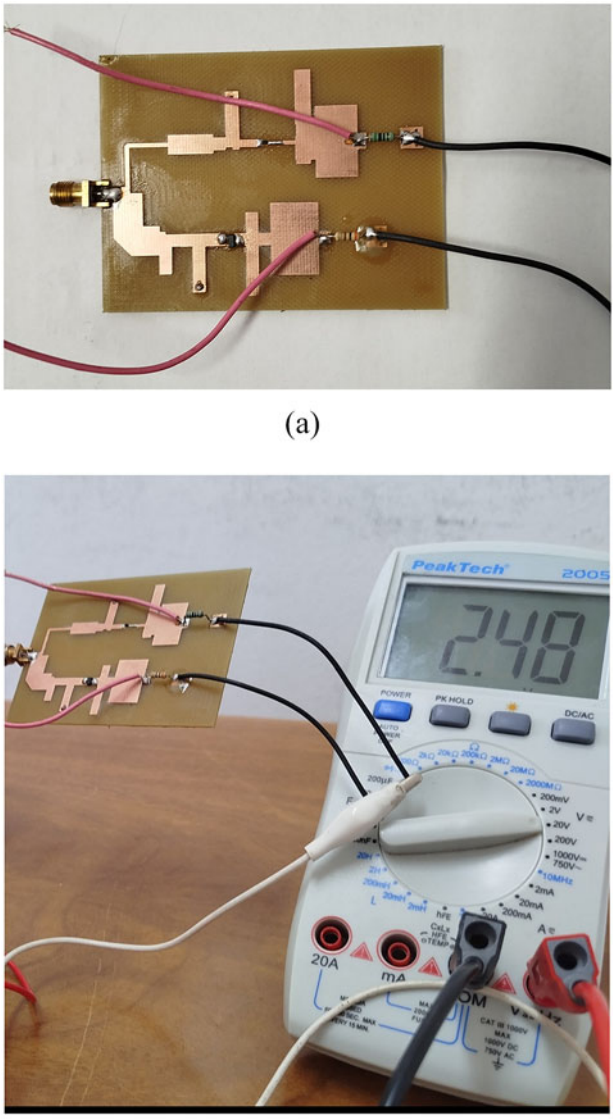


Figure 18. (a) WIPR prototype. (b) Measurement setup.

This performance is enabled by an innovative DSRS-based dual-path architecture employing two sub-rectifiers directly connected to the input without power splitters, T-junctions, or RF switches. The dynamic selection of the active sub-rectifier is achieved fully passively through impedance adaptation, allowing efficient operation across a much wider input power range than conventional single-path rectifiers. As a result, the proposed rectifier significantly reduces insertion losses and circuit complexity while preserving high conversion efficiency. To the best of the authors' knowledge, no prior work has reported such a wide input power range at 3.5 GHz, highlighting the novelty and practical relevance of this approach for compact RF front-ends in 5G-enabled IoT and WPT applications.

Conclusion

This work presented several RF-to-DC rectifier circuits optimized for different input power levels using microstrip-based matching networks. A high-power rectifier achieved 2.8 V and 64% efficiency at 15 dBm, while a low-power design reached 52% efficiency at −2 dBm.

In addition, a WIPRR based on a fully passive DSRS dual-path architecture was proposed, enabling efficient operation over a significantly wider input power range than conventional single-path rectifiers at similar frequencies. This design maintains over 30% efficiency from −12.5 dBm to 19.7 dBm, with a peak of 55.5% at 16 dBm.

By combining a very wide input power dynamic range, high conversion efficiency, and low circuit complexity without RF switches or active control circuits, the proposed rectifier represents a clear advancement over the state of the art at 3.5 GHz.

The proposed converters are well-suited for 5G RFEH and WPT applications involving highly variable RF power levels, such as energy-autonomous IoT nodes.

Future work will focus on system-level integration and deployment in wearable, biomedical, and 5G-enabled energy-autonomous platforms.

Table 4. Performance comparison of state-of-the-art wide input power range rectifiers

Ref	Feq (GHz)	$PCE_{max}(\%)@P_{in}$	Power dynamic rectifier extension technique	Input power band with PCE$>$ 20% (dB)
[31]	0.820	39 @ -5	Reconfigurable	14
[32]	2.4	47.1 @ -6	Resistance compression	16
[33]	0.902	33 @ -8	Reconfigurable	13
[34]	0.953	47.87 @ -19	Dual input	25
[35]	0.896	43 @ -11	Optimum voltage compensation	8.5
This work	3.5	54.7 @ 16	DSRS	41

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Competing interests. The author(s) declare none.

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Mounira Ben Yamna is an engineer specializing in communications and networks, having graduated from the National Engineering School of Gabes, Tunisia, in 2012. She holds a Master's degree in Embedded Electronics and Communication Systems from the Higher Institute of Computer Science in Medenine, Tunisia. She received her Ph.D. degree in Electrical Engineering, with research focused on RF energy harvesting and rectenna systems. Her research focuses on antenna, rectenna, and energy harvesting.



Nabil Dakhli He received the M.Sc. degree in Electrical Engineering from Tunis University in 2005 and the Ph.D. degree from the Higher School of Communication of Tunis in 2014. He is currently an Associate Professor at the High Institute of Computing of Medenine, Tunisia. His research interests include antennas, metamaterials, and RF/microwave circuit design for energy harvesting and sensing applications.



Hedi Sakli He received the M.S. degree in high-frequency communication systems from Marne-La-Vallée University, France, in 2002, and the Ph.D. and H.D.R. degrees in telecommunications from the National Engineering School of Tunis, Tunisia, in 2009 and 2014, respectively. He has been a Professor at the university of Gabes since 2022. His research interests include propagation in anisotropic media, metamaterials, antennas, sensors, 5G systems, IoT, and AI.

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