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Modified Y-junction SIW power divider/combiner circuit

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Research Paper

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Abstract

A modified compact Y-junction substrate-integrated waveguide (SIW) four-way power divider (PD)/combiner is proposed in this paper. The proposed approach is based on the traditional Y-junction waveguide. By using direct transition structure from SIW to half-mode SIW, four-way PD that provides equal power split to all four output ports is achieved. The even- and odd-mode equivalent circuits are given to analyze and design the PD. The measured results validate the proposed design methodology and show good agreement with the simulation results. The measured 17 dB return loss bandwidth and 1.2 dB insertion loss bandwidth of this four-way PD are both about 2.5 GHz.

Introduction

Power divider (PD) is one of the most important passive circuits and is widely used in microwave circuits [1–18]. Since the PD has been proposed, great interest has been aroused in developing various kinds of power-dividing/combining circuits, such as waveguide PDs [1–3], planar PDs [4–13], and substrate-integrated waveguide (SIW) PDs [14–18]. SIW techniques are attractive for the design of microwave and millimeter-wave components, due to their high Q factor, low cost, and high integration capability. The half-mode SIW (HMSIW) has been developed in recent years [19–21]. Compared with the SIW, HMSIW is a newly proposed planar structure that keeps the advantages of SIW but the size is nearly half reduced. In [22], a Y-junction four-way PD is proposed by integrating the SIW PD and the HMSIM PD.

In this paper, a modified four-way Y-junction PD/combiner that is based on the traditional Y-junction structure is proposed. The proposed divider/combiner is a five-port structure and is capable of producing equal power ratios. The simulated and measured results show that the insertion loss is <1.2 dB for each of the four output ports from 4.5 to 7.0 GHz. The proposed divider/combiner exhibits better than 17 dB return loss with more than 13 dB isolation between adjacent ports in the same frequency range. The theory and design of the proposed PD/combiner are given. The proposed four-way PD is fabricated and measured. The measured results agree with the simulated ones closely.

Analysis of PD/combiner circuit

The topology of the modified Y-junction PD/combiner circuit is shown in Fig. 1. The circuit consists of three parts: a Y-junction structure based on SIW and two identical two-way HMSIW PDs. The signal through which the Y-junction structure is divided into two paths and then four output ports is achieved by HMSIW dividers. To improve the isolation between the four output ports, the isolation resistors are set between the two adjacent HMSIW. In addition, only a single substrate is used in the PD/combiner circuit; on the one hand, it is easy to install the isolation resistor, and it can improve the reliability of the circuit.

As can be seen, the modified four-way Y-junction PD/combiner is symmetrical, so the even- and odd-mode equivalent circuit analysis can be used. The equivalent circuit of the circuit is shown in Fig. 2. Under the even-mode excitation, a bisection of the PD is shown in Fig. 2(a). Z_0 and Z_1 are the characteristic impedance of microstrip line and SIW. The characteristic impedance of the taper-shaped transition at x can be derived as [23]:

$$Z_{T(x)} \frac{120\pi}{\sqrt{\varepsilon_e}[(w_1(x)/d) + 1.393 + 0.677\ln((w_1(x)/d) + 1.444)]}, \tag{1.a}$$

where

$$w_1(x) = \frac{x(w_4 - w_3) + w_3 t_2}{t_2}, \tag{1.b}$$

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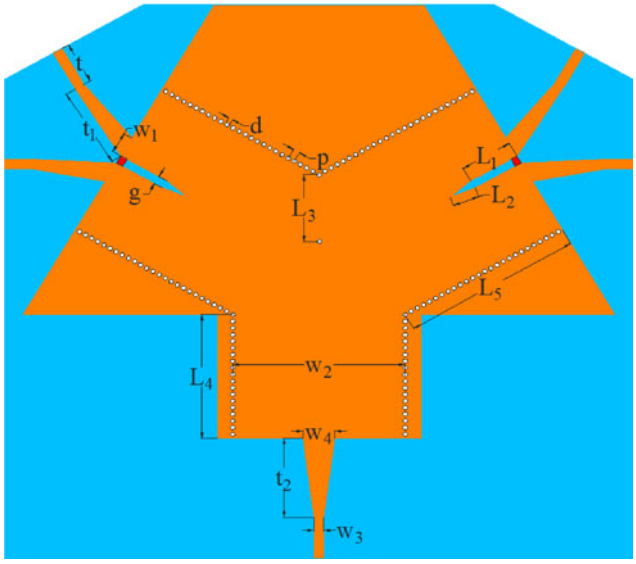


Fig. 1. Topology of modified four-way Y-junction SIW power divider/combiner circuit.

d is the height of the substrate; ε_e is the relative permittivity; t_2 is the length of the taper; w_3 and w_4 are the widths of the taper, as shown in Fig. 1. The quarter wavelength taper is sufficient to obtain a good return loss. In any case, taper lengths must be chosen as a multiple of a quarter of a wavelength in order to minimize the return loss. The transmission parameters of a linear tapered TEM transmission line are already known analytically [24] and the widths w_3 and w_4 can be achieved. These equations are used to verify the return loss of the taper over the full bandwidth. According to the end of the taper, the reflection coefficient and the input impedance can be derived as:

$$\Gamma_{\text{in1}} = \frac{1}{2}\int_0^{t_2} e^{-j2\beta x}\frac{d[\ln 2Z_T(x)]}{dx}dx + \Gamma_L, \tag{2.a}$$

$$Z_{in1} = \frac{(1+\Gamma_{in1})2Z_1}{(1-\Gamma_{in1})}. \tag{2.b}$$

Thus, the input impedance of the Y-junction Z_{in2} and the input impedance Z_{ine} can be, respectively, derived as:

$$Z_{in\,2} = 2Z_1\frac{Z_{in1} + 2jZ_1\tan\theta_1}{2Z_1 + jZ_{in\,1}\tan\theta_1}, \tag{3.a}$$

$$Z_{ine} = \frac{Z_{in\,2}}{1 + jBZ_{in\,2}}. \tag{3.b}$$

When part A is matched, the total input impedance of the part A circuit is equal to Z_1. The good impedance match can be achieved when:

$$B = \frac{1}{jZ_1} - \frac{2Z_1 + jZ_{in1}\tan\theta_1}{2jZ_1(Z_{in1} + 2jZ_1\tan\theta_1)}. \tag{4}$$

When part A is matched, the total input impedance of the part A circuit is equal to Z_1. The good impedance match can be achieved when:

$$Z_{ine} = Z_1. \tag{5}$$

A centrally located via acts as an inductive matching post to nullify the effect of the Y-junction capacitance and therefore promoting lower return loss at the input. The parameter "w_2" determines the propagation constant of the fundamental mode, the diameter of via-holes "d", and the pitch length of via-holes "p" are set to minimize the radiation loss and the return loss. The "d" and "p" can be achieved according to [25] and the dielectric constant in the frequency normalization allows an almost direct design of SIW junctions using any substrate by determining w_2. The results are valid in the following range [26]:

$$0.65 < w_2\sqrt{\varepsilon_r}/\lambda < 0.92. \tag{6}$$

Furthermore, it can be found from Fig. 2(a) that part A of the even-mode equivalent circuit can be further analyzed by even and odd modes. The even- and odd-mode equivalent circuits of part A are shown in Fig. 3. As we can see from Fig. 3(a), in the even-mode equivalent circuit, no current flows through the isolation resistor. Thus, the input impedance and reflection coefficient, which are seen from the end of the HMSIW, can be derived as:

$$Z_{in\,3} = Z_2\frac{2Z_1 + jZ_2\tan\theta_3}{Z_2 + 2jZ_1\tan\theta_3}, \tag{7.a}$$

$$\Gamma_{in\,3} = \frac{Z_{in\,3} - Z_{T1}(0)}{Z_{in\,3} + Z_{T1}(0)}. \tag{7.b}$$

The characteristic impedance of the taper-shaped transition at x in the odd-mode equivalent circuit can be derived as [23]:

$$Z_{T1}(x) = \frac{120\pi}{\sqrt{\varepsilon_e}[(w_2(x)/d) + 1.393 + 0.667\ln((w_2(x)/d) + 1.444)]}, \tag{8.a}$$

where

$$w_2(x) = \frac{t_1 w_1 - (w_1 - w_3)x}{t_1}, \tag{8.b}$$

t_1 is the length of the output taper, and w_1 and w_3 are the widths of the taper, as shown in Fig. 1. Seen from the end of the taper, the reflection coefficient and the input impedance can be derived as:

$$\Gamma_{\text{in}} = \frac{1}{2}\int_0^{t_1} e^{-j2\beta x}\frac{d[\ln Z_{T1}(x)]}{dx}dx + \Gamma_{\text{in3}}, \tag{9.a}$$

$$Z_{in} = \frac{(1+\Gamma_{in})Z_0}{(1-\Gamma_{in})}. \tag{9.b}$$

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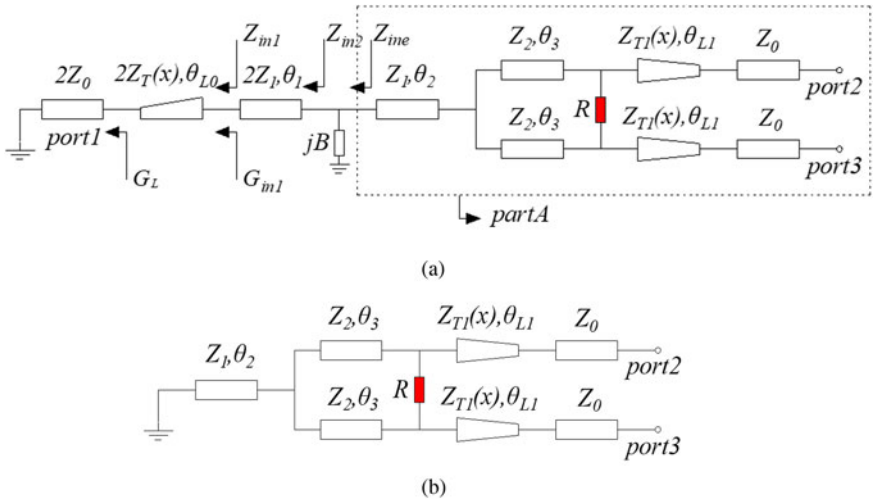


Fig. 2. Equivalent circuit model of broadband-modified four-way Y-junction power divider/combiner circuit: (a) even-mode equivalent circuit; (b) odd-mode equivalent circuit.

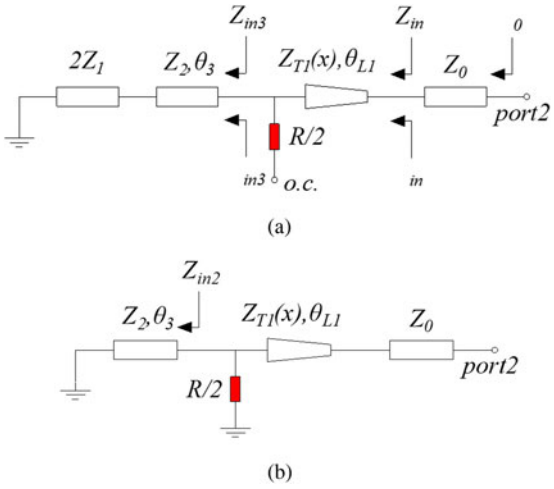


Fig. 3. Equivalent circuit model of part A: (a) even-mode equivalent circuit of part A; (b) odd-mode equivalent circuit of part A.

The reflection coefficient at the port 2 can be derived as:

$$\Gamma_0 = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} = \Gamma_{in}. \tag{10}$$

Therefore, the reflection coefficient of the port 2 can be determined by the above equations, when the port 2 reflection coefficient Γ_0 is given. The parameters of microstrip transition can be obtained [24]. As shown in Fig. 3(b), in order to achieve the impedance match, the circuit must satisfy:

$$\frac{Z_{in2}(R/2)}{Z_{in2} + R/2} = Z_{T1}(0), \tag{11.a}$$

where

$$Z_{in2} = jZ_2 \tan\theta_3. \tag{11.b}$$

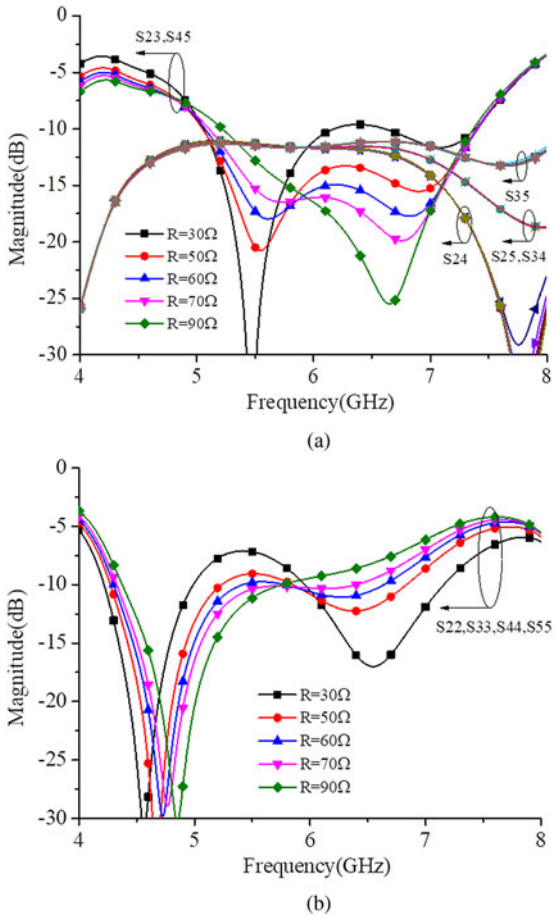


Fig. 4. Effect of isolation resistor on circuit isolation and output VSWR: (a) effect on isolation; (b) effect on output VSWR.

Thus, the isolation resistor must satisfy:

$$R = \frac{2Z_{in2}Z_{T1}(0)}{Z_{in2} - Z_{T1}(0)}, \tag{12.a}$$

when $\theta_3 = \frac{\pi}{2}$, $Z_{in2} = \infty$. By equation (12.a), resistor can be

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Table 1. Values of parameters of circuit

L_1	L_2	L_3	L_4	L_5	W_1	W_2	W_3
6	3.04	8.09	14.9	20.5	2.5	19.5	1.11
$W4$	T	t_1	t_2	d	P	g	
3.6	5	9.57	9.5	0.5	0.8	1	

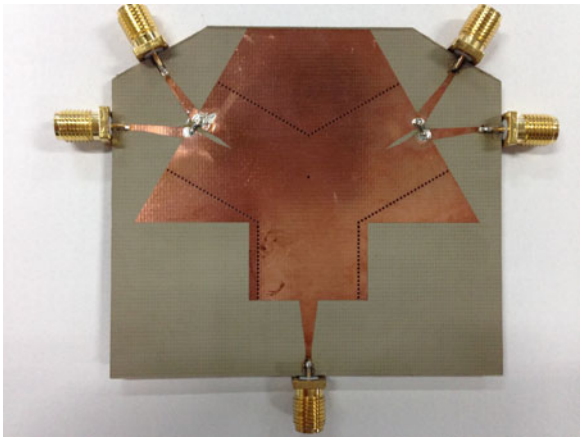


Fig. 5. Photograph of the broadband-modified four-way Y-junction power divider/combiner circuit.

expressed as:

$$R = 2Z_{T1}(0). \tag{12.b}$$

The value of isolation resistor can be determined by equation (12.b). After the initial width of the taper w_1 1 is determined. The $Z_{T1(0)}$ and the value of isolation resistor can be determined. The slot can be determined according to [27].

The correctness of above deduction can be verified by the simulation results of the circuit. The relationship between resistor and isolation or return loss when $w_1 = 2.5$ mm is shown in Fig. 4, when the value of isolation resistor is about 50–60 Ω, the isolation and the VSWR bandwidth are better. When $w_1 = 2.5$ mm, the $Z_{T1}(0) \approx 28.9\ \Omega$ and $R = 57.8\ \Omega$. The simulation and measurement results show good agreement. The final value is $R = 51\ \Omega$.

Summary of the total design procedure

(a) The width of the 50 Ω transmission line w_3 can be determined by the theory of transmission lines and the width of the microstrip taper w_1 and w_4 can be determined by equations (1) and (8) according to [23].

(b) The taper lengths t_1 and t_2 should be chosen as a multiple of a quarter of a wavelength in order to minimize the return loss. The analytical equations presented in [24] are applied to find the length that minimizes the return loss over the full bandwidth.

(c) The diameter of via-holes "d" and the pitch length of via-holes "p" are determined according to [25], and the equivalent width of the SIW w_2 can be determined by equation (6) and the inductive post can be generated with the use of an FEM software package according to [26].

(d) The gap between the HMSIWs is an important design factor, the length of the gap L_1, L_2, and the width of the gap g can be determined according to [27] and the resistance can be determined by equation (12)

(e) When the initial parameters are obtained according to the aforementioned design procedure, the proposed PD can be constructed and optimized in 3D electromagnetic simulation tools (such as Ansoft-High Frequency Structure Simulator (HFSS)). Then, the optimized structural dimensions can also be obtained.

Simulation and realization of PD/combiner circuit

The broadband-modified four-way Y-junction PD is fabricated with a two-layer substrate Taconic RF-35 with a dielectric constant ε_r of 3.5, a thickness of 0.508 mm, and a loss tangent of 0.0018. Figure 5 gives the fabricated broadband four-way Y-junction PD, and the final optimized circuit size is shown in Table 1.

The simulated and measured results are shown in Fig. 6. It can be seen from Fig. 6(a), the center frequency of the circuit is 5.75 GHz. The simulated input return loss is larger than 15 dB, and the measured one is larger than 17 dB in a frequency range of 4.5–7 GHz. Equal power division for simulated results is achieved around 4.5–7 GHz, while the measured insertion losses are around 1.2 dB, and amplitude unbalance is about ±0.25 dB in the same frequency range. The measured results of phase relationship among output ports are shown in Fig. 6(b); it can be seen that the measured phase unbalances are ±2° from 4.5 to 7 GHz. In addition, the simulation and measured results of the isolation and the output VSWR are shown in Figs 6(c) and 6(d); it can be seen that the isolation of adjacent output ports (such as ports 2, 3 and ports 4, 5) is more than 13 dB. It is better than the non-adjacent ports isolation, which is more than 11 dB across the band 5.2–7 GHz. The better isolation is caused by isolation resistors that are loaded between the adjacent ports. As we can see from Fig. 6(d), the simulation and measured results of the output return loss are both better than 15 dB. The measured results are in good agreement with the simulated ones, and the small difference between the two is mainly caused by the manufactural error. The increase of the insertion loss is mainly caused by the conductor loss of the substrate and the loss of the SMA joint.

Conclusion

In this paper, a broadband-modified four-way Y-junction SIW PD/combiner based on the traditional Y-junction waveguide is proposed. The broadband equal power ratio is achieved by using direct transition structure from SIW to HMSIW. The isolation and the VSWR bandwidth are improved by loading the isolation resistor between HMSIW in the output ports. The design is analyzed by the even- and odd-mode analysis method. The measured average insertion loss of the broadband-modified

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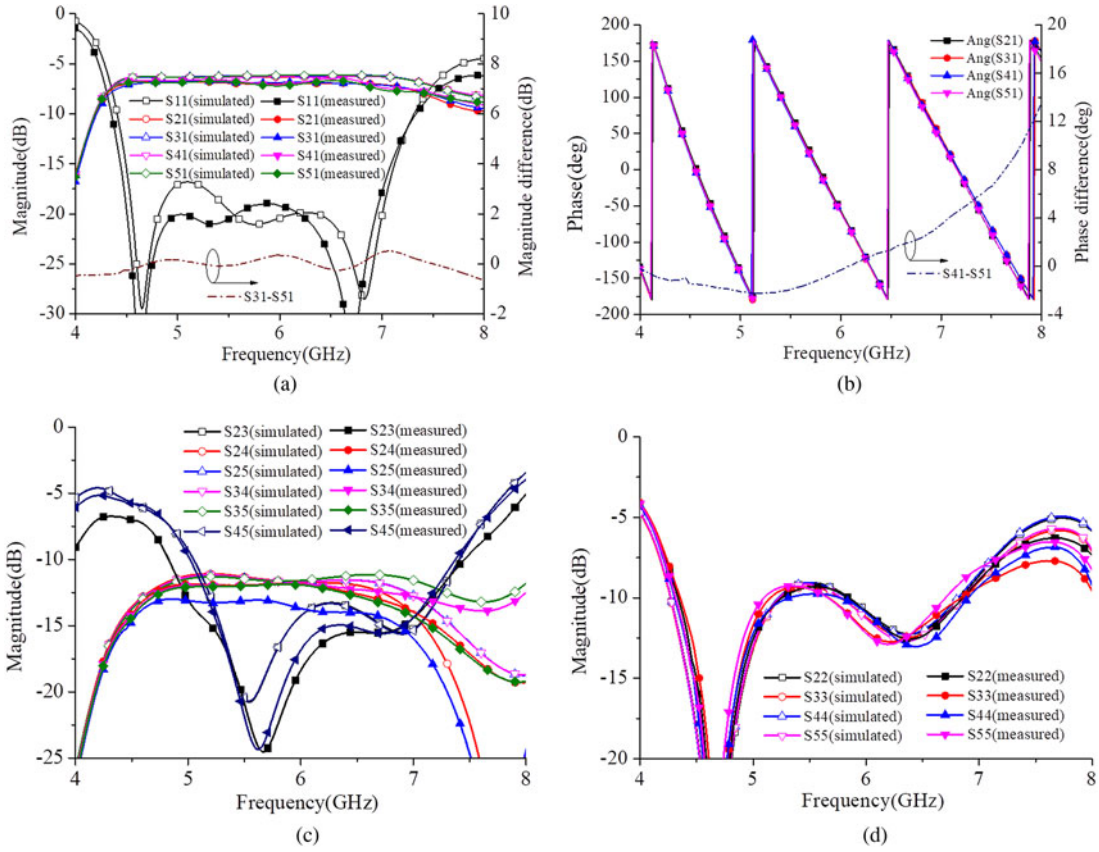


Fig. 6. Simulation and test results of broadband-modified four-way Y-junction power divider/combiner circuit: (a) input return loss and insertion loss; (b) phase; (c) isolation; (d) output return loss.

four-way Y-junction PD/combiner is approximately 1.2 dB and the return loss is >17 dB from 4.5 to 7 GHz. A maximum amplitude imbalance of ± 0.25 dB and a phase imbalance of ±2° are observed over the entire operating frequency range. The measured and simulated results show good agreement with each other over the operating frequency range.

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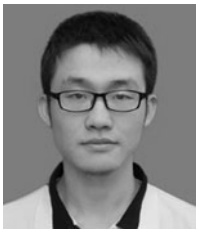
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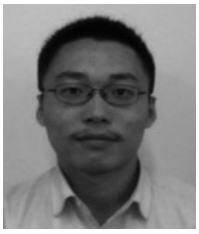
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