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High efficiency continuous mode RF power amplifier based on second and third harmonic manipulation

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Research Paper

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Abstract

Continuous mode class-J radio-frequency (RF) power amplifier is a promising technique that extends the operating bandwidth of the conventional class-B power amplifier. However, the maximum theoretical efficiency is limited to that of the class-B power amplifier. In this paper, an enhanced mode of operation for the class-J power amplifier is proposed by incorporating a third harmonic voltage component to produce an optimum waveform for maximizing the fundamental voltage component and thereby to increase the drain efficiency and introduce a new design space. A detailed derivation for the necessary relations of output power, drain efficiency, and the required harmonic load impedances is provided, showing a significant improvement in theoretical maximum efficiency from 78.5 to 89.8%. In order to confirm the developed analytic approach, a 10 W prototype amplifier model was designed and fabricated to operate within the global system for mobile communications (GSM) frequency band 850–950 MHz using a commercial GaN power high electron mobility transistor (HEMT). The experimental results have indicated that the drain efficiency of the circuit varies from 68 to 80% within the desired band.

Introduction

With the advancement in contemporary wireless mobile communication systems, high efficiency broadband radio-frequency (RF) power amplifiers become of great importance to amplify and transmit high data-rate modulated signals efficiently. Conventional harmonically tuned power amplifiers, like class-F [1] and inverse class-F [2], have been extensively and successfully used to realize efficient amplification techniques for narrowband signals. The narrowband nature of these power amplifiers is referred to the harmonic load resonators incorporated with the matching networks used in their construction [1]. Recently, continuous modes of operation for such types of amplifiers have been developed to achieve both broad bandwidth and efficient operation. These techniques include class-J [3], continuous class-F [4], and continuous inverse class-F [5] power amplifiers. In the latter modes, a larger range of harmonic impedances presented to the active device is allowed, leading to wider bandwidth and more flexible design space for the circuit [6].

In the class-J power amplifier, the drain current is assumed to have a half-sinusoidal shape while the drain voltage signal is approximated by the fundamental and second harmonics with additional phase shift of $\pi/4$ between the fundamental components of the two waveforms [7]. This is achieved by making the fundamental harmonic impedance complex and the second harmonic impedance purely reactive at the current-generator plane of the RF power field effect transistor (FET) [8]. An empirical parameter is also introduced to set the drain voltage waveform in different forms with the overall efficiency kept equivalent to that of the class-B power amplifier [3]. The third harmonic drain voltage component is assumed to be short-circuited by the output capacitance of the transistor, and control is restricted to the first and second harmonics. The price paid for the bandwidth improvement in the class-J power amplifier is an increase in the peak value of the RF drain voltage due to second harmonic tuning. The latter condition adds additional constraints on the power transistor's stress and breakdown voltage, requesting devices with higher drain breakdown voltages such as the GaN RF power HEMTs [9].

Some recent studies showed that the efficiency of the class-J power amplifier is practically affected by the third harmonic impedance and can be further increased when tuning the third-harmonic component of the drain voltage in addition to the second harmonic [10, 11]. However, a more in-depth analysis is needed to evaluate the operation of the class-J power amplifier when contributing the third harmonic component. In this paper, a modified operation for the class-J power amplifier is described by evaluating the optimum drain voltage waveform coefficients for the first three harmonic components with both the maximally-flat and the maximum-efficiency waveforms. Based on this analysis, the equations of the desired harmonic load impedances, output RF power, and drain efficiency are formulated to show the performance improvement of the suggested mode (class-J_{23}) over the conventional class-J

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power amplifier. The analysis has been verified through both ADS computer simulation and practical circuit implementation.

Theory of conventional class-J power amplifier

As stated above, the current waveform in class-J power amplifier has half-sinusoidal shape. If the power FET is assumed to be biased in a class-B mode, then the drain current is approximated by [12]:

$$i_D(\theta) = I_{\max}\left(\frac{1}{\pi} - \frac{1}{2}\cos(\theta) + \frac{2}{3\pi}\cos(2\theta) - \frac{2}{15\pi}\cos(4\theta) + \cdots\right) \quad (1)$$

where $I_{\max}$ is the drain peak current and $\theta = \omega_0 t$, with ω_0 representing the fundamental RF frequency.

The optimum theoretical drain voltage waveform with second harmonic peaking has been found to be [13]:

$$v_D(\theta) = V_{DD}(1 + \sqrt{2}\cos(\theta) + 0.5\cos(2\theta)) \quad (2)$$

where V_{DD} is the drain bias voltage.

If a certain phase-shift angle, φ, is introduced between the drain voltage and current signals, then the above equation can be re-written as:

$$v_D(\theta) = V_{DD}(1 + \sqrt{2}\cos(\theta + \varphi) + 0.5\cos 2(\theta + \varphi)) \quad (3)$$

When φ is set to $\pi/4$ to avoid second harmonic impedance with negative real part and to make the load network realizable, the above equation can be expressed as:

$$v_D(\theta) = V_{DD}(1 + \cos(\theta) - \sin(\theta) - \frac{1}{2}\sin(2\theta)) \quad (4)$$

By developing an empirical shaping parameter, α, the above equation can be re-written as:

$$v_D(\theta) = V_{DD}(1 + \cos(\theta) - \alpha\sin(\theta) - \frac{1}{2}\alpha\sin(2\theta)) \quad (5)$$

The condition $v_D(\theta) \geq 0$ is necessary to avoid driving the HEMT into the knee region which may cause severe distortion in the drain current signal. It can be shown that the peak value of the drain voltage, $v_{D(\max)} = 2.9\ V_{DD}$.

A simplified circuit model for the RF power HEMT with the main intrinsic and parasitic components is presented in Fig. 1, although more accurate nonlinear models are available in the literature [9]. In this diagram, the drain impedance at three plane levels are indicated which are the drain impedance at the current generator plane Z_d (Plane A), the load impedance at the intrinsic plane of the bare chip model Z_L' (Plane B), and the actual load impedance at the extrinsic package plane Z_L (Plane C). The nonlinear intrinsic drain to gate feedback capacitance C_{gd} is embedded with C_{ds} using the well-known Miller effect. On the other hand, C_{pd} is the drain package capacitance and the parasitic inductance L_d stands for the drain pad and bond wires. The drain-to-source resistance R_{ds} is relatively high and can be ignored in the analysis.

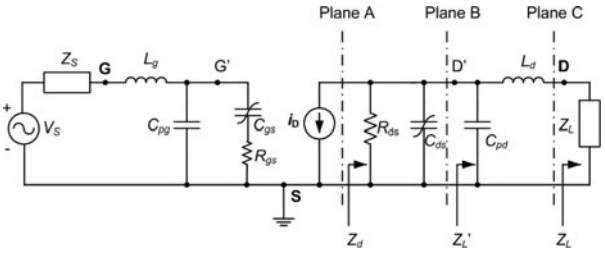


Fig. 1. Simplified circuit model for the GaN HEMT.

The first, second, and third harmonic impedances at the current generator plane are given by [8]:

$$Z_{d1} = R_{\text{opt}} + j\alpha R_{\text{opt}} \quad (6)$$

$$Z_{d2} = -j\frac{3\pi\alpha}{8}R_{opt} \quad (7)$$

$$Z_{d3} = 0 \quad (8)$$

where R_{opt} is the optimum intrinsic load-line resistance for the traditional class-B operation and is given by [12]:

$$R_{opt} = \frac{2(V_{DD} - V_k)}{I_{\max}} \quad (9)$$

with V_k representing the knee voltage of the HEMT device.

Drain voltage with second and third harmonic tuning

As presented in the design theory of the class-J power amplifier, only the fundamental and second harmonic components of the drain voltage waveform are tuned, while the third harmonic component is assumed to be zero. In the following section, the optimum drain voltage waveform is evaluated when both the second and third harmonic components are taken into account.

The drain voltage waveform that is composed of the first three harmonic components can be written as:

$$v_D(\theta) = V_{DD} + V_{d1}\cos(\theta) + V_{d2}\cos(2\theta) + V_{d3}\cos(3\theta) \quad (10)$$

where V_{DD} is the drain DC bias voltage, V_{d1} is the amplitude of the fundamental drain voltage component, V_{d2} is the amplitude of the second harmonic drain voltage component, V_{d3} is the amplitude of the third harmonic drain voltage component, and $\theta = \omega_0 t$.

Equation (10) can be re-written in the form:

$$v_D(\theta) = V_{DD}(1 + \gamma_{V1}\cos(\theta) + \gamma_{V2}\cos(2\theta) + \gamma_{V3}\cos(3\theta)) \quad (11)$$

where $\gamma_{V1} = V_{d1}/V_{DD}$, $\gamma_{V2} = V_{d2}/V_{DD}$, and $\gamma_{V3} = V_{d3}/V_{DD}$ are known as the voltage waveform factors.

The waveform factors are to be evaluated in order to produce a drain voltage signal with maximally flat bottom [14] or with maximum fundamental component [15], where the waveform in this

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Table 1. Evaluated drain voltage waveform factors

Drain voltage waveform type	γ_{V1}	γ_{V2}	γ_{V3}
Maximally-flat	1.5	0.6	0.1
Maximum efficiency	1.618	0.8677	0.2527

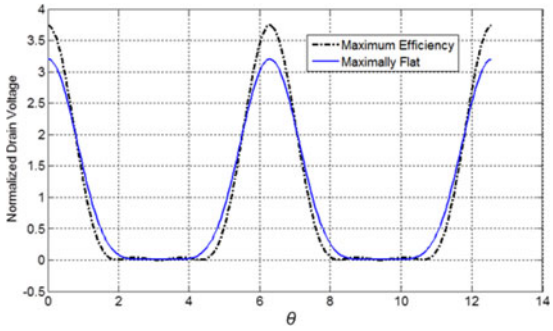


Fig. 2. Drain voltage waveform for the modified class-J mode.

case contains both odd and even harmonic components. In both shapes, the drain voltage waveform should satisfy the constraint $v_D(\theta) \geq 0$ so that severe distortion is avoided in the I–V knee region of the FET output characteristics.

The waveform factors in (11) for the maximally-flat signal can be found by successive differentiation of the drain voltage v_D with respect to θ at the critical points and equating the result to zero [16]. On the other hand, in order to obtain maximum drain efficiency, the drain voltage fundamental component has to be maximized. The waveform factors in this case are not easy to be determined analytically as those of the maximally flat waveform. A technique based on Fejer-Riesz's theorem of non-negative trigonometric polynomials together with the method of *Lagrange* multipliers can be employed to evaluate the waveform factors after converting the problem into an optimization one for maximizing γ_{V1} [17,18]. The evaluated factors for the two cases are summarized in Table 1.

The normalized drain voltage waveforms for the two cases are sketched in Fig. 2. It can be shown that $v_{D(\max)} = 3.2V_{DD}$ for the maximally flat waveform and $v_{D(\max)} = 3.7384\ V_{DD}$ for the maximum efficiency case by substituting for $\theta = 0$ in (11) with the corresponding values of the waveform factors, revealing an increase in the peak drain voltage in the latter case due to maximization of the fundamental harmonic component.

Modified operation of the class-J power amplifier

In this section, the necessary relations for finding the harmonic load impedances at the current-generator plane, output power, and drain efficiency of the proposed mode of class-J power amplifier (also may be called class-J_{23}) are formulated based on the drain voltage and current waveforms pointed to in the previous sections. The drain voltage waveform composed of the first three harmonics can be written as:

$$v_D(\theta) = V_{DD}(1 + \gamma_{V1}\cos(\theta + \varphi) + \gamma_{V2}\cos 2(\theta + \varphi) + \gamma_{V3}\cos 3(\theta + \varphi)) \tag{12}$$

where φ is an additional phase angle between the voltage and current waveforms contributed to the conventional 180° phase shift to avoid second harmonic impedance with negative resistance.

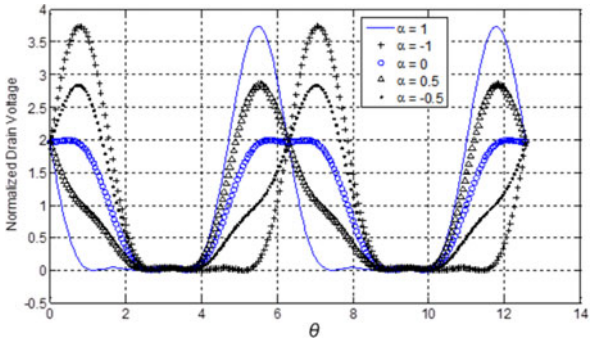


Fig. 3. Drain voltage waveform patterns for the modified class-J PA with α as a parameter.

In a similar analysis to that clarified in the class-J mode above, if $\varphi = \pi/4$, then (12) can be expanded to:

$$v_D(\theta) = V_{DD}\left(1 + \frac{\gamma_{V1}}{\sqrt{2}}\cos(\theta) - \frac{\gamma_{V1}}{\sqrt{2}}\sin(\theta) - \gamma_{V2}\sin(2\theta) - \frac{\gamma_{V3}}{\sqrt{2}}\cos(3\theta) - \frac{\gamma_{V3}}{\sqrt{2}}\sin(3\theta)\right) \tag{13}$$

This equation can also be re-written in another form after developing a similar shaping parameter, α, to make the reactive parts of the harmonic components adjustable:

$$v_D(\theta) = V_{DD}\left(1 + \frac{\gamma_{V1}}{\sqrt{2}}\cos(\theta) - \frac{\gamma_{V1}\cdot\alpha}{\sqrt{2}}\sin(\theta) - \gamma_{V2}\cdot\alpha\sin(2\theta) - \frac{\gamma_{V3}}{\sqrt{2}}\cos(3\theta) - \frac{\gamma_{V3}\cdot\alpha}{\sqrt{2}}\sin(3\theta)\right) \tag{14}$$

where $-1 \leq \alpha \leq 1$.

The drain voltage waveform is sketched in Fig. 3 for different values of α. It can be seen that α affects both the amplitude and phase of the drain voltage signal.

Based on the latter equation, the harmonic components of the drain RF voltage are given by:

$$V_{d1} = \frac{\gamma_{V1}}{\sqrt{2}}(1 + j\alpha)V_{DD} \tag{15}$$

$$V_{d2} = j\gamma_{V2}\alpha V_{DD} \tag{16}$$

$$V_{d3} = \frac{\gamma_{V3}}{\sqrt{2}}(-1 + j\alpha)V_{DD} \tag{17}$$

If the effect of the knee voltage of the HEMT is considered, then V_{DD} is replaced by $(V_{DD} - V_k)$ in the above three equations. The drain current signal is defined as given in (1) and therefore the drain harmonic impedances at the current generator reference plane are evaluated from dividing the harmonic drain voltage components by their equivalent harmonic current components:

$$Z_{dn} = -\frac{V_{dn}}{I_{dn}} \tag{18}$$

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So, we have:

$$Z_{d1} = \frac{\gamma_{V1}}{\sqrt{2}}(R_{\text{opt}} + j\alpha R_{\text{opt}}) \tag{19}$$

$$Z_{d2} = -\frac{j3\pi\gamma_{V2}\alpha}{4} R_{\text{opt}} \tag{20}$$

$$Z_{d3} = \infty \tag{21}$$

where R_{opt} is given by (9) and can be tolerated to adjust the peak drain current $I_{\max}$ in real power devices as well as to maximize the output RF power.

Although the value of third harmonic impedance is theoretically infinite due to zero third harmonic drain current, but in reality it can be of some finite value when there is a third harmonic drain current component resulting from a conduction angle >180°.

The output RF power is given by:

$$P_{\text{out}} = 0.5\text{Re}[V_{d1} \cdot I_{d1}^{*}] = \frac{\gamma_{V1}}{4\sqrt{2}} V_{DD} \cdot I_{\max} \tag{22}$$

This equation can be formulated as

$$P_{\text{out}} = \frac{\gamma_{V1}}{2\sqrt{2}} \frac{V_{DD}^2}{R_{\text{opt}}} \tag{23}$$

The DC input power is given by the product of drain DC voltage and current components:

$$P_{\text{DC}} = \frac{1}{\pi} V_{DD} \cdot I_{\max} \tag{24}$$

The drain DC to RF efficiency is therefore found through dividing (22) by (24):

$$\eta_D = \frac{\pi}{4} \cdot \frac{\gamma_{V1}}{\sqrt{2}} \times 100\% \tag{25}$$

The second term in (25) represents the improvement in the theoretical drain efficiency of the modified class-J mode over that of the conventional class-J PA. It can be shown that the theoretical efficiency for the case of maximally flat waveform is equal to 83.3%, and that of maximum efficiency case reaches to about 89.8% by substituting the corresponding values of γ_{V1} from Table 1 in (25). Both of these figures exceed the theoretical value of the conventional class-J power amplifier due to the inclusion of the third harmonic component, with a net result of raising the fundamental voltage component. This will, however, increase the peak value of the drain voltage waveform to about $3.73V_{DD}$ as illustrated in the previous section.

The drain voltage waveforms presented in Fig. 3 seem, for the first glance, similar (but not identical) to the voltage patterns obtained in the continuous class-F mode power amplifier. However, the exact drain voltage signal in continuous class-F mode, when de-factorized, contains four harmonic components that have different coefficients from those obtained in (14) with amplifier's maximum theoretical efficiency of 90.7% [12]. The contribution of a fourth harmonic load impedance requires devices with higher gain-bandwidth product and lower output capacitances so as not to short-circuit the fourth harmonic voltage component unless approximation is carried out by neglecting this impedance. Besides, we have introduced voltage waveform factors to control the amplitude and shape of the drain voltage signal which adds additional flexibility to reduce the signal peak amplitude at the expense of some expected loss in efficiency. Additionally, for more generalized analysis with current conduction angles other than 180°, there will be a third harmonic current component and therefore the third harmonic impedances will vary considerably since the third harmonic voltage component of the modified class-J mode is entirely different from that of the continuous class-F mode and includes both real and imaginary parts as predicted in (17).

A general comparison between the conventional and modified class-J power amplifier modes is summarized in Table 2.

Table 2. Theoretical performance comparison between conventional and modified class-J modes

Characteristic	Class-J	Modified class-J
Drain voltage tuned harmonics	2	3
Drain current harmonics	2	2
Maximum drain efficiency	78.5%	89.8%
Peak drain voltage	$2.9V_{DD}$	$3.73V_{DD}$
Fundamental drain impedance	Complex	Complex
Second-harmonic drain impedance	Reactive	Reactive
Third-harmonic drain impedance	Zero	Infinite

Evaluation of the extrinsic harmonic impedances

In this section, explicit-form relations for the required harmonic load impedances at the drain of the device package are derived in terms of the internal model and parasitic components of the HEMT as well as the shaping parameter α. These equations are useful in estimating the actual load impedances that can, otherwise, be obtained through the harmonic load-pull test or by nonlinear embedding techniques to transform the impedances from the current generator plane into the package plane [19–21]. In order to investigate the effect of the intrinsic and extrinsic elements of the power transistor on harmonic load impedances, a real power GaN HEMT device from Wolfspeed is selected. The large signal CAD models for the packaged transistor, CGH40010F, together with its bare die CGH60015D have been used to estimate the parasitic components of the transistor. A simplified packaged model for the HEMT is presented in Fig. 4.

At higher microwave frequencies, additional FET parasitic elements such as the source lead inductance and resistance can be inserted for more accurate analysis. On the other hand, the intrinsic output capacitance C_{ds}, shown in Fig. 1, is estimated from a technique adopted in [22] and is equal to 1.1 pF, where it actually includes both the gate-to-drain Miller capacitance and the drain-to-source capacitance as stated previously. Although this capacitance is usually voltage dependent and is a nonlinear element, it can be assumed linear in GaN HEMT devices with satisfactory results to simplify the analysis [23, 24].

For a drain bias voltage of 28 V, knee voltage of 4 V, and drain peak current of 1.6 A, the optimum load-line resistance is estimated from (9) to be 30 Ω. However, the value of R_{opt} can be

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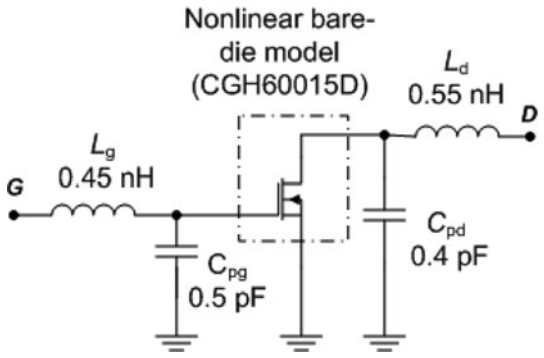


Fig. 4. An optimized model for the CGH40010F Packaged HEMT.

adjusted to control drain efficiency, output RF power, and the peak value of the drain current waveform. The theoretical drain harmonic impedances at the current generator reference plane of the power HEMT are evaluated from (19)–(21), respectively.

The effect of the parasitic elements of the drain can be investigated by referring to Fig. 1. If R_{ds} is ignored and the drain intrinsic capacitance C_{ds} and drain package capacitance C_{pd} are combined together in one equivalent capacitance, C_{out}, then $C_{\text{out}} = C_{ds} + C_{pd}$. Using linear embedding technique, it can be shown that the real and imaginary parts of the fundamental harmonic load impedance Z_{L1} are given by:

$$R_{L1} = \frac{(1+\alpha^2)R'_{\text{opt}}}{1+(\alpha+\omega_0 C_{\text{out}}(1+\alpha^2)R'_{\text{opt}})^2} \tag{26}$$

$$X_{L1} = \frac{(\alpha+\omega_0 C_{\text{out}}(1+\alpha^2)R'_{\text{opt}})(1+\alpha^2)R'_{\text{opt}}}{1+(\alpha+\omega_0 C_{\text{out}}(1+\alpha^2)R'_{\text{opt}})^2} - \omega_0 L_d \tag{27}$$

where R'_{opt} is given by:

$$R'_{\text{opt}} = \frac{\gamma_{V1}}{\sqrt{2}} R_{\text{opt}} \tag{28}$$

Similarly, the second harmonic load impedance Z_{L2} is given by:

$$Z_{L2} = j\frac{3\pi\gamma_{V2}\alpha R_{\text{opt}} + 8\omega_0 L_d - 12\pi\omega_0^2\gamma_{V2}\alpha R_{\text{opt}} L_d C_{\text{out}}}{6\pi\omega_0\gamma_{V2}\alpha R_{\text{opt}} C_{\text{out}} - 4} \tag{29}$$

The combination of the third harmonic load impedance, Z_{L3}, with the inductive reactance of the drain parasitic inductance, L_d, should resonate with C_{out} at the third harmonic frequency to present an infinite impedance at the intrinsic drain of the power HEMT, and therefore:

$$Z_{L3} = j\left(\frac{1}{3\omega_0 C_{\text{out}}} - 3\omega_0 L_d\right) \tag{30}$$

Figure 5 shows the effect of C_{out} and L_d in shifting the harmonic load impedances as compared with the ideal drain harmonic impedances at the current generator plane. The output capacitance is set to 1.5 pF and the drain inductance is equal to 0.55 nH as indicated in Fig. 4.

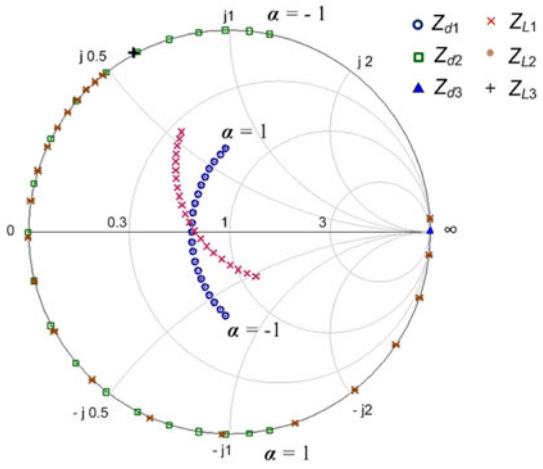


Fig. 5. Normalized harmonic load impedances at the current generator and package planes.

Investigation of the power amplifier operation

A computerized test setup has been used to study the behavior of the proposed class-J power amplifier mode for different loading conditions as depicted in Fig. 6. In this test circuit, the CGH60015D bare-chip nonlinear CAD HEMT model, embedded with the package parasitic elements, is excited by a 50 Ω signal source. This device is biased with gate-to-source voltage of −3 V, and drain-to-source voltage of 28 V through suitable RF chokes and bypass capacitors. The circuit is terminated with the harmonic load impedances formulated in (26), (27), (29), and (30) at the first three harmonic frequencies. The voltage waveform factors are taken for the maximum efficiency case, while α is varied as a parameter. This simulation setup is implemented with the aid of the ADS microwave CAD program of Keysight.

A comparison between the drain voltage and current waveforms for the class-J and modified class-J modes is presented in Fig. 7 for a shaping parameter $\alpha = 1$ and at an operating frequency of 900 MHz. In this simulation, the input driving power level is set to 29 dBm. This sketch shows clearly the increase in the peak drain voltage of the modified mode and narrower overlapping with the drain current signal. On the other hand, the drain current waveforms for both modes are close to each other, approaching to a half-sinusoidal shape. A comparison between the fundamental components of the drain voltage for the two modes of operation versus input drive power is presented in Fig. 8(a), showing a significant increase in the case of the modified mode. On the other hand, the fundamental drain current components are almost close to each other as shown in Fig. 8(b).

The simulated drain efficiencies of the two modes versus drive power are sketched in Fig. 9. It is apparent that the maximum efficiency for the enhanced class-J power amplifier is more than 85% at 29 dBm input signal power, and it equals to 76% for the class-J mode at the same input power level. It is also shown from the sketch that the drain efficiency with maximally-flat voltage waveform for the modified mode lies in-between the responses of the two modes mentioned above.

In Fig. 10, the simulated drain voltage and current waveforms of the modified class-J mode are sketched for $\alpha = 0$ and $\alpha = -1$ at 900 MHz. The shape of each drain voltage waveform in Fig. 10 resembles the corresponding theoretical pattern in Fig. 3.

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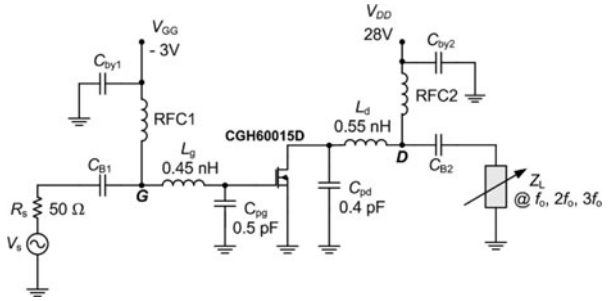


Fig. 6. Simulation setup for examining the behavior of the modified class-J PA mode.

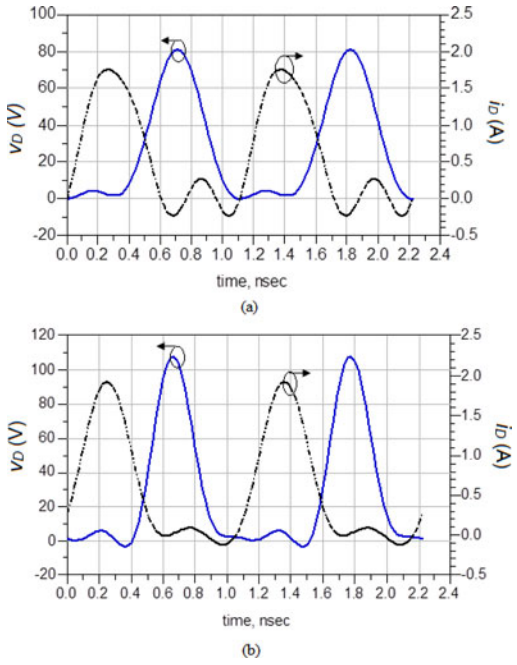


Fig. 7. Drain voltage and current waveforms for the class-J (a) and modified class-J (b) modes for $\alpha = 1$.

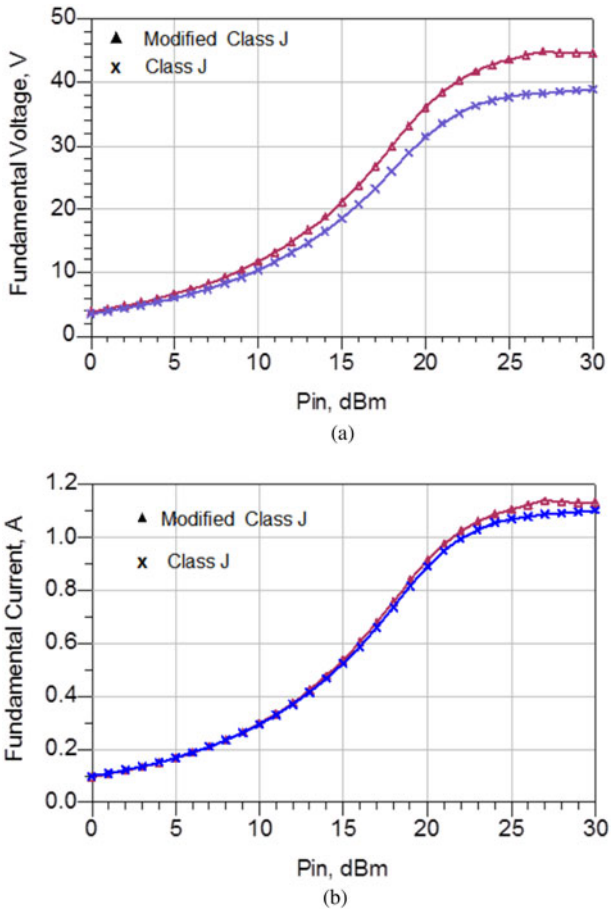


Fig. 8. Fundamental drain voltage (a) and current (b) components versus input power for the class-J and modified class-J modes when $\alpha = 1$.

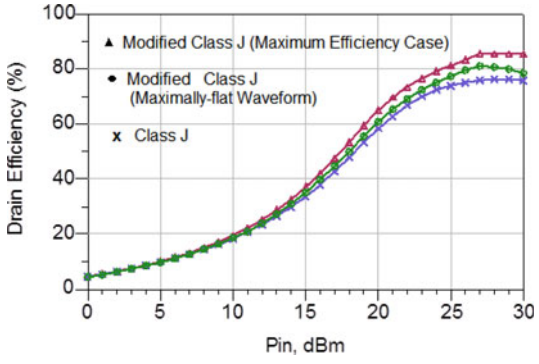


Fig. 9. Simulated drain efficiency versus input power for class-J and modified class-J modes.

Design of a GSM power amplifier circuit

In order to confirm the proposed power amplifier mode, a typical 10 W RF power amplifier circuit has been designed based on the commercial GaN HEMT CGH40010F of Wolfspeed to operate within the GSM band from 850 to 950 MHz. Although the selected bandwidth is moderate, it is adequate to verify the theory presented thus far. The optimum load impedances at the first three harmonics are evaluated for specific frequencies in the desired band with appropriate selected values of the shaping parameter, α.

It is well known that complex impedances are only realizable when they change in clockwise direction on the Smith chart with the increase in frequency. However, for a given value of α, it can be seen from (29) that the required second harmonic load impedance is varying in anti-clockwise direction against frequency. On the other hand, the extrinsic second harmonic load impedance can be made changing in clockwise direction by decreasing α in a prescribed range as it is clear from Fig. 5. So, the range of change in the parameter α can be selected in such a way to overcome the anti-clockwise rotation of the second-harmonic load impedance with frequency [23]. Based on this approach, the range for α variation has been selected from 0.8 to 0.4 with an increase in frequency from 850 to 950 MHz. Actually, the range over which α is adjusted is proportional to the operating bandwidth of the circuit, and the individual values of the shaping parameter are taken to avoid very high peak drain voltages that may drive the device near the breakdown region as predicted in (14) and Fig. 3.

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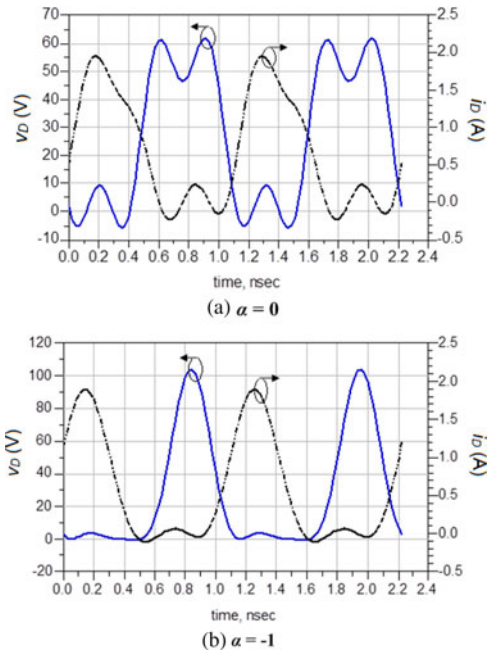


Fig. 10. Drain current and voltage signals for two values of α. (a) $\alpha = 0$, (b) $\alpha = -1$.

For a step size in frequency of Δf, the number of evaluated frequencies in the band of interest is given from:

$$n = \frac{f_H - f_L}{\Delta f} \tag{31}$$

In this relation, f_L and f_H are the low and high frequency edges of the band. When $f_L = 850$ MHz, $f_H = 950$ MHz, and $\Delta f = 10$ MHz, then $n = 10$. The decrement in α for a corresponding increment in frequency is calculated from:

$$\Delta\alpha = \frac{\alpha_{max} - \alpha_{min}}{n} \tag{32}$$

where $\alpha_{max} = 0.8$ and $\alpha_{min} = 0.4$.

Starting from $f_L = 850$ MHz and $\alpha_{max} = 0.8$, and proceeding with $f_{i+1} = f_i + \Delta f$, $\alpha_{i+1} = \alpha_i - \Delta\alpha$ until $f_H = 950$ MHz and $\alpha_{min} = 0.4$, the harmonic load impedances can be estimated from (26), (27), (29), and (30) with a load-line resistance of 30 Ω and are sketched in Fig. 11.

The load network can therefore be designed to predict the harmonic load impedances presented in Fig. 11 across the desired frequency band. There are several topologies used to synthesize the output matching networks for harmonically-tuned RF power amplifiers [25–27]. In this design, a three-section low-pass impedance matching network is synthesized analytically at the center frequency and then optimized with ADS to fit the desired impedances across the entire band. The topology of the load network is presented in Fig. 12, where the transmission line electric lengths and characteristic impedances are evaluated using a technique adopted in [22] to present $Z_{L1} = 23.5 + j20.25\ \Omega$, $Z_{L2} = -j104.15\ \Omega$, and $Z_{L3} = j30\ \Omega$ for $\alpha = 0.6$ at 900 MHz.

The load network has then been optimized to predict the calculated harmonic load impedances across the entire frequency band. All the transmission lines were converted to microstrip lines based on Rogers RO4350B substrate with thickness of 1.527 mm

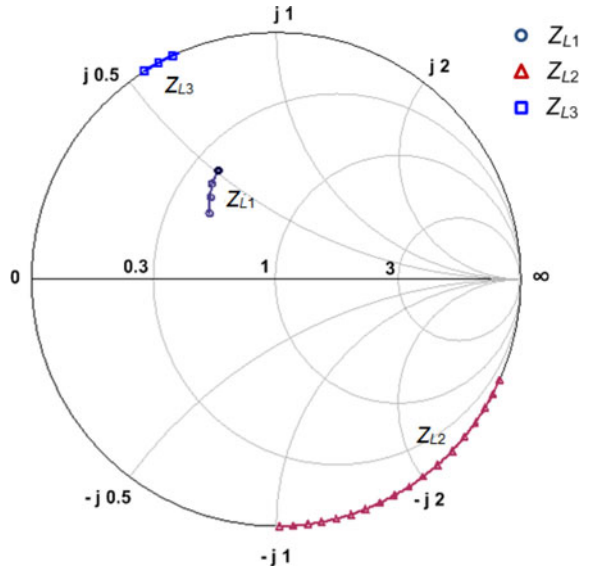


Fig. 11. Estimated harmonic load impedances for the frequency range 850–950 MHz.

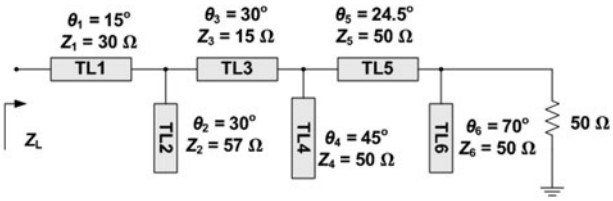


Fig. 12. Initial design of the harmonic load network at 900 MHz.

(60 mil), dielectric constant of 3.66 and loss tangent of 0.0031 at 1 GHz. Figure 13 presents the schematic of the optimized load network while its impedance response is depicted on the Smith chart in Fig. 14. The harmonic load impedances in this sketch are almost close to the calculated values presented in Fig. 11 for the frequency band of interest. This implies that the optimized load network well fits the target theoretical harmonic load impedances.

In order to increase the stability factor of the circuit and prevent parasitic oscillations, a stabilizing circuit consisting of a series microstrip line and a parallel *RC* network has been inserted at the input of the GaN HEMT. With the output matching network connected to the drain of the packaged transistor and the stabilizing circuit existing at the input port, the power amplifier circuit was simulated to evaluate the large signal input impedance across the desired frequency band at an input driving level of 29 dBm. An input matching circuit, using two-section ladder structure, was thereafter designed for conjugate matching to increase the power gain of the amplifier. The schematic of the final power amplifier circuit is shown in Fig. 15.

Circuit simulation and implementation

The power amplifier circuit has been simulated by means of the harmonic balance simulator embedded with ADS software. In Fig. 16, the drain voltage and current waveforms at the current generator reference plane of the GaN HEMT are displayed at the lower band edge, center of the band, and upper band edge,

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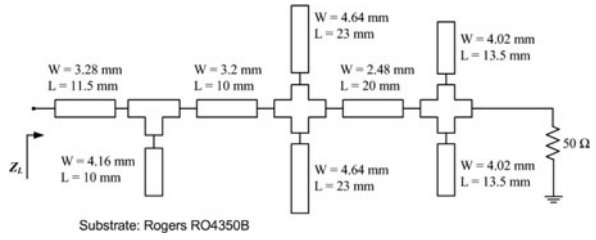


Fig. 13. Circuit schematic of the optimized microstrip-line load network.

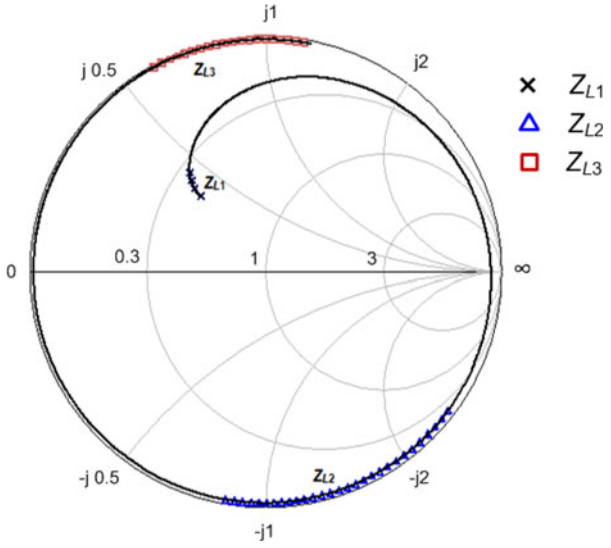


Fig. 14. Simulated impedances versus frequency for the optimized load network.

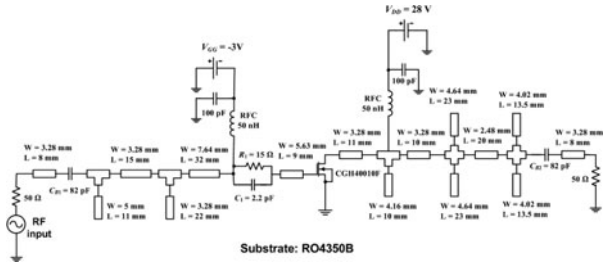


Fig. 15. Schematic diagram of the designed power amplifier circuit.

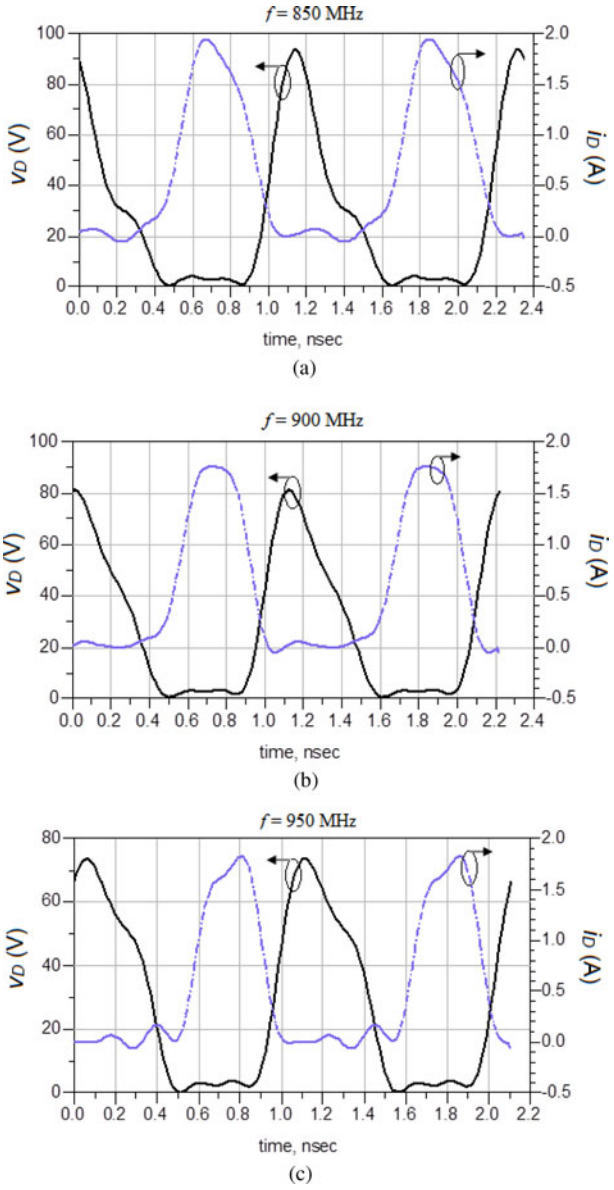


Fig. 16. Simulated drain voltage and current waveforms for different frequencies. (a) f=850 MHz, (b) f=900 MHz, (c) f=950 MHz.

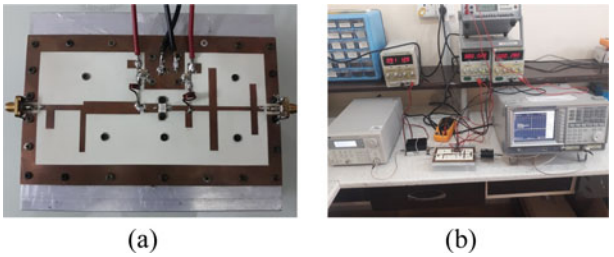


Fig. 17. Photographs for the constructed power amplifier (a) and the test-setup (b).

respectively. These waveforms are consistent with those presented in Fig. 3 where α is set to 0.8 at 850 MHz, 0.6 at 900 MHz, and 0.4 at 950 MHz. The drain current has an approximate half-sinusoidal shape at the three mentioned frequencies.

A prototype model for the modified class-J power amplifier circuit was constructed to verify the proposed mode of operation. A printed circuit board was manufactured using Rogers RO4350B substrate with dimensions of 15 cm × 9 cm. This board was fixed tightly on a suitable aluminum heat sink using small-size screws which served also as pads between the upper and lower grounds. The RF transistor was mounted on the heat sink by means of two screws after cutting a slot on the board. The RF chocks were wounded manually using three turns of size 20 AWG wires. The RF performance of each lumped component was tested by means of the Anritsu MS4642A VNA and using suitable fixture before soldering it into the printed board. A photograph for the assembled power amplifier is depicted in Fig. 17(a). The practical test setup for measuring the performance of the power amplifier

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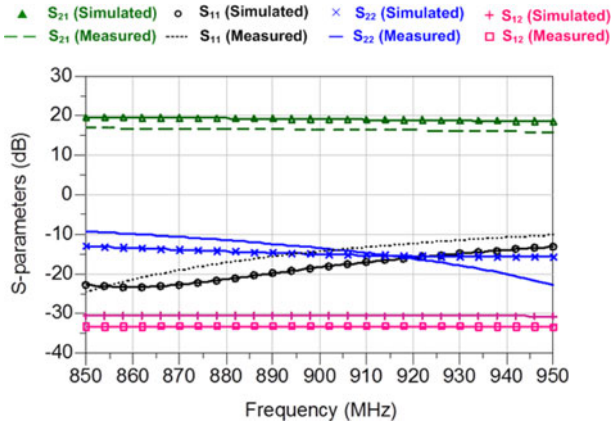


Fig. 18. Simulated and measured small signal *S*-parameters versus frequency.

consists of a TTi TGR-1040 synthesized RF signal generator followed by a driver power amplifier module (MPA-0950 from RF Bay) to raise the signal power level at the input of the amplifier under test. A 25 W, 30 dB attenuator was connected to the output of the amplifier to attenuate the amplified RF signal before applying it to the ED PSA-3000 spectrum analyzer. The measurement setup is shown in Fig. 17(b).

The small signal *S*-parameters of the circuit are simulated and measured versus frequency in Fig. 18. It can be seen that the measured small signal gain S_{21} is lower than the simulated gain by about 2.5 dB across the band of interest with an average value of 16.5 dB. Both the simulated and measured input and output return losses, S_{11} and S_{22}, are lower than −10 dB revealing acceptable matching over the specified frequency range. The reverse gain, S_{12}, is shown to be better than −30 dB, thereby providing acceptable isolation between the output and input ports.

The simulated and measured large signal performance characteristics of the power amplifier against the desired frequency range are presented in Fig. 19 for an input driving signal level of 29 dBm. No tuning process was carried out for the matching stubs to improve the practical response of the circuit. The simulated drain efficiency is changing between 82.5 and 83.5%, showing a significant improvement over the conventional class-J mode. However, the measured drain efficiency varies between 68 and 80% for different sample frequencies in the band. The mean value of the measured efficiency for the circuit is almost lower than the simulated result, but in certain frequencies it exceeds the 78.5% limit of the conventional class-J power amplifier. This sketch shows that the simulated large signal gain varies between 12 and 12.5 dB while the measured gain changes from 10.41 to 11.25 dB across the mentioned frequency range. The simulated output power is about 41 dBm at 850 MHz and drops to 40.5 dBm at 950 MHz while the measured output RF output power changes between 39.41 and 40.25 dBm. This difference between the simulated and measured response is referred to the additional parasitics and imperfections resulted from the implementation process and also to the deviation between the transistor CAD model and the actual behavior of the physical device. Additionally, there may be some reflected power from the power amplifier under test into the driver amplifier which makes the latter not working in its perfectly matched conditions.

When comparing the small signal gain presented in Fig. 18 and the saturated large signal gain in Fig. 19, a considerable difference is noted because in the latter case the amplifier is heavily driven into the nonlinear region with input power of 29 dBm.

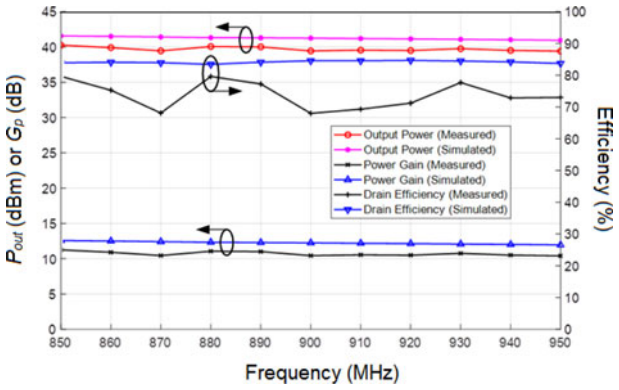


Fig. 19. Simulated and measured performance characteristics versus frequency.

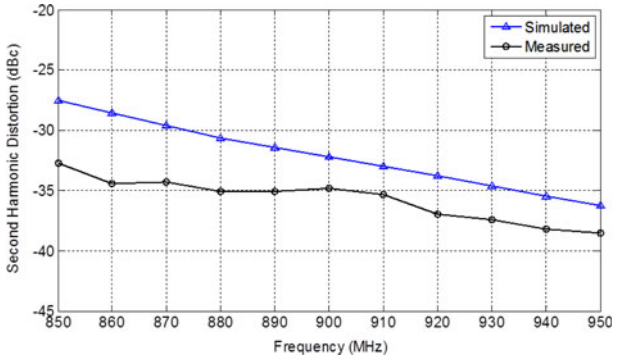


Fig. 20. Simulated and measured second harmonic level versus frequency.

Table 3. Comparison with other recent works on class-J PAs

Ref.	Year	Frequency (GHz)	η_D (%)	Power (dBm)
[10]	2011	2.3–2.7	60–62	40–40.7
[23]	2012	0.5–1.8	50–69	39–40
[24]	2014	0.5–0.9	60–72	39.5–40.5
[21]	2017	1.3–2.4	63–72	40.1–41.2
[26]	2017	1.79–2.21	71–74	40.1–42.39
[27]	2019	1.0–3.0	55–66	40–42.6
This work	2020	0.85–0.95	68–80	39.41–40.25

This is necessary to generate the required harmonic component levels that shape the drain voltage signal properly for maximized efficiency. In Fig. 20, the simulated and measured second harmonic levels are presented against frequency. The measured response shows a second harmonic distortion lower than −30 dBc across the entire band as a result of the low pass nature of the load network.

A comparison in performance parameters of the designed modified class-J power amplifier with some other recent works on the class-J continuous mode power amplifier is summarized in Table 3, revealing improved drain efficiency, η_D.

Conclusion

A design approach to enhance the efficiency of class-J RF power amplifiers has been proposed and verified. This approach involves

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the incorporation of a third harmonic component to the drain voltage signal of the RF power device. The optimum theoretical drain voltage harmonic component amplitudes have been derived and the resulting relations for output RF power and maximum drain efficiency of the circuit were evaluated. Furthermore, simplified relations have been given to estimate the required harmonic load impedances at the package plane of the transistor. In order to validate the proposed mode of operation, a typical 10 W RF power amplifier circuit using a commercial GaN power HEMT has been designed, simulated, and fabricated for operation within the GSM mobile communication band from 850 to 950 MHz. The experimental results showed that drain efficiency between 68 and 80% was obtained across this band, which revealed an improved efficiency performance. Although theoretical formulas were used to expect the optimum harmonic load impedances based on a CAD device model, empirical load-pull measurement or nonlinear embedding technique can also be used to determine these impedances more accurately. Also, a more generalized analysis can be conducted when the conduction angle of the drain current signal is taken into consideration where the odd harmonics of the current waveform are no longer zero.

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