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Coherent J-Band radiating arrays based on ×27 CMOS activemultiplier chips

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Research Paper

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Abstract

This paper presents a hybrid design of 1 × 2 and 1 × 4 arrays operating in 0.277–0.292 THz on 65 nm Complementary metal–oxide–semiconductor (CMOS) technology. Each of the chips has an X-band input with 3 ×3 multiplier stages and connected at the output to an on-chip ring antenna. A wideband microstrip Wilkinson four-way and two-way power dividers have been developed on a multilayer printed circuit board to feed the array elements with proper radio frequency and direct current inputs. Demonstrating improvements in effective isotropically radiated power and in total radiated power compared to a single CMOS element, the hybrid integration approach proves effective in implementing coherent THz transmitter arrays. Theoretical and practical factors that reduce the radiated power compared with ideal arrays are also discussed.

Introduction

The THz radiation domain possesses many advantages for different promising applications in variety of fields. In recent years, several researches have been conducted, to implement on-chip sources with different virtues and drawbacks trying to produce a low cost, highdirect current-to-radio frequency (DC-to-RF) efficiency source [1]. Another goal is to achieve minimal losses in radiating the high frequency signal outside the chip. The last issue acquires additional complexity when we talk about feeding the signal into an array of radiating elements.

In designing THz source and antenna, semiconductor material has a major impact on the performance, affecting both the cut-off frequency, and the on-chip antenna radiation efficiency and pattern. In terms of f_t/f_{max}, no doubt that III–V compound semiconductors have many advantages over CMOS ($f_{max} < 200$ GHz) at such high frequencies. In [2–4] the SiGe compound ($f_{max} \approx 300$ GHz) have been used. Another attempt to overcome this issue is the use of Silicon on insulator ($f_{max} \approx 250\ GHz$) [5]. These approaches make it possible to design a higher frequency source, and reach the THz band with fewer multiplications. Nevertheless, the low cost and the capability of providing high integration of analog and digital circuits made CMOS technologies very attractive for future developments in the THz domain. In light of these benefits, several techniques were researched to achieve highly functional sources in CMOS [6–11].

Two approaches exist for THz source implementation – a fundamental voltage-controlled oscillator (VCO) and a low frequency source in conjunction with frequency multiplier chain. Regarding the former, in most of the cases, a VCO is used in N-push topology, to generate higher harmonics while maintaining a reduced component size [3, 4, 7–12]. Pushing higher harmonics is fraught with decreasing the output power and DC-to-RF efficiency and requires a proper locking technique. The multiplier chain alternative may require several stages, but gives the advantage of utilizing the lower bands for effective amplifications, on the way to THz radiation. Several articles [2, 5, 6] describe different approaches to the use of multiplier chains.

After utilizing one of the above solutions for THz source, one needs to decide on the antenna solution. As before, two solutions exist – off-chip and on-chip antennas. In [13] Liquid Crystalline Polymer was used for printed circuit board (PCB) material to implement the off-chip antenna solution. High gain and constant radiation pattern are the major advantages for this approach, but the high losses caused by the bond-wire transition create a trade-off condition for a designer.

The above arguments were considered in designing, manufacturing, and measuring a single chip that combines a ×27 multiplier chain with an on-chip ring antenna on Taiwan Semiconductor Manufacturing Company (TSMC) 65 nm CMOS substrate. In [6] the reader can find a detailed explanation of the circuit architecture, and the measurement results. This work utilizes this chip, to implement an array of elements. Several challenges exist in expanding a single element to an array in the THz band, which involves the decision on an array feeding network topology.

In this work, we present one-dimensional transmitter steerable arrays based on CMOS active ×27 frequency multiplier chips. The on-chip J-Band antenna array design considerations

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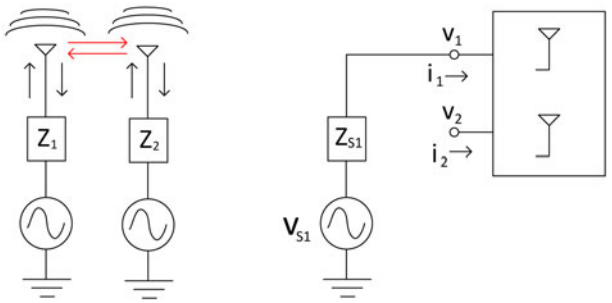


Fig. 1. Two elements array coupling diagram.

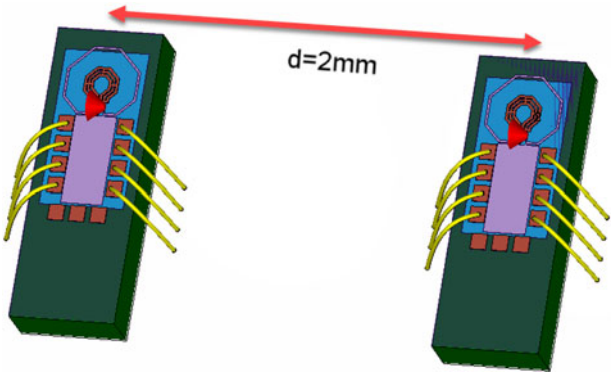


Fig. 2. Simulated structure of the 1 × 2 array with $d = 2$ mm.

are discussed in the section "Array design considerations". In section "Design" we discuss the specific 1 × 2 and 1 × 4 array designs, including the X-band grounded coplanar waveguide (GCPW) Wilkinson power divider (WPD). The measured results of the power divider and the radiating arrays are presented in the section "Measurement results", and the section "Conclusion" summarizes the work.

Array design considerations

CMOS on-chip antennas pose design challenges due to the non-isolating high permitivity substrate. Performance is highly influenced by the silicon thickness and chip lateral dimensions and the antenna effective area can well extend the chip area. As a result, coupling between array elements can have a significant effect on its performance and need to be carefully investigated. Moreover, amplitude and phase mismatch between array elements can also have an impact on the array performance, especially when the elements multiply the input frequency by 27. In this section, we analyze the impact of these imperfections analytically and numerically.

Coupling

In theory, the farfield radiation pattern of an array of elements can be seen as a lossless combination of each element pattern. In reality, there is mutual coupling between the elements resulting in a change of the boundary conditions, that in turn affects the radiation and terminal properties. Figure 1 shows a case of two antennas forming a 1 × 2 array. To analyze the affect of the mutual coupling, Z-parameters calculations can be used:

$$\mathbf{v} = \begin{pmatrix} v_1 \\ v_2 \end{pmatrix} = \mathbf{Z} \cdot \mathbf{i}, \tag{1}$$

$$\begin{cases} v_1 = Z_{11} i_1 + Z_{12} i_2; \\ v_2 = Z_{21} i_1 + Z_{22} i_2. \end{cases}, \tag{2}$$

$$v_1 = v_{S1} - Z_{S1} i_1, \tag{3}$$

$$v_{S1} - Z_{S1} i_1 = Z_{11} i_1 + Z_{12} i_2, \tag{4}$$

$$i_1 = \frac{v_{S1} - Z_{12} i_2}{Z_{11} + Z_{S1}}, \tag{5}$$

$$v_2 = \underbrace{\frac{Z_{21} v_{S1}}{Z_{11} + Z_{S1}}}_{v_2^{oc}} + \underbrace{\left[Z_{22} - \frac{Z_{21} Z_{12}}{Z_{11} + Z_{S1}} \right]}_{Z_{in,2}} i_2. \tag{6}$$

It can be seen in Equation 6, that the input voltage at port 2 depends on the voltage of port 1. This dependency is translated into input characteristics at port 2 and radiation pattern changes. Let us look at the radiation pattern of this array. The total radiation pattern is the sum of the embedded patterns of each element, while all the other elements are "open circuit".

$$f(\theta, \phi) = \sum_n f_n^{oc}(\theta, \phi) i_n = f_1^{oc} i_1 + f_2^{oc} i_2. \tag{7}$$

To show the impact of the first element on the second element pattern, Equation 5 will be used, with $v_1 = 0$.

$$f(\theta, \phi) = f_2^{oc} i_2 - \frac{f_1^{oc} Z_{12} i_2}{Z_{11} + Z_{S1}} = \underbrace{\left[f_2^{oc} - \frac{Z_{12}}{Z_{11} + Z_{S1}} f_1^{oc} \right]}_{f_2^{oc'}(\theta, \phi)} i_2. \tag{8}$$

In conclusion, the influence of each element on each other should be taken into consideration of the array structure.

Next, to simulate possible coupling in a similar structure of J-Band elements, CST MWS was used. The simulated structure is shown in Figure 2. The element distance of 2 mm was chosen for practical reasons, and its effect will be discussed in the next section. In general, to achieve greater steering angles for phased array, the distance should be smaller than λ, but as distance grows, so does the gain of the array. As for the coupling between the elements, the relation between it and the distance is reversed.

At $f = 264$ GHz – $Re\{Z_{21}\}$ is at its maximum with 2.4 Ω, while $Im\{Z_{21}\}$ reaches its maximum value, 1.67 Ω, at 259.5 GHz. Using Equation 8, $Z_{source} = 50$ Ω together with Z_{11} and Z_{21} values from Figures 3, 4 at $f = 264$ GHz, yields around $(0.02 - 0.003j) f_1^{OC}$. It represents the effect of the first element on the radiation pattern of the second element, and will affect both the amplitude and the phase difference between them. It is important to note that for frequency range measured in this paper, simulated coupling between elements is <0.1%.

Another way to illustrate coupling affects would be to compare element radiation pattern between a stand alone element and an

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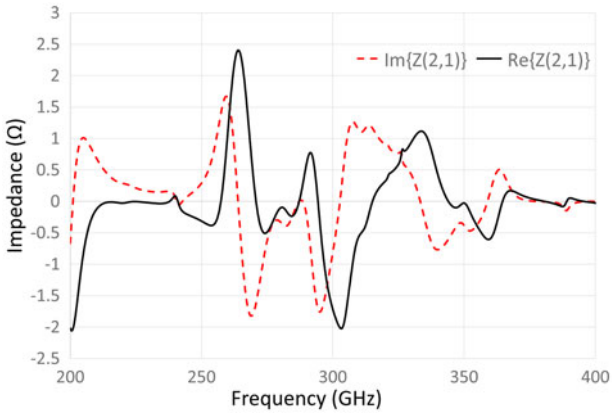


Fig. 3. Z_{21} real and imaginary parts representing coupling between two J-Band elements of the 1 × 2 array with $d = 2$ mm.

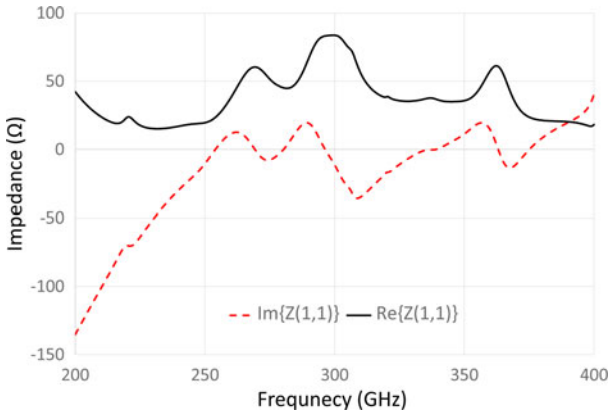


Fig. 4. Z_{11} real and imaginary parts representing the input impedance of a single J-Band element.

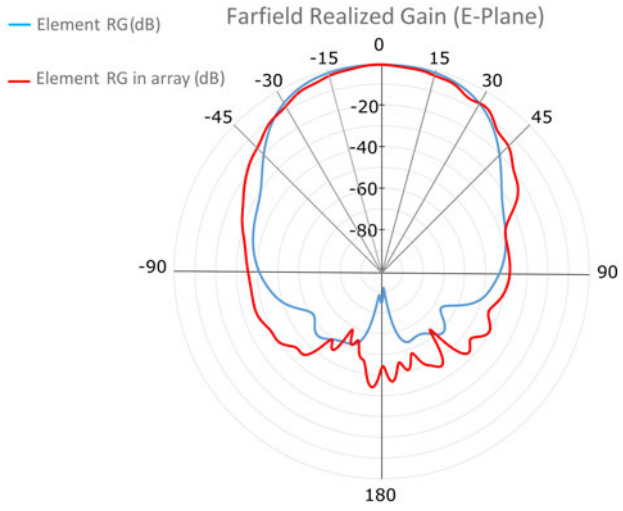


Fig. 5. Radiation pattern comparison between stand-alone element simulation and single element in an array, $f = 280$ GHz.

element in array. Figure 5 demonstrates the difference, and it can be seen that other elements have impact on the phase and amplitude of a single element.

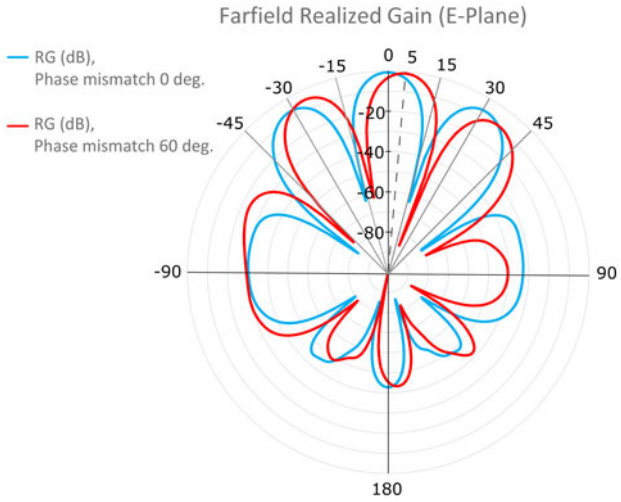


Fig. 6. Phase mismatch impact on the *E*-Plane of the Farfield Realized Gain of the 1 × 2 array, $f = 280$ GHz; $d = 2$ mm.

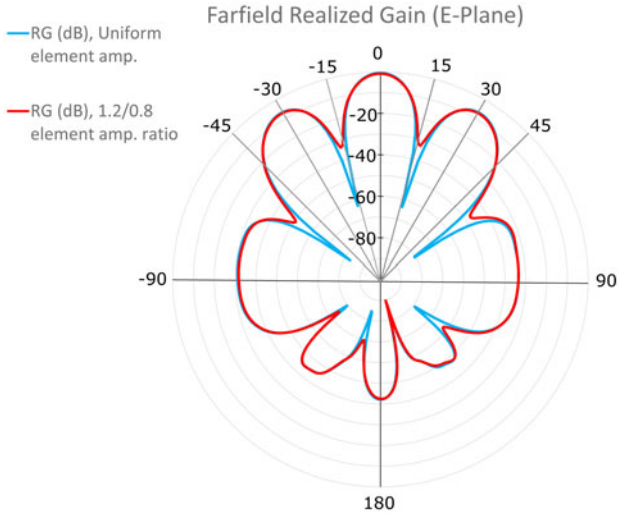


Fig. 7. Amplitude mismatch impact on the *E*-Plane of the Farfield Realized Gain of the 1 × 2 array, $f = 280$ GHz; $d = 2$ mm.

Phase and amplitude mismatch

To analyze the phase and amplitude mismatch impact on the simulation it is necessary to determine the range of possible deviation for each parameter. Phase mismatch can be a product of a small mismatch between the feeding network outputs, through bondwires connected to the chip input pads. This difference is than multiplied by ×27. Coupling effect discussed in the previous subsection could also add to the phase differences. This small error can get as high as ±1.1° so the maximum phase mismatch between elements can get as high as 60°. Figure 6 shows simulated *E*-Plane results for both 0° and 60° phase mismatch. It can be seen that the maximum simulated phase mismatch gives 5° direction shift on *E*-Plane, also resulting in 0.2 dB mainlobe loss.

Regarding the amplitude deviation between array elements, the reason can be different DC operating points for each element, and coupling issues. Amplitude deviation affects the gain of the total radiation pattern and sidelobe level. Figure 7 shows the impact

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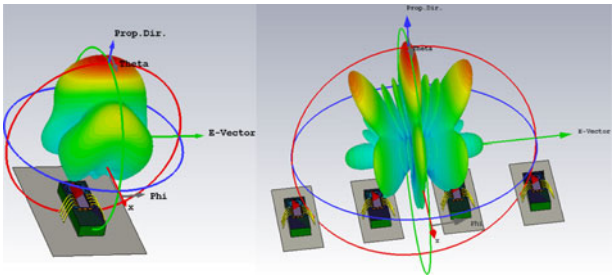


Fig. 8. Comparison between radiation patterns of a single element and the 1 × 4 array.

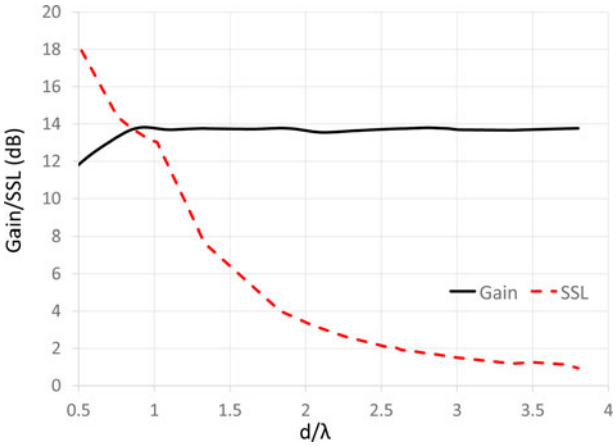


Fig. 9. Gain and Sidelobe Suppression Level (SSL) versus normalized element spacing, 1 × 2 array.

of amplitude mismatch on the radiation pattern. The change can be seen mostly on the sidelobe level, but there is also a small mainlobe decline.

Design

J-Band array

The starting point of this research was the development of the J-Band radiating source [6] and further interest to develop a solution for an array implementation in sub-THz bands. The previous paper showed remarkable results for single chip, with effective isotropically radiated power (EIRP) over 10 dBm and total radiated power (TRP) of 0 dBm with 15 GHz bandwidth. As in the single chip case CST software was used to simulate and estimate the performance of the ring antenna array in the CMOS structure environment. In Figure 8 simulation results are presented to compare the patterns of one versus four elements. Measurements for single chip showed a slight shift from simulation results, and the maximum gain was achieved for 287 GHz instead of 275 GHz, received in the simulation.

Usually, in uniform arrays, the distance between the elements should be $\lambda/2 \leq d \leq \lambda$ for the energy to be concentrated around the broadside direction. In Figure 9 one can see the gain and the sidelobe suppression level versus element distance. The dependence of the gain on the spacing is also shown in Equation 9. It can be seen that spacing larger than λ causes no increase in gain but a rise in a sidelobe level. Thus, implementing an array with element spacing close to $\lambda \approx 1$ mm is a good point

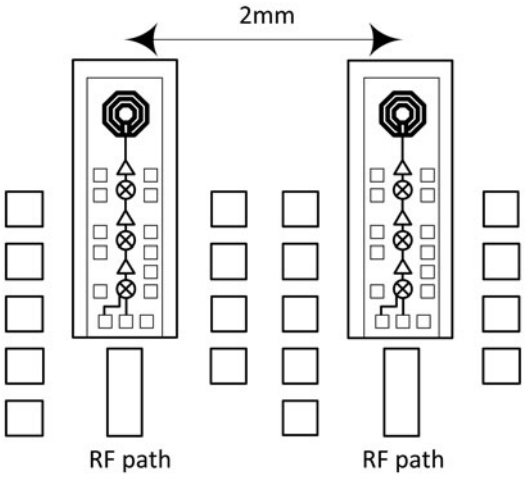


Fig. 10. Drawing of the array elements environment. The DC supply pads are located on the PCB, near each element.

in terms of both array gain and grating lobe suppression. However, as can be seen in Figure 10, DC pads located between the elements placement on the PCB determine the minimum element spacing. Due to manufacturing process constraints on minimum via/metal dimensions, the minimum element spacing of the array is set to 2 mm.

$$G(\phi) = |1 + e^{jkdcos\phi}|^2. \quad (9)$$

Feeding network

In this subsection, the design of an array feeding network is described. Keeping in mind that output port isolation, return loss, and insertion loss combined with wide bandwidth are a priority, Wilkinson Power Divider topology has to be considered. As in previous discussions, the designer has to decide whether to implement it on-board or on-chip, combining the feeding network with array elements to a single chip. The on-chip solution has major drawbacks in terms of circuit area and element replacement. Nevertheless, this approach is described in [14, 15] with several improvements. Implementing WPD on PCB has several degrees of freedom, including substrate thickness and material properties. Several papers describe microstrip implementation of X-Band WPDs [16, 17], with different improvements from the original work [18].

For the reasons mentioned above, on-board WPD topology was selected as an X-Band divider for the array. Keysight Advanced Design System was used for initial design and CST MWS for pre-manufacturing EM simulations. In Figure 11 the basic diagram of the 1 × 4 array is presented. In pursuit of minimum micro-via pad diameter and low dissipation factor, a multilayer Panasonic R5775 K (Megtron6) laminate was chosen. The PCB layer structure and the WPDs dimensions and design were optimized to obtain 50 Ω at all ports. In Figure 12 layer structure of the PCB is presented. This is not the best solution, considering the fact that the output ports are connected to the array through bond-wires (usually having a much higher inductive impedance). The reason for the 50 Ω optimization was to simplify the characterization of the power divider breakouts. Considering the large Surface-mount assembly (SMA) connector dimensions, relative to the output ports spacing, the divider breakout boards had to have a single output, with all the others terminated by 50 Ω Surface-mount device (SMD) resistors.

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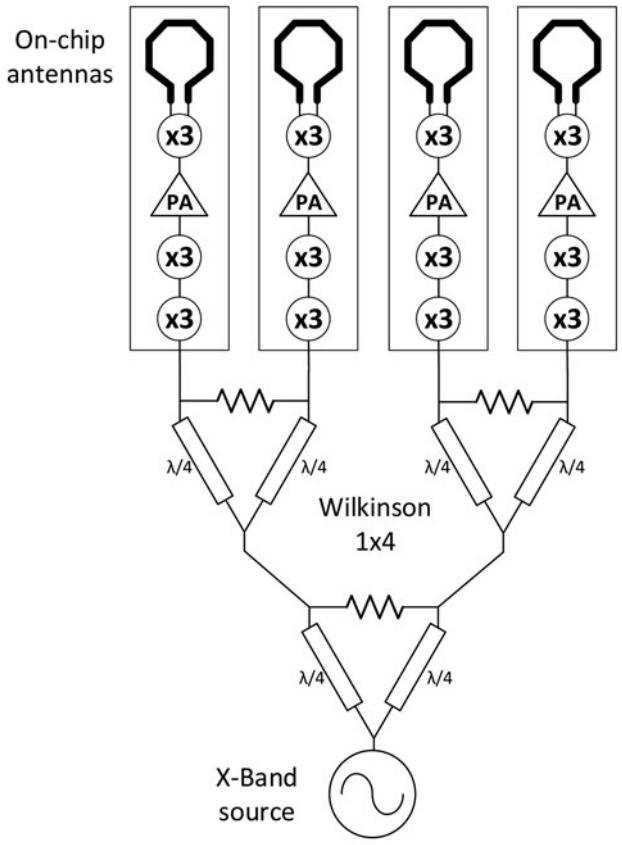


Fig. 11. Drawing of 1 × 4 Wilkinson Power Splitter feeding the J-Band array. This is a basic electrical diagram of the implemented system, from the source to the radiating array elements.

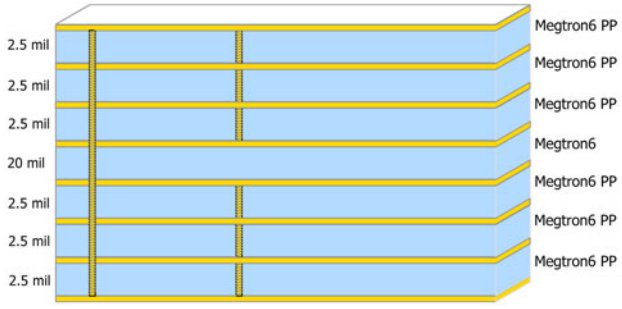


Fig. 12. Stack-up of the PCB structure. There is a single core layer with three prepreg layers from each side.

Measurement results

Feeding network

In this subsection, we present the results of the measurement boards of the four-way and two-way Wilkinson dividers and compare them to simulation. As was mentioned above, the initial boards were designed to feed the array elements, however, in order to measure the power divider by themselves, we needed to terminate all of the output ports, except one, with 50 Ω resistors. This effectively converted the 4-Way and the 2-Way WPDs to a 2-Port devices. The characterization setup of the 4-way divider breakout board is shown in Figure 13. The measurements were made with Network Analyzer (Agilent E8361C). The

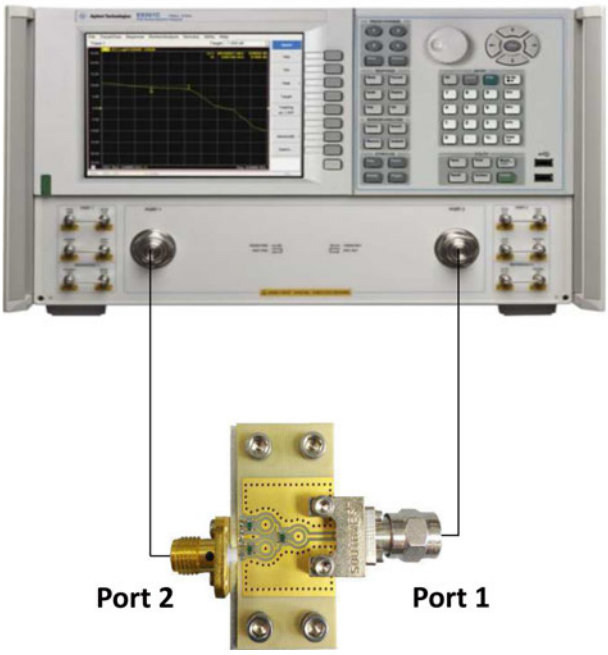


Fig. 13. Diagram of the four-way Wilkinson measurement board setup.

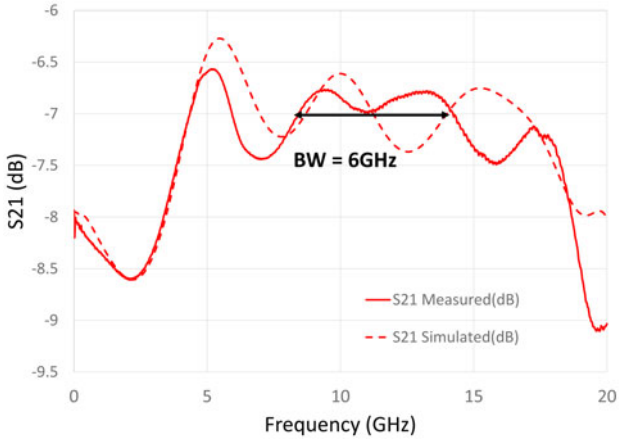


Fig. 14. Simulation and measurements results of S_{21} for 1 × 1 Wilkinson power divider.

calibration was conducted using short-open-load-thru kit (50 Ω load) for the two ports of the Performance Network Analyzer (PNA). After the calibration process, the transmission parameters of the 2-Port devices were measured.

Figures 14, 15, 16 present both simulated and measured results of the S_{21}, S_{11}, and S_{22} parameters. The return loss for both ports achieves high bandwidth, with 8–15 GHz and 3.5–14.2 GHz below −10 dB for port 1 and port 2, respectively. The insertion loss shows a slightly lower bandwidth with loss below 1 dB in 8.3–14.5 GHz range. The overall bandwidth of the 4-Way Divider is 5.9 GHz, which is roughly 53% for 11.1 GHz central frequency.

J-Band array

After ensuring the proper functionality of the feeding WPD network the chips were glued with conductive epoxy to the board.

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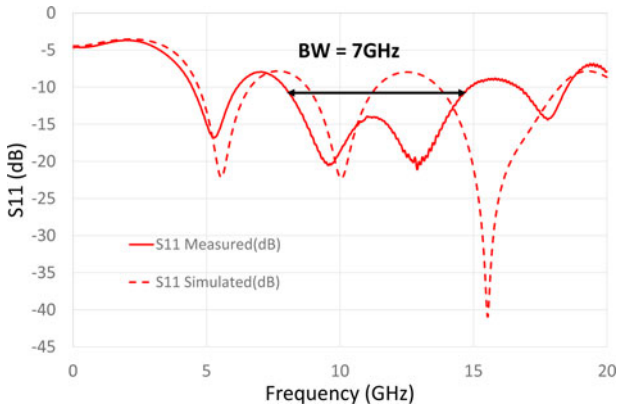


Fig. 15. Simulation and measurements results of S_{11} for 1 × 1 Wilkinson power divider.

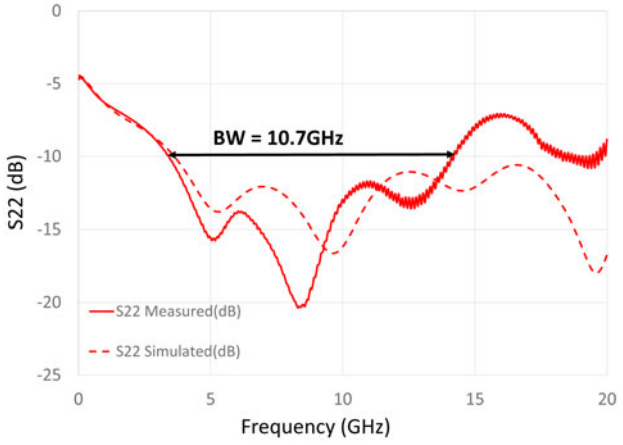


Fig. 16. Simulation and measurements results of S_{22} for 1 × 1 Wilkinson power divider.

Bond-wire connections were created for DC and RF. For signal connections two bond-wires were used in parallel to lower the impedance and to bring it closer to 50 Ω. In Figure 17 the 1 × 4 array board photographs are shown.

Figure 18 presents the measurement setup diagram and photograph. The measurements were conducted using the VDI WR3.4MixAMC downconverter with an open waveguide input that operates in the 220–330 GHz range. The received signal was downconverted to VHF band and recorded using a Keysight spectrum analyzer. The array board was fixed on a rotating stand and its position was gently tuned to achieve maximum power used for EIRP calculation. This procedure was repeated for several distances and multiple boards. For TRP measurements wide area scans were performed. The results in Figures 19, 20, 21 show the comparison of *E*–*H* planes for three elements configuration. The *E*-plane measured beamwidths of a single element, 1 × 2 and 1 × 4 arrays are 23°, 14°, and 6.1°, respectively, with an error of 2, 5, and 10% from the simulation results.

In the implemented J-**b**and arrays, compared with a single J-**b**and chip in Table 1, the 1 × 2 array achieved an EIRP higher by 5.3 dB, very close to the ideal 6 dB. The 1 × 4 array, however, achieved only a 7.2 dB boost in the EIRP. The measured radiation patterns matched the simulations nicely, showing the narrowing of the beam in the *E*-plane as the number of elements in the array increases and only minor effects on the *H*-plane pattern.

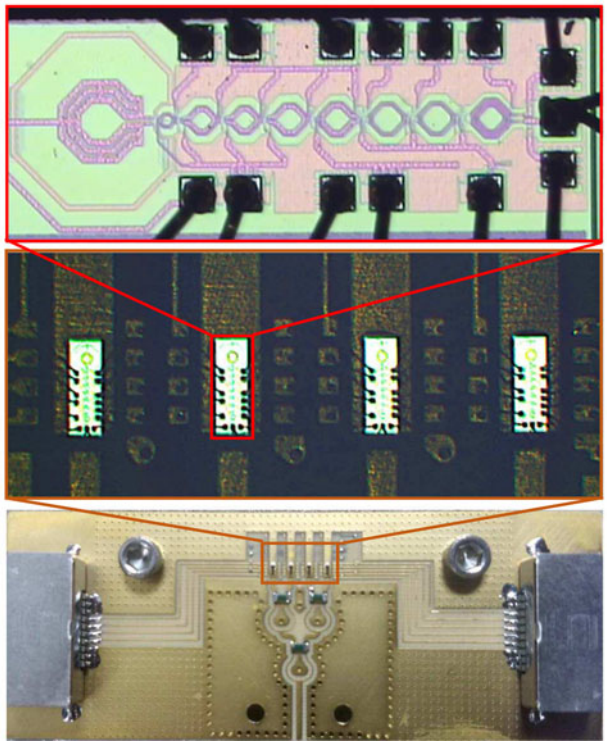


Fig. 17. Photographs of the assembled 4-way divider circuit with radiating elements.

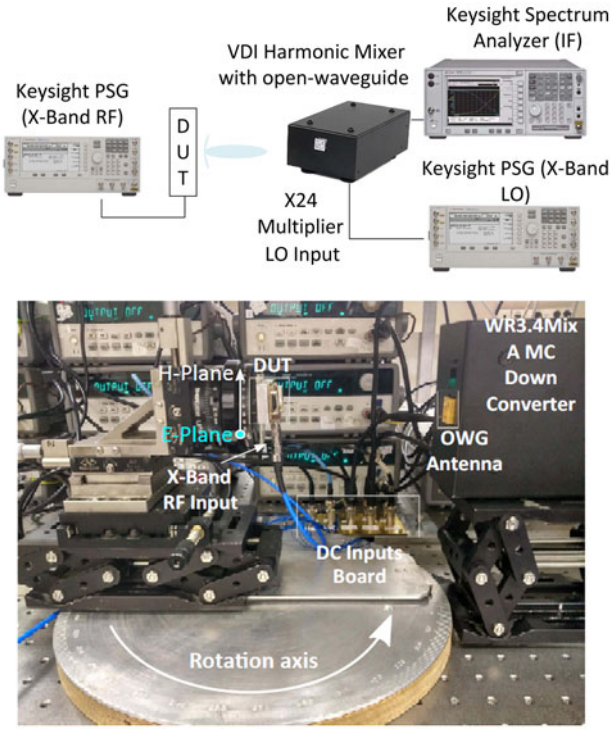


Fig. 18. Diagram and a photograph of the setup for measuring the J-Band array performance.

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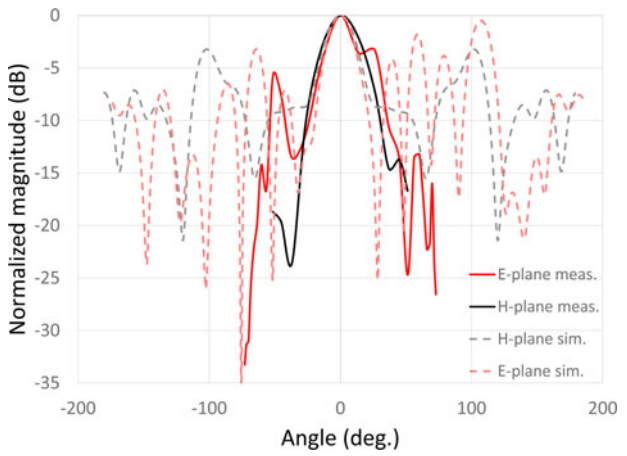


Fig. 19. *E–H* planes normalized radiation pattern comparison plot of a single chip. The plot shows the measured (continuous lines) versus the simulation (dashed lines) results.

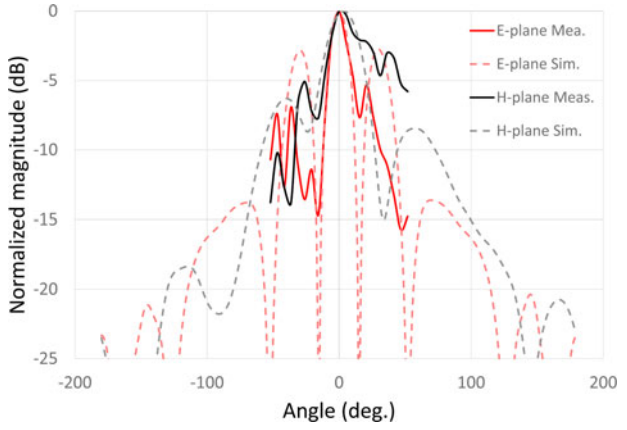


Fig. 20. *E–H* planes normalized radiation pattern comparison plot of the 1 × 2 array. The plot shows the measured (continuous lines) versus the simulation (dashed lines) results.

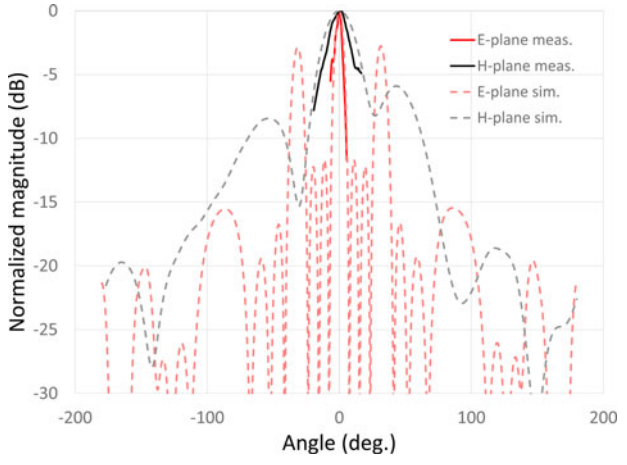


Fig. 21. *E–H* planes normalized radiation pattern comparison plot of the 1 × 4 array. The plot shows the measured (continuous lines) versus the simulation (dashed lines) results.

Table 1. EIRP results for different element configuration. The ideal result stands for the 6 dB theoretical addition expected from multiplying the elements number by two

Case	Max EIRP (dBm)	Ideal EIRP (dBm)
Single Chip	7.09	–
1 × 2 array	12.35	13.09
1 × 4 array	14.32	19.09

Table 2. Comparison with previous state of the art J-Band arrays

Parameters	This work	[19]	[7]	[20]
Array size	1 × 2/1 × 4	4 × 4	4 × 4	4 × 4
Technology	CMOS 65 nm	CMOS 45 nm	CMOS 65 nm	SiGe 0.13 um with lens
Frequency (GHz)	277–292	270–280	333–340	317
DC Power consumption (W)	0.51/0.97	0.82	1.54	0.61
EIRP (dBm)	12.4/14.3	9.4	17	22.5
Total Die Area (mm^2)	0.98/1.96	7.3	3.9	2.1
EIRP/TDA (mW/mm^2)	17.73/13.73	1.19	13.15	85.49

Conclusion

In this work, we propose and demonstrate an approach of boosting the radiated THz power generated using CMOS chip. The approach is based on integrating a 1D array of sources on a low cost multilayer PCB and distributing a relatively low (X-band) LO signal that is frequency multiplied by 27 and amplified before being radiated using an on-chip antenna in 65 nm CMOS chips. Arrays of 1, 2, and 4 chips were designed and demonstrated. For the X-band input signal distribution, a Wilkinson power divider has been designed and demonstrated. Better matching between measured and simulated results was achieved using the bottom layer as the ground. The measurement results for 1 × 2 and the 1 × 4 WPD show close correlation with simulation, demonstrating a bandwidth of 53% around 11.1 GHz.

The array measurements showed a correlation between measured and simulated radiation patterns. According to theory, placing an array along the *x*-axis results in narrowing of the beam in the *E*-plane direction. Demonstration of that narrowing in measurement demonstrates the coherent array effect in our implementation.

Modeling and simulation show how close element proximity can result in antenna coupling and array degradation. EIRP can also be degraded by the variance in each element phase and magnitude. This variance is enhanced by the multi-stage chain in each element and the total ×27 frequency multiplication. As the number of elements in the array increases, variance and yield issues are more pronounced. Magnitude and phase trimming per channel are thus needed for future designs. This addition will also enable beam steering.

Table 2 shows J-Band state of the art transmitter arrays performance summary. When compared to these works, ours stand

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out as a coherent array with all the elements fed by the same source, to promise an optimal array performance. It is also worth noticing that our concept has a higher EIRP per total die area (TDA), compared to other works, without any lens boosts. Future developments will involve larger arrays and they will focus on the improvement of the manufacturing and the assembling process.

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