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A 1.5–40 GHz frequency modulated continuous wave radar receiver front-end

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Research Paper

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Abstract

This study presents an ultra-wideband receiver front-end, designed for a reconfigurable frequency modulated continuous wave radar in a 130 nm SiGe BiCMOS technology. A variety of innovative circuit components and design techniques were employed to achieve the ultra-wide bandwidth, low noise figure (NF), good linearity, and circuit ruggedness to high input power levels. The designed front-end is capable of achieving 1.5–40 GHz bandwidth, 30 dB conversion gain, a double sideband NF of 6–10.7 dB, input return loss better than 7.5 dB and an input referred 1 dB compression point of −23 dBm. The front-end withstands continuous wave power levels of at least 25 and 20 dBm at low band and high band inputs respectively. At 3 V supply voltage, the DC power consumption amounts to 302 mW when the low band is active and 352 mW for the high band case, whereas the total IC size is 3.08 nm^2.

Introduction

The increasing demand for software defined, wideband, multi-functional radar systems requires innovation and novel ideas on how to overcome certain physical and design challenges. Wideband radar systems enable achieving a good range resolution, furthermore an ability to have a re-configurable system allows for complying with various international frequency allocation standards. The reported State of the Art (SotA) wideband radar Receiver (RX) front-ends typically cover the frequencies below the X band, or between the X and Ka bands [1–6]. However, to the best knowledge of the authors, there has been no RX front-end reported that would be able to continuously cover C–Ka bands and furthermore, to be designed robust up to 20–25 dBm input power levels. In this study, a robust (RX) front-end for a software defined, ultra-wideband, frequency modulated continuous wave (FMCW) imaging radar was investigated and designed. The chosen application of multiple input, multiple output (MIMO) radar topology with co-located antenna layout required a number of design solutions and trade-offs. Special attention was drawn toward the input power ruggedness, integration, direct current (DC) power consumption, linearity and the direct path issue. Next to that, the typical design challenges, such as flat Conversion Gain (*CG*) response and low noise figure (*NF*) were tackled. This paper focuses on the final design of the RX front-end unit. Initially, in section "General architecture" the general front-end architecture is discussed, section "Front-end IC" addresses the design of each front-end component and section "RF switch and active balun" presents the RF board design. Finally in section "Measurement results and discussion" the measurement results are demonstrated, followed by the conclusion in section "Conclusion." Insights on the improvements done on certain components from the their very first versions are given in the text.

General architecture

Due to limited antenna bandwidth, the input was divided into low band (LB) and high band (HB) channels. The frequencies were chosen respectively 4–12 GHz for the LB and 10–40 GHz for the HB. Because of the chosen FMCW radar topology with co-located antenna layout, the direct path issue was addressed in the following ways. For both (LB and HB) channels the gain of the low noise amplifier (LNA) circuits was chosen to be variable, ranging from 0 to 12 dB. This allowed for turning the LNA in a low gain mode and hence preventing saturation, when a nearby co-located Tx antenna is actively sending. This is because it is not possible to perfectly isolate the Transmitter (TX) and RX antennas in a wide frequency range and hence there is always a coupling between the TX and RX antennas – the so-called direct path. In case the RX front end is prevented from saturation due to the direct path signal, when the closest TX antenna is transmitting, the signals can be processed. For an extreme case the LB and HB inputs were chosen to be designed outstandingly rugged. With a dedicated choice of LNA topologies input power ruggedness up to 20 dBm could be reached. An additional

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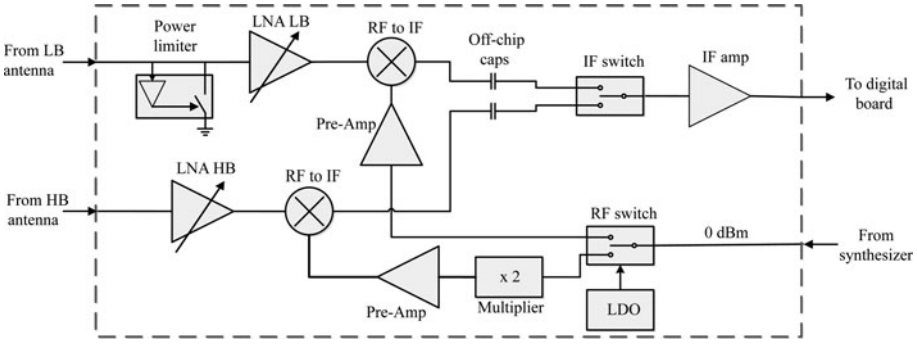


Fig. 1. Top level view of the RX front-end unit.

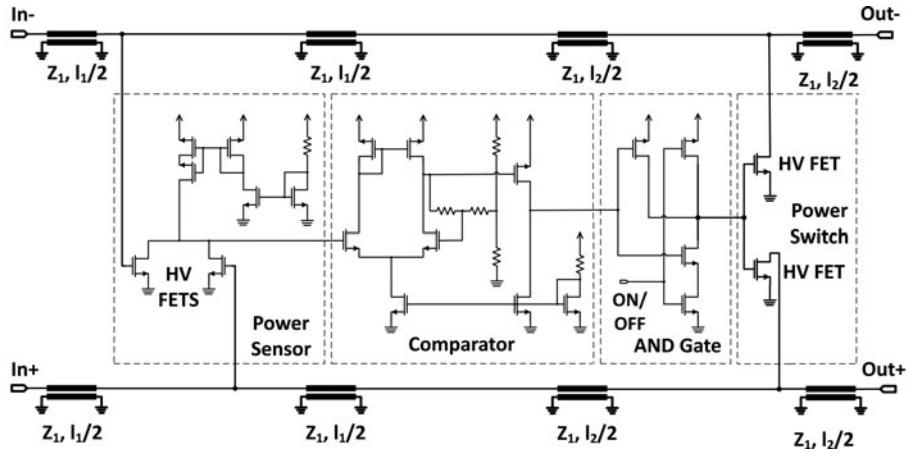


Fig. 2. Design topology of the active power limiter. $Z_{1,2}$ is the resulting characteristic wave impedance, $l_{1,2}$ is the length of the corresponding TL [7].

power limiter was introduced in the LB channel. This enabled increasing the input power ruggedness at least up to 25 dBm.

To enable a wide frequency tuning range, an *N*-fractional phased locked loop functioning from 4 to 20 GHz was employed. For the LB channel a frequency of 4–12 GHz without any conversion is provided. For the HB channel on the other hand, a frequency doubler is used to acquire 10–40 GHz from a 5–20 GHz input. The lower and upper intermediate frequency (IF) limits are defined with respect to the frequency chirp duration, steepness, the required minimum and maximum detection range and the resulting frequency of the direct path signals. The chosen IF bandwidth is therefore 10–100 MHz. This condition implies that off-chip blocking capacitors shall be used to effectively block the lower IF frequencies ranging from DC to 10 MHz. The IF switch selects between the LB and HB channel and the signal is then amplified to drive the analog to digital converter (ADC). The gain of the IF amplifier is defined with respect to the input voltage handling capabilities of the chosen ADC, it's input impedance and the measurement speed, determined by the number of averaging samples. For the case of the received direct path signal, the input voltage of the ADC should not exceed its peak-to-peak level, whereas on the other hand the smallest received signal should be amplified sufficiently, so that after performing the fast Fourier transformation, it could be extracted from the noise with a reasonable number of averaging samples. The top level schematic of the Rx front-end is presented in Fig. 1. To address the design challenges, such as the ultra-wide bandwidth, high degree of integration and complexity, a SotA 130 nm silicon germanium (SiGe) BiCMOS technology was chosen. Some of the components to be discussed, namely power limiter, LNA, mixer, and frequency doubler have been published in the past study [7–9], whereas the others are introduced here for the first time. This system-level paper is dedicated to demonstrate the design of the overall RX front-end. A brief description will be given for each component seen in Fig. 1 in a dedicated subsection and finally the measurement results of the whole Rx front-end will be presented.

Front-end IC

Power limiter

At the low frequencies, to protect the circuits from external large signals, which could tentatively destroy the hardware, the power limiter was employed. Typically the power limiter circuits consist of a reversely biased diode. However, the disadvantage is that such diodes typically introduce large input capacitance, which degrade the input and noise matching. Compensation for such capacitance in a broadband operation becomes impossible, especially because there is a limitation in cut-off frequency of the arbitrary transmission lines (TLs). To minimize the circuit input capacitance introduced by the power limiter, a novel active power limiter architecture was designed (Fig. 2). The circuit consists of a power sensor, comparator, AND gate and a power switch.

All these components are designed by using high-voltage field effect transistor (HV-FET) devices to ensure no breakdown occurs in the power limiter itself. The circuit is implemented under large cross-section TL structures, which are designed for both to match the capacitance introduced by the power limiter and to be able to accommodate large impinging currents. The circuit functionality

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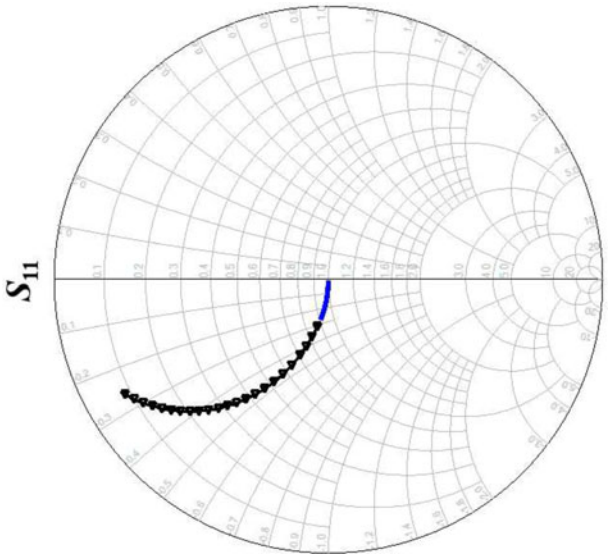


Fig. 3. Impact by the parasitic capacitance, modeled in the 50 Ω domain. Solid blue: active power limiter, black triangles: equivalent performance diode limiter 1.5–18 GHz [7].

can be described as follows: the power sensor initially has a high DC potential at the output. In case an input power exceeding a certain threshold is applied, the HV-FET devices at their inputs are switched on and the DC output voltage of the power sensor drops. The comparator circuit is used to create a hysteresis and by this means to protect the power limiter from switching on and off at a single power level. The AND gate is an optional circuit, allowing externally to switch the active power limiter off. If the comparator provides a low signal, it gets then inverted by the AND gate and is further passed to the power switches and the power switches ground the signal. In case of an impinging small signal the power switches remain closed and create an open, letting the signal pass to the LNA. The total parasitic capacitance introduced by the proposed active power limiter topology in off-state can be approximated as follows: $C_{Sensor} + C_{Switch} = (C_{GD} + C_{GS}) + (C_{DB} + C_{GD})$. C_{Sensor} and C_{Switch} describe the capacitance introduced by the power sensor and the power switch, C_{GD}, C_{GS}, and C_{DB} are the gate–drain, gate–source, and the drain–bulk capacitances of the HV-FET devices respectively. For small impinging signals the power sensor and the power switch transistors are in the off state. Hence, the major capacitance C_{GS} disappears due to the lack of carriers in the channel. This strongly reduces the overall capacitance introduced by the active power limiter for the low impinging power case. An approximation can be done: $C_{Sensor} + C_{Switch} = 2 \times C_{GD} + C_{DB}$ [7].

Considering a passive diode based power limiter on the other hand, two diodes one forward biased and one reverse biased are needed to absorb the positive and negative half-waves. Hence, in contrast to the proposed topology, the parasitic junction capacitance remains, regardless if the impinging power is high or low. In the particular case, based on components provided within the process development kit, the power switches were modeled for a 10 dBm RF power absorption. The active power limiter introduced a total parasitic capacitance of 52 fF in off-state. On the other hand, the power limiter designed from the diodes with the same power absorption performance at the frequency of interest introduced a total of 780 fF of capacitance Fig. 3 [7].

LNA

The design goal for the LNA and mixer components was to maximize the dynamic range and to yield the flat *CG* response along the 4–40 GHz bandwidth. Addressing the direct path, it is important that the LNA and mixer components remain in the linear region. The large impinging signals of the nearby object (or the direct path) are down-converted to very low frequencies and thus can be easily suppressed by simple off-chip high-pass filters on the IF side. To address the trade-off between the input power ruggedness and the ultra-wide band operation, a distributed traveling wave amplifier topology was chosen for the LNA design (Fig. 4). The topology was optimized to withstand at least 20 dBm of input power level, without any damage being made to the circuit. This was achieved by choosing large input transistor devices, large cross section TLs and wide resistors along the input signal path. With increased number of cascode stages, the linearity is enhanced, where the limitation is given by the cut-off frequency of the resulting overall input/output TL length. The optimum linearity versus noise matching versus bandwidth trade-off was found when employing four input cascode stages (Fig. 4). The matching was achieved by adjusting l_1, l_2 (Fig. 4) and the size of the blocking capacitor C_b (Fig. 5) for the given biasing condition. The length of output TLs l_2 was adjusted iteratively with respect to the chosen values of C_b and l_1. Peaking inductors L_{peak} were employed to increase the gain flatness over the bandwidth. Furthermore, with the balanced design the even harmonics could be nearly eliminated, which further enhanced the linearity.

Two topologies were designed and tested. The first one used adjusting the tail current for implementing the gain control [10]. However, the issue that this topology was facing was that reduced tail current reduces the maximum output current swings and hence linearity of the corresponding gain stage itself. To overcome this issue, a second version of the LNA was designed, where the gain control was implemented by controlling the amount of signal passing through the feedback path. Compared to the previous and other reported gain control topologies [11, 12], this approach had the advantage that when reducing the gain, the bias conditions of the LNA circuit itself remain unchanged and hence the linear operation versus the input power is strongly increased. The same LNA topology was chosen for the LB and HB channels with some difference of scaling to better address the corresponding bandwidth and expected maximum input power levels.

Mixer

Two different mixer topologies were tested. Initially a multi-Tanh input-based Gilbert cell topology [13] was chosen. The core advantage of such topology is its unique capability of spreading the g_m curve versus the input voltage. This feature is a very promising design approach for highly linear circuit designs. However, the multi-Tanh topology still suffers from a number of drawbacks. Complex circuitry is penalized by high DC power consumption. Increasing the number of input pairs does spread the g_m curve versus input voltage, but it also complicates and makes symmetrical layout impossible, causing the circuit to lose the balanced setup advantages. Broadband matching is difficult, since the input connects to high impedance and highly capacitive transistor gates or bases. The attenuation, introduced by the input source/emitter follower stage further deteriorates the noise performance. The second designed mixer topology (Fig. 6) was implemented to overcome the abovementioned drawbacks and to keep the

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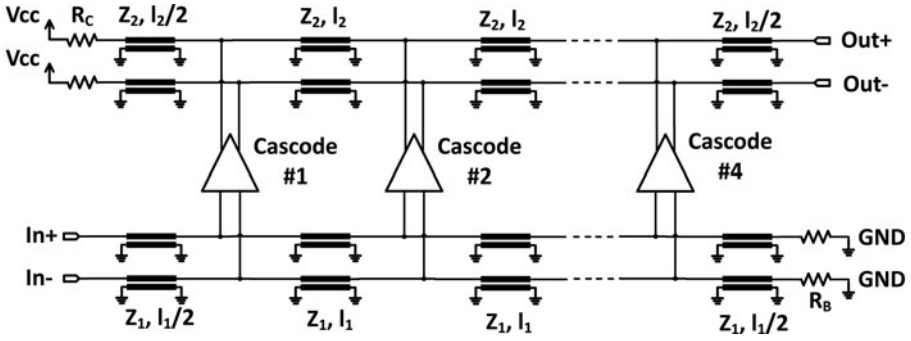


Fig. 4. Top level view of the chosen four-stage distributed differential LNA topology. $Z_{1,2}$ is the resulting characteristic wave impedance, $l_{1,2}$ is the length of the corresponding TL and $R_{B,\,C}$ denote the base, or collector loadline resistor [7].

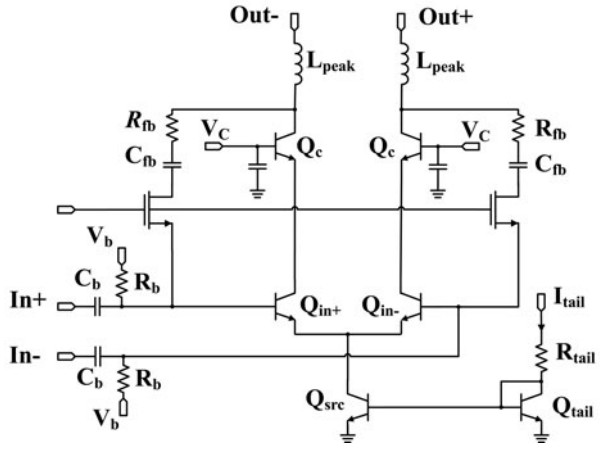


Fig. 5. Differential cascode stage with controlled feedback and inductive peaking [7].

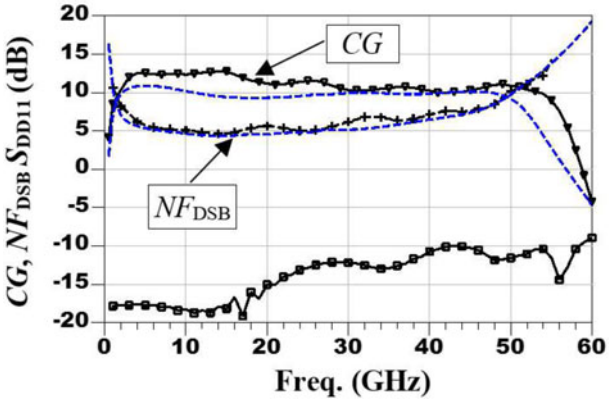


Fig. 7. Combined HB LNA and mixer. *CG* (triangles) and NF_{DSB} (crosses), S_{DD11} (squares). Measured (solid) versus simulated (dashed). IF freq. = 100 MHz, LO = 0 dBm, RF = −30 dBm, high gain setting [8].

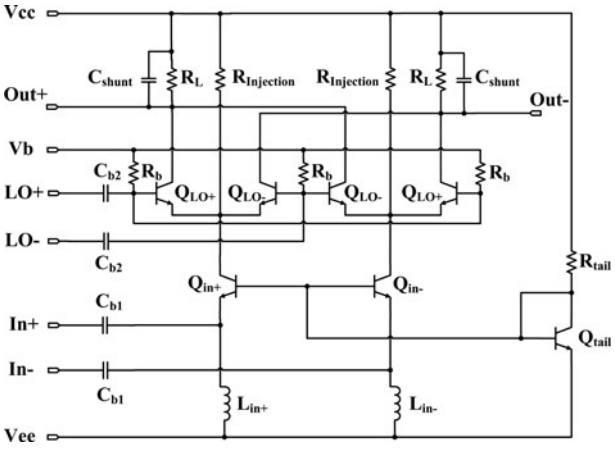


Fig. 6. Schematic diagram of the designed mixer circuit [7].

advantages of a Gilbert cell. This topology uses a simple common base input, which has a low-ohmic impedance that can be approximated as follows (equation (1)):

$$Z_{IN+/-} = \frac{1}{g_{m,\,CB+/-}} \| jwL_{IN+/-} \tag{1}$$

$g_{m,\,CB}$ describes the transconductance for a common base configuration and L_{IN} in stands for the input shunt inductance. As seen in equation (1), Z_{IN} is a function of both $g_{m,\,CB}$ and L_{IN}. Hence, Z_{IN} can be adjusted by scaling the devices (Q_{IN+} and Q_{IN-}), sizing the shunt inductances (L_{IN+} and L_{IN-}) or actively by changing the bias points of Q_{IN+} and Q_{IN-} [14]. For yielding the optimum broadband noise matching, the input impedance was adjusted with respect to the simulated Z_{OPT} [8].

Furthermore, it can be demonstrated that in a hetero-junction bipolar transistor (HBT) most of the harmonics are generated in the base–emitter junction [15], therefore injecting the input signal into the emitter gives a more linear behavior. In addition to that the shunt input inductors $L_{IN}+$ and $L_{IN}-$ are modeled to create a short (by reaching the resonance frequency) for harmonic waves above the fundamental frequencies in this way adding to the linearity of the circuit. The output is shunted with capacitors C_{SHUNT}, which serve for grounding the RF and LO leakages, whereas the charge injection resistors $R_{Injection}$ serve for higher gain. The simplistic topology allows for an easy, symmetrical layout and no buffers are needed for the impedance matching. Some major measured performance figures of the stand-alone LNA and mixer combination ICs are presented below (Figs 7 and 8) [8].

The LB LNA plus mixer circuit was fabricated combined with the active power limiter. Its performance was assessed by increasing and then decreasing the power level of the input signal (Fig. 9). More details about the active power limiter can be found in [7].

Frequency doubler

Frequency doublers are usually designed by using differential pair, bootstrapped mixer, or even distributed topologies [16–18].

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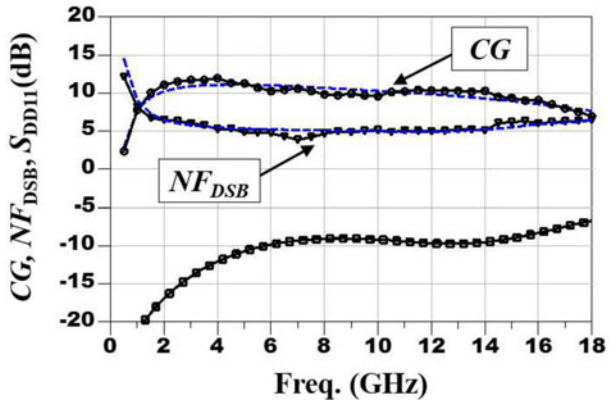


Fig. 8. Combined LB active limiter, LNA, and mixer. *CG* (triangles) and NF_{DSB} (crosses), S_{DD11} (squares). Measured (solid) versus simulated (dashed). IF freq. = 100 MHz, LO = 0 dBm, RF = −30 dBm, high gain setting.

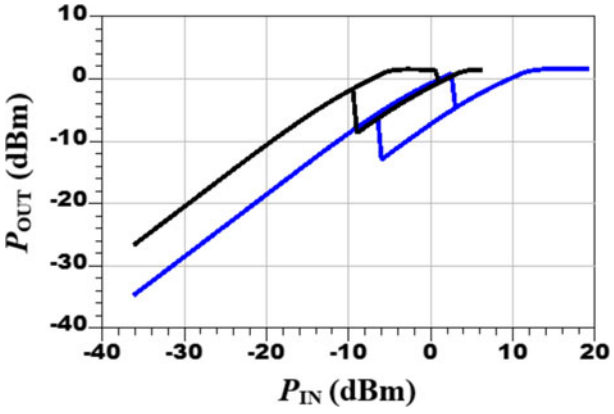


Fig. 9. Combined active limiter, LNA, and mixer. Measured P_{OUT} versus P_{IN}: high gain setting (black) and low gain setting (blue). RF freq. = 10 GHz, IF freq. = 100 MHz, LO power = 0 dBm [7].

However, all these topologies suffer either from very high DC power consumption, low bandwidth, or poor harmonic rejection ratio. To overcome the wideband matching problem and to inherently implement a good fundamental and harmonic frequency rejection ratio, a balanced, ultra-wideband, and very simple frequency doubler technique was designed (Fig. 10).

The quasi-passive topology utilizes the diode connected HBT devices and resistors to set the operational point. With the symmetrical design, the frequency doubler strongly suppresses the fundamental and the odd harmonic frequencies, leaving just the signals at $2 \times f_0$ and the $4 \times f_0$. The fourth harmonic frequency is spectrally far apart and in some applications, can be suppressed by filtering. Alternatively, adding a fully balanced amplifier on the output the fourth harmonic could be strongly suppressed. More information about the circuit can be found in [9].

RF switch and active balun

Two versions of the RF switch and active balun circuit were designed. The first version stood out for its good isolation and flat G_T response, however the relatively low amplitude and especially phase imbalance was considered critical for directly using it as an LO driver of a Gilbert cell type mixer [19]. The second

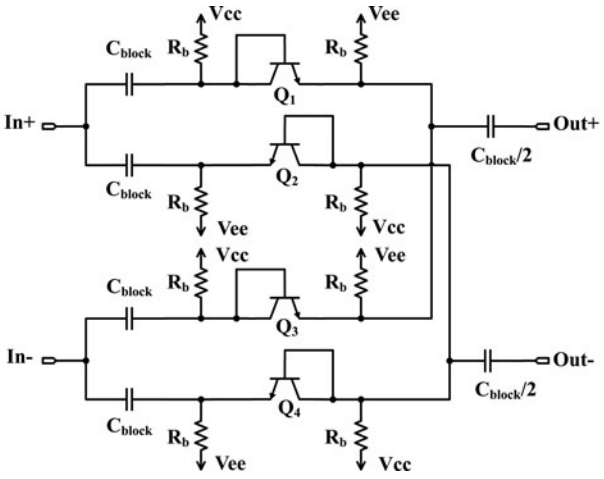


Fig. 10. Chosen ultra-wideband, balanced frequency multiplier topology [9].

version was designed to address these issues. Next to some further layout optimization, additional fully balanced large signal amplifiers at the LB and HB outputs were added. These amplifiers were optimized for the corresponding 4–12 GHz and 5–20 GHz frequencies and a good common mode suppression to minimize the phase and amplitude imbalances. In addition for minimizing the DC power consumption and to improve the isolation, these amplifiers feature tail current deactivation (Fig. 11). In case an LB channel is active, the tail current of the HB amplifier is switched off, preserving the circuit from drawing DC power and turning the deactivated HB large signal amplifier into an attenuator. This further improves the isolation of the deactivated LB, or HB channel. Furthermore, two extra inverters are employed in order to fully push, or pull the control signal to GND, or V_{DD}. By adding the two dedicated fully differential amplifiers, the G_T could be increased by approximately 11 dB. Due to biasing the differential amplifiers with a supply voltage of 3 V, rather than 2 V as is done for the RF switch itself, the saturated output power of the combined circuit was increased from −1 to 2.3 dBm. This enabled a better driving of the LO input on the LB mixer side and the frequency multiplier on the HB side. Furthermore, due to the increased G_T, the output power saturation was reached at the input drive level of approximately −7 dBm. This gave an advantage that the mixer and the frequency multiplier circuits and hence the RX front-end performance became less sensitive to the LO power level applied. This effect will be shown in the final front-end measurement results. The simulated phase and amplitude imbalance is presented in Fig. 12.

Low drop-out regulator

The LDO circuit is employed as a protection helping to keep the RF switch transistors from reaching the collector–emitter breakdown voltages V_{CE0} when in the off state. The schematic of the LDO circuit is presented in Fig. 13.

The supply voltage (V_{supply}) is reduced by the output resistance of the transistors (M_9 and M_{10}). These are controlled by the two-stage amplifier with a feedback to ensure a constant output voltage (V_{output}). Two voltage dividers, consisting of R_1, R_2 and R_3, R_4, placed at the input of the amplifier are used to set the required output voltage (V_{output}) level. A capacitor C_{Stab} of 16 pF is

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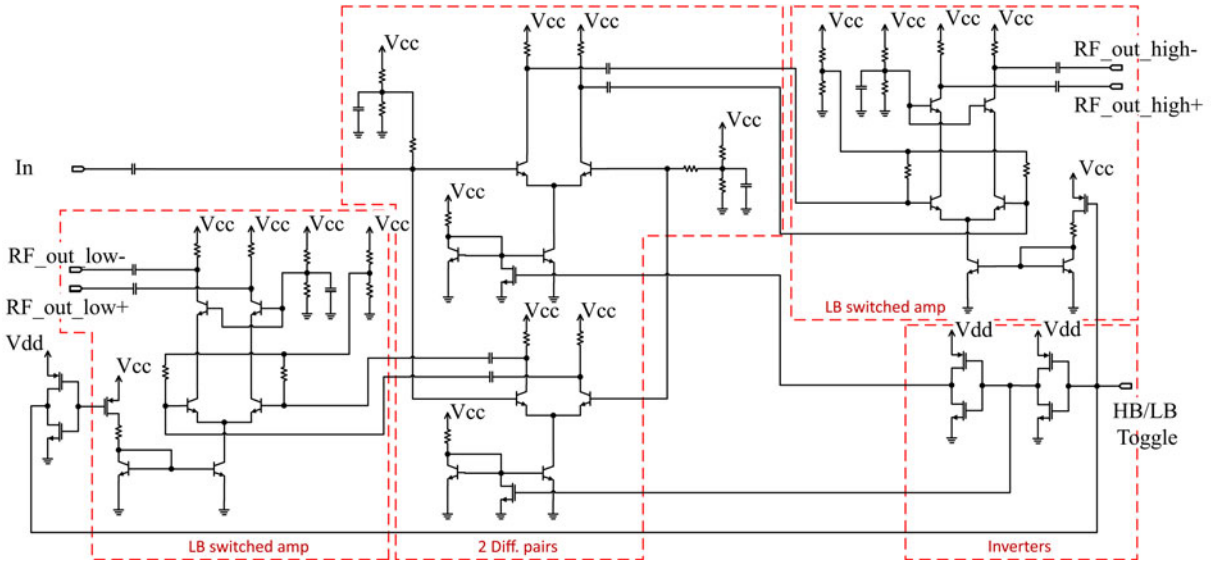


Fig. 11. Schematic diagram of the second version RF switch and active balun IC.

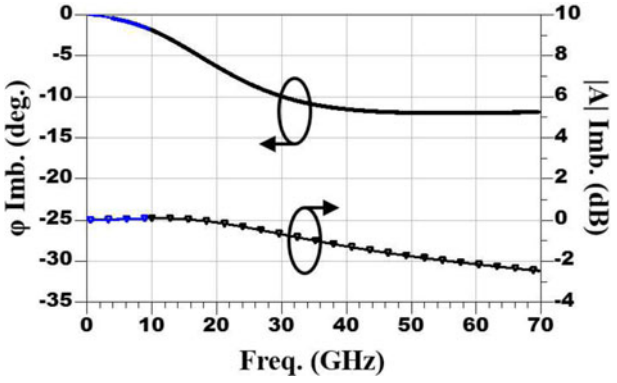


Fig. 12. Simulated (ϕ) imbalance (left Y -axis, solid) and $|A|$ imbalance (right Y -axis, triangles), LB (blue) and HB (black) respectively.

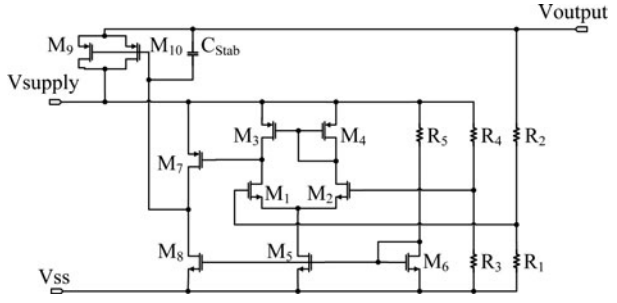


Fig. 13. Simplified schematic of the LDO circuit.

employed to assure the stability of the feedback circuit. Simulation results are presented in Fig. 14.

It can be seen that after switch on, it takes some time for the output voltage to set to the required 2 V reading. This is because the large stabilizing capacitor (C_{Stab}) needs to be charged. The value of C_{Stab} can be decreased, however this would reduce the gain/phase margin and is not a necessary condition for a constant ON operation.

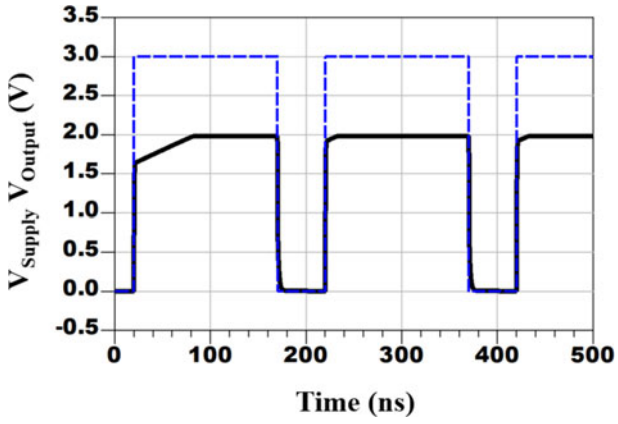


Fig. 14. Simulated time domain performance of the LDO circuit. Output voltage (solid) versus input voltage (dashed, blue).

IF switch and IF amplifier

For addressing the 10–100 MHz frequency range, HV-FET devices could be chosen for the design. This gave the advantage of being able to choose a higher supply voltage, ranging from 3 to 5 V. Choosing 5 V supply voltage enables larger output voltage amplitudes without driving the IF amplifier into compression. In such a way larger direct path signals can be handled by choosing an ADC with corresponding maximum peak-to-peak input voltage. In this way the dynamic range of the Rx itself is improved. Due to the single-ended input of the ADC, the output of the IF switch and IF amplifier circuit was chosen to be single-ended. The chosen topology of the IF switch is presented in Fig. 15. The IF switch consists of two differential pair circuits, one for the LB signal (marked on the left side of the schematic) and one for the HB (marked on the right side respectively) and the inverters for selecting between the LB, or the HB channels. In order to enhance the gain compression, a common gate input configuration is employed. The switching between the LB and HB is implemented by controlling the bias of the input

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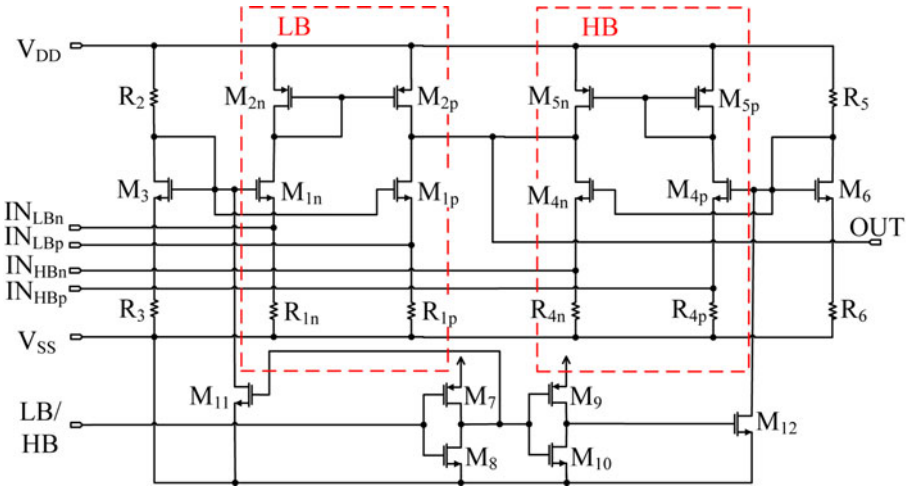


Fig. 15. Simplified schematic view of the designed IF switch circuit. The LB part is circled left and the HB circled right.

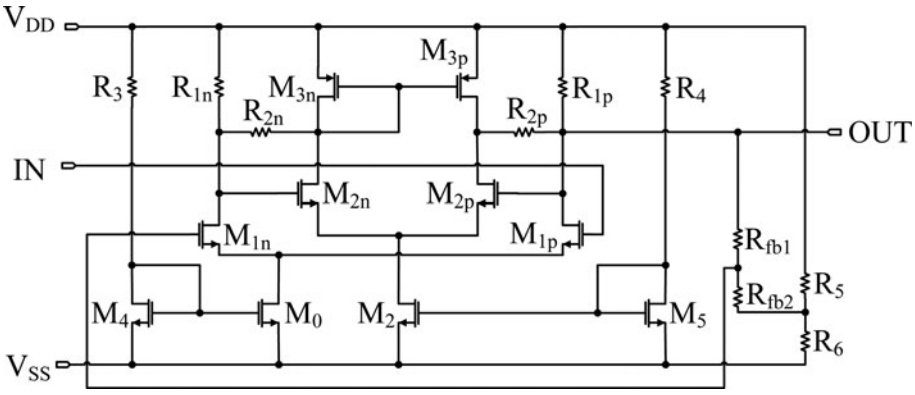


Fig. 16. Simplified schematic view of the designed IF amplifier circuit.

transistors. To maximize the high- and low-switching voltage amplitudes, two inverter pairs are employed. In case the LB signal is needed, a logic 1 (3–5 V) is applied to the LB/HB input, in this way activating the LB differential pair and fully shutting off the HB differential pair. The chosen circuit topology is presented in Fig. 16. A two-stage topology with a resistive feedback was employed to enable a flat gain response. A differential configuration was chosen, where one side of the differential pair is connected to the input and the other is used for the feedback. The resistive feedback is employed to make the gain of the circuit more stable against temperature variations.

Rx front-end IC

The designed components were combined into a single RX IC unit. The fabricated IC photograph with denotations is shown in Fig. 17. The HB input is seen at the bottom left, whereas the LB input is placed in the middle right. Both, LB and HB input GSGSG pads are placed on the bottom side with some distance apart, this is for the reason to have sufficient spacing between the on-board differential TLs. On the HB side, the first component is the variable gain LNA followed by the mixer component. The down-converted signal is routed to the output of the IC to the off-chip capacitors for high-pass filtering. The same approach is seen on the LB side, with one difference that the first component here is the active power limiter. The LO input is located on the top side of the IC in order to separate the on-board LO TL from the LB and HB inputs. The 4–20 GHz LO signal is passed to RF switch, and commuted either to the LB or the HB channel. In case the HB channel is active, the LO signal is passed to a frequency doubler to up-convert the frequency from 5–20 GHz to 10–40 GHz. The following fully differential amplification stage is responsible for boosting the signal amplitude above 0 dBm and to reduce the amplitude and phase imbalances. The same approach is seen on the LB channel, with the difference that no frequency multiplication is required. On the right side of the IC, the IF switch and IF amplifier circuits are seen. With one input being activated at a time, it chooses whether the LB, or the HB signal is passed through, or attenuated and amplifies it to the required power level to drive the ADC input. On the top right side, the IF output pads are seen and on the right bottom side the control and bias voltage inputs are located.

RF printed circuit board design

A four-layer Rogers 4350 substrate was chosen for the RF board design. The upper two layers were used for RF and the lower two layers for the DC routing. To reduce the effect of the parasitic bond wire inductance, a cavity with a depth equal to the IC die thickness was used. The bond-wire interconnections between the IC and the RF board were modeled and assessed with a 3D electro-magnetic (EM) simulator (Fig. 18).From bottom left to bottom right, the HB and LB inputs are seen. These are connected to on-board differential TLs with tapered ends toward the IC. The tapering was required due to a limitation in pitch and minimum TL width, defined by the PCB technology. The coplanar ground

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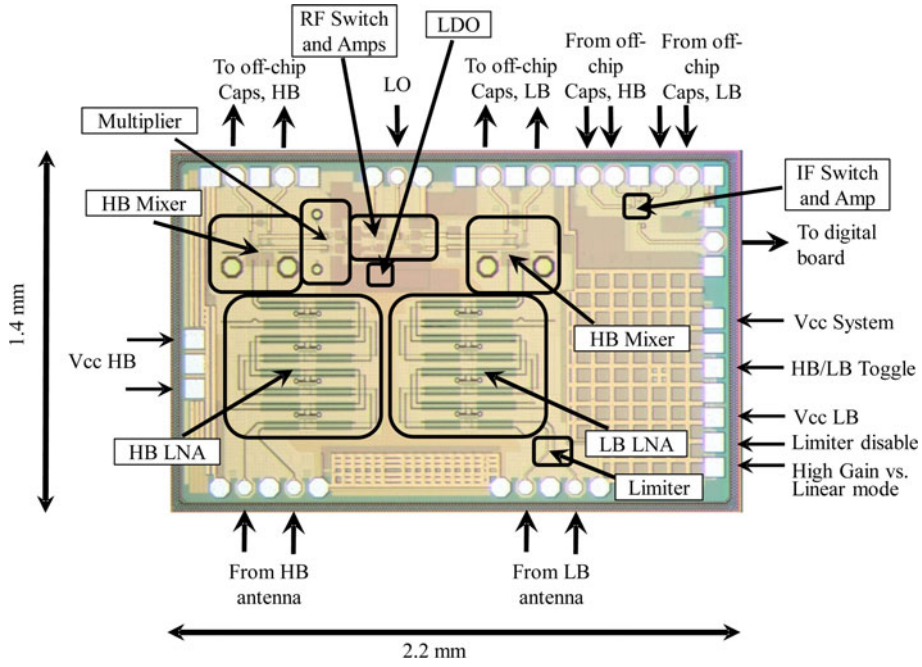


Fig. 17. Microscopic view of the designed RX IC with denotation of separate components.

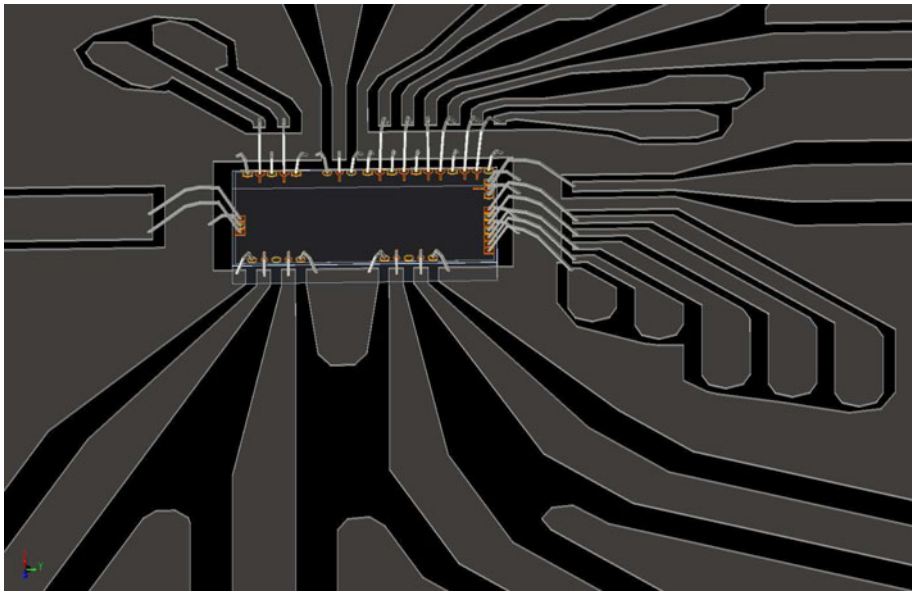


Fig. 18. 3D view of the RF board and the RX IC.

between the TLs was introduced after the tapering as it could fit between the TLs. This discontinuity in terms of characteristic wave impedance was assessed by means of EM simulations and optimized by adjusting the coplanar ground clearance and the tapering itself. On the top side of Fig. 18 the LO input is seen. The DC power supply and control signals were routed on the lower two layers of the board and connected to a header. The IF output is seen on the top right side. Wideband 1.85 mm standard edge launch V-connectors were chosen for the design. The off-chip high pass filtering was implemented by employing 0.5 nF surface-mounted device capacitor. The overall losses associated with the RF board will be presented with the measurements. A photograph of the finalized RF front-end is presented in Fig. 19.

Measurement results and discussion

With the purpose to evaluate the performance of the IC itself and the losses associated with the RF board and bonding, initially the LB and HB inputs were probed, whereas the remaining connections were bonded. It was assumed that the major losses due to bonding, connectors, and RF board are experienced at the RF frequencies, whereas the losses after the down-conversion were assumed negligible. Second, the inputs were then bonded and the whole front-end was measured. The *CG*, double side-band noise figure (NF_{DSB}) and input matching, expressed as S_{DD11} for LB and HB channels respectively are shown in Figs 20 and 21.

Considering the LB channel, the 3 dB bandwidth ($BW_{3\,dB}$) and NF_{DSB} of 7–8 dB was achieved for 1.5–14 GHz band, whereas the

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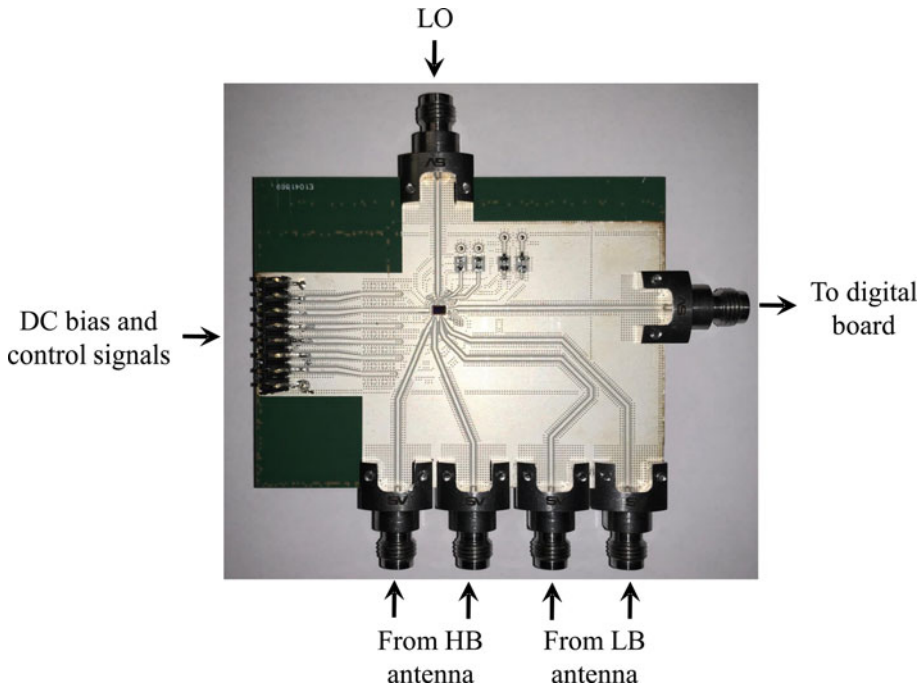


Fig. 19. Top view of the designed RF front-end.

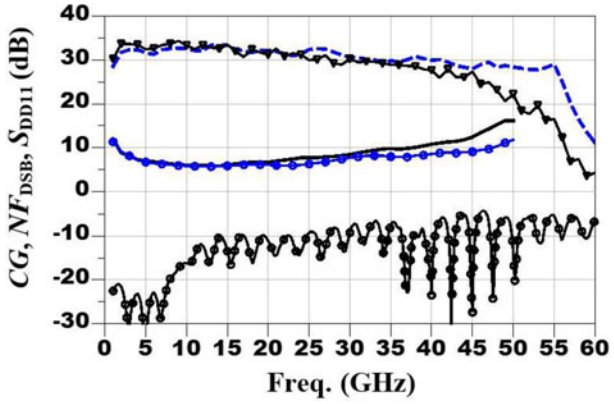


Fig. 20. HB, measured *CG*: IC input (dashed, blue), RF board input (triangles), and NF_{DSB} IC input (circles, blue), RF board input (solid). IF freq. = 100 MHz, LO power = −10 dBm, feedback off. Measured S_{DD11}, RF board input (circles).

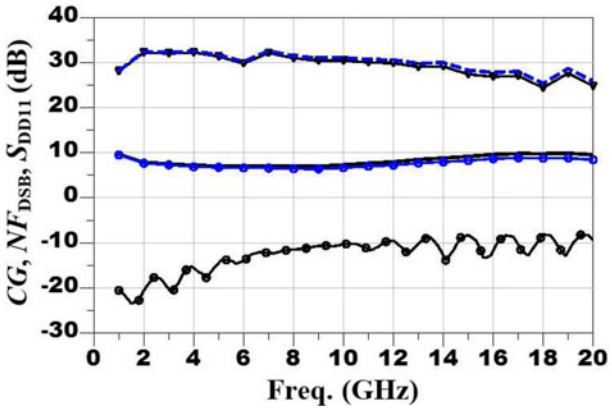


Fig. 21. LB, measured *CG*: IC input (dashed, blue), RF board input (triangles), and NF_{DSB}: IC input (circles, blue), RF board input (solid). IF freq. = 100 MHz, LO power = −10 dBm, feedback off. Measured S_{DD11}, RF board input (circles).

parasitic impact due to bond wires, RF board, and V-connectors is nearly negligible. The limitation toward higher frequencies here was caused by the active power limiter, which employs the 300–330 nm gate length HV-FET devices with oscillation frequencies below 18 GHz. An input matching better than −8 dB with the RF board is achieved. On the HB side, a flat *CG* response was measured from 1.5 up to 55 GHz when probing the IC input, however when measured over the RF board, a notable performance degradation due to input mismatch caused by the bond wires, substrate, and connector parasitic effects is seen above 45 GHz. These results can be traced back by means of simulations. Since the targeted HB frequency range is 10–40 GHz, these results perfectly satisfy the requirements, however for applications requiring broader frequency response, a flip chip option, and Rogers 4003 substrate should be alternatively considered. The achieved NF_{DSB} in the 10–40 GHz band was 6–8.5 dB and 6–12 dB when measuring over the IC and RF board inputs respectively. An input matching better than −7.5 dB with the RF board is achieved. No explicit low frequency filtering was employed for the HB channel, since it is inherently done by the antenna and the off-chip (tunable/adaptive) filters. All the following results will be referred to the bonded input case. The gain compression measurements were performed with a 50Ω load termination with the variable gain LNA first set to its high gain mode (feedback off) and then to the linear mode (full feedback on). The measured results for the LB and HB channels are shown in Figs 22 and 23 respectively.For the LB channel, the input referred 1 dB compression point was measured at P_{IN} = −39 and −28 dBm for high gain mode and linear mode respectively. Comparably, for the HB case, $P_{IN,\,1\,dB}$ was reached at P_{IN} = −38 dBm and P_{IN} =−23 dBm respectively. This proves the potential of controlling the gain of an LNA by switching the feedback, since over 10 dBm more input power can be handled. The *CG* sensitivity to the LO drive level was accounted for in the design phase by adding the dedicated LB and HB LO driver amplifiers at the outputs of the RF switch. These were designed to deliver

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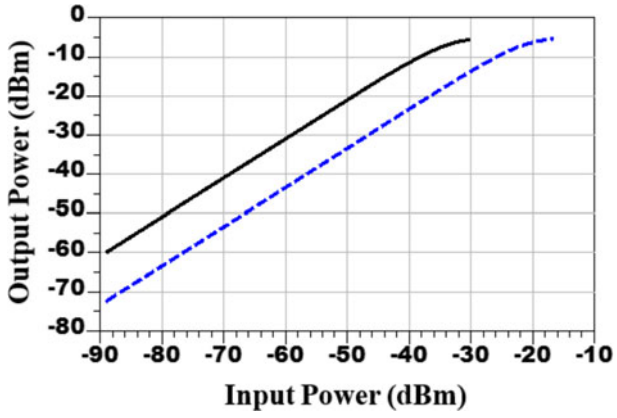


Fig. 22. LB, measured P_{OUT} versus P_{IN}: high gain mode (solid), linear mode (dashed, blue). RF freq. = 8 GHz, IF freq. = 100 MHz, LO power = −10 dBm.

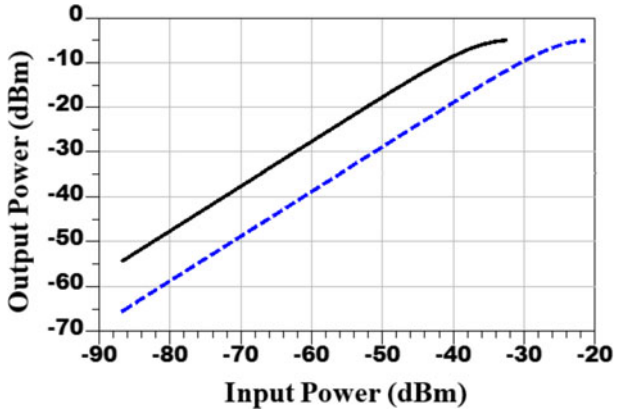


Fig. 23. HB, measured P_{OUT} versus P_{IN}: high gain mode (solid), linear mode (dashed, blue). RF freq. = 25 GHz, IF freq. = 100 MHz, LO power = −10 dBm.

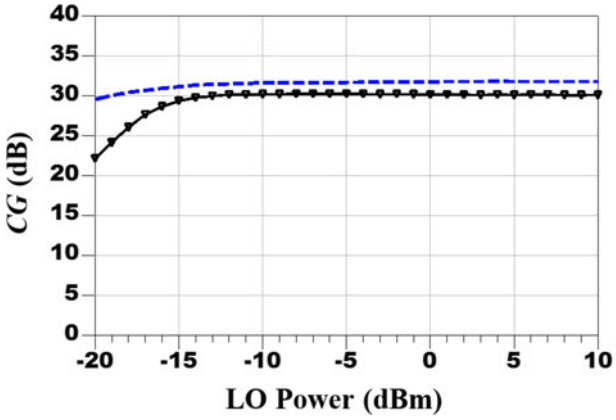


Fig. 24. Measured *CG* versus supplied LO input power level. LB (dashed, blue) RF freq. = 8 GHz, IF freq. = 100 MHz, HB (triangles) RF freq. = 25 GHz, IF freq. = 100 MHz.

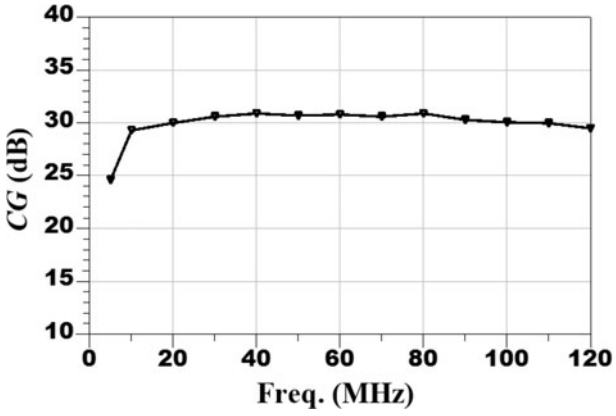


Fig. 25. LB, measured *CG* versus IF frequency. RF freq. = 8.05 GHz 8.12 GHz, LO freq. = 8 GHz, LO power = −10 dBm.

Table 1. SotA comparable RX front-ends.

Technology	$BW_{3\,dB}$ (GHz)	NF_{DSB} (dB)	*CG* (dB)	$P_{OUT,\,1\,dB}$ (dBm)	P_{DC} (mW)	Area (mm^2)	Ref.
130 nm SiGe BiCMOS	10–40	n/a	17–20	−1[a]	390	1.32	[5]
130 nm SiGe BiCMOS	8–18	7.8	33–53	−10	180	1.81	[6]
250 nm SiGe BiCMOS	30–40	n/a	18	0	207	n/a	[20]
250 nm SiGe BiCMOS	26–43	7	20	−10[a]	n/a	2.5	[21]
130 nm SiGe BiCMOS	1.5–54	9	18–30	−9	302/352	3.08	IC
130 nm SiGe BiCMOS	1.5–40	10.7	18–30	−9	302/352	n/a	IC + Board

n/a stand for not provided, or not applicable.
[a]Denotes a calculated value.

14 dB gain, ensuring the Gilbert cell mixers are provided with sufficient LO drive level. The *CG* versus LO input signal level is presented in Fig. 24. A flat *CG* response is yielded above LO input power level of −13 dBm. Note that in the HB channel the LO driver signal is commuted to the frequency doubler, hence when reducing the LO power below the threshold of approximately −15 dBm, the *CG* response falls with twice the steepness. The *CG* versus the IF frequency response was assessed in the 5–120 MHz frequency range. The corresponding results are demonstrated in Fig. 25. The employed IF amplifier ensures flat *CG* response for the required 10–100 MHz IF frequency band, whereas below 10 MHz a drop in *CG* due to off-chip capacitors is observed. The *LB* and *HB* inputs were stressed with 25 and 20 dBm input power levels and no change in performance could be observed. The total DC power consumption is 302 mW when the LB channel is active and 352 mW for the active HB channel case.

For the benchmarking purpose, a comparison of the designed RX front-end with the SotA is presented in Table 1.

The designed front-end IC strongly outperforms the SotA in terms of achieved 3 dB bandwidth. Although some of the reported

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RX ICs show slightly better NF or DC power consumption, none of the reported wideband RX IC designs give any data about input power ruggedness. This parameter was one of the key performance trade-offs in terms of noise matching, bandwidth, and DC power consumption.

Conclusion

An ultra-wideband, highly robust 1.5–40 GHz FMCW radar RX front-end was designed. Consisting of multiple innovative components that initially have been separately designed, fabricated, and tested, the RX front-end demonstrates an outstanding performance in terms of achievable bandwidth, NF, linearity, and high input power ruggedness. Furthermore, the separately tested front-end IC demonstrates a capability of reaching a large bandwidth of 1.5–55 GHz. To the best knowledge of the authors, there has been no comparable RX front-end reported yet that would fully cover S to Ka bands and compete in terms of differential, compact design, input power ruggedness, linearity, and NF.

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