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Nonideality sources and implementation considerations in polar transmitters

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In this paper, the main nonidealities appearing in polar transmitters will be addressed, together with several implementation considerations. Special attention will be paid to the role of AM modulation nonlinearity and parasitic AM-to-PM conversion, once architecture mechanisms such as time-delay mismatch between branches or limited bandwidth in the amplitude path are controlled. The device limiting factors for a highly efficient switched mode operation and a linear amplitude modulation will be identified. Some circuit design and implementation guidelines for the RF modulating stage and the envelope amplifier will be discussed, to finish with system-level analysis considerations under two-tone and real communication signal excitations.

Keywords: Efficiency, Linearity, Nonlinear distortion, Polar transmitters, Power amplifiers, Wireless systems

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I. INTRODUCTION

Emerging wireless transmitter architectures have recently been receiving a lot of attention from both industry and academics. In comparison to the still more common *I/Q* or Cartesian transmitter, Tx, architecture, a polar topology can achieve a much better trade-off between nonlinear distortion and supply power efficiency. Derived from the envelope elimination and restoration (EER) or Kahn [1] concept, a polar Tx circumvents the compromise representing the complex envelope using amplitude and phase signals, $a_x(t)$ and $\phi_x(t)$, respectively, which are then treated independently until the last Tx stage, the RF PA. The power amplifiers (PA) is in fact a switching device, typically operating in a highly efficient class D^{-1}, E, F, or F^{-1} mode, whose excitation signal is a constant envelope $\phi_x(t)$ modulated carrier, while $a_x(t)$ is finally restored dynamically modulating the PA's supply voltage, $v_{DD}(t)$. In Fig. 1, a system-level model of such architecture is presented.

Unfortunately, as in the case of any other engineering solution, this architecture does not follow an ideal distortion-free operation, presenting a series of nonlinear impairment mechanisms at device, circuit, and system levels.

In [2], Raab treated the finite AM modulator bandwidth in an approximate way, assuming an ideal brick-wall reconstruction filter, while the differential delay between the AM and PM paths was studied considering this delay as fixed and independent of the base-band envelope frequency. Later, the finite bandwidth analysis was extended by Milosevic *et al.* in [3], where a general reconstruction filter was considered.

In [4], Wang *et al.* experimentally investigated the distortion caused by $v_{DD}(t)$-to-$a_y(t)$ nonidealities, $v_{DD}(t)$-to-$\phi_y(t)$ conversion, and differential delay. There, they recognized that $v_{DD}(t)$-to-$a_y(t)$ presented a certain degree of nonlinearity, as the tested class E PA presented carrier feedthrough, i.e., the pressed $a_y(t)$ levels off to a non-null value when $v_{DD}(t)$ goes to zero.

In the present paper, the impact of the main nonidealities appearing in a polar transmitter will be addressed. Special attention will be paid to the identification of the limiting factors of device operation as an RF switch, AM modulated through the supply voltage. Circuit design guidelines and implementation considerations will also be presented, with emphasis on the modulating stage and the envelope amplifier (EA). An analytical model of the nonlinear distortion in a polar transmitter will be included, together with system-level simulation results for the clasical two-tone linearity test or under real telecommunication signals. The results to be presented were obtained from the joint work of several European institutions inside the TARGET Network of Excellence. In particular, such results were derived from Task D activities inside Work Package 2.3.2 WiSELPAs.

II. IDENTIFICATION OF TRANSISTOR LIMITING FACTORS FOR HIGHLY EFFICIENT RF SWITCHING

In polar transmitters, a switched mode power amplifier, handling a phase-modulated carrier, is usually modulated in amplitude by means of the drain supply voltage. A highly efficient and linear operation along the whole modulating range is then desired for properly overcoming the limitations of *I/Q* transmitting architectures.

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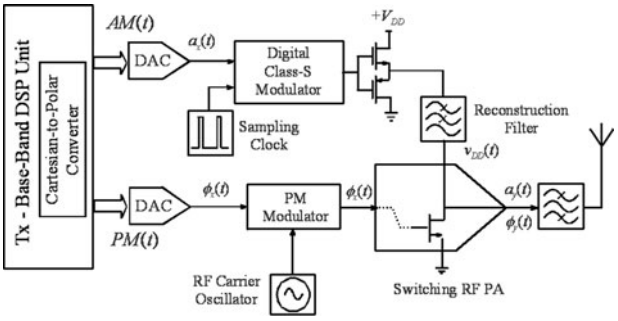


Fig. 1. System model of a wireless Tx with polar architecture.

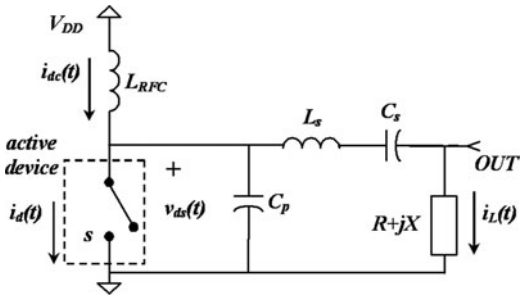


Fig. 3. Circuit schematic of a class E PA.

A) Switching models

In switched mode PAs, the devices are used as high-speed switches rather than controlled current sources as in traditional power amplifiers. To first order, the devices may therefore be modeled by either of the simplified switch models shown in Fig. 2.

In general, most devices are best described by the model in Fig. 2(b), where the output capacitance is in parallel to the switch (i.e., the intrinsic channel region) and the series inductance is an extrinsic parasitic mainly present due to the device package. Both models also include a finite on-resistance, R_{on}. In switched mode PAs, the switch is periodically closed and opened with the RF input signal as a stimulus. For model (b) in Fig. 2, any voltage, V_c, present over the switch when it closes will result in wasted energy in the switch resistance according to

$$P_{C,\mathrm{Loss}} = \tfrac{1}{2} C V_c^2 f. \tag{1}$$

To maximize the efficiency and enable high-frequency operation, it is therefore crucial to make sure that V_c is zero when the switch closes. By a careful design of the transistor load network, zero voltage switching (ZVS) can be obtained.

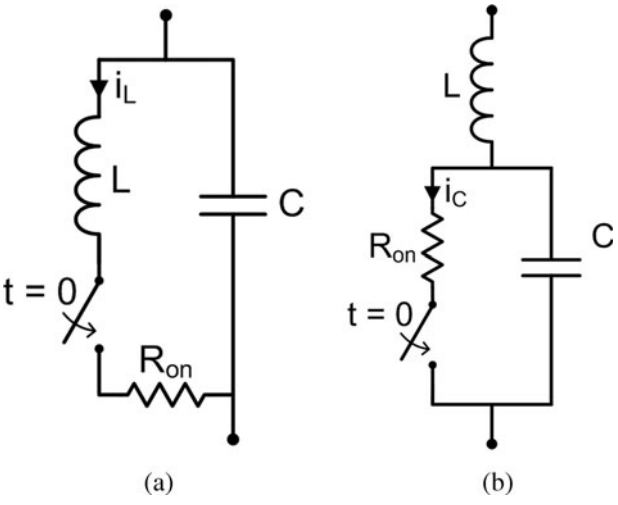


Fig. 2. Idealized switch models: (a) series inductance loss model and (b) parallel capacitance loss model.

A number of classes of switched mode power amplifiers have been derived, including classes E, D, E/F, and F.

B) Device limitations in class E PAs

Since one of the most popular and effective switching mode PA configurations is the class E amplifier, its operation and intrinsic limitations will be focused on in the following. The basic circuit configuration of a class E PA is depicted in Fig. 3, where the active device is represented by a switch and the capacitor C_p includes both device output parasitic reactance and circuit stray capacitances, and may be eventually increased by an external capacitor (if required).

Once the capacitor value, C_p, is determined from optimum circuit conditions [5], the maximum operating frequency can be obtained as in (2).

$$f_{\max} = 0.0177 \frac{I_{\max}}{V_{DD} C_p}. \tag{2}$$

Besides, if a nonzero ON resistance for the switch is considered, R_{on}, the stage efficiency becomes [6]

$$\eta = \frac{1 + \left((\pi/2) + \omega C_p R_{on}\right)^2}{(1 + (\pi^2/4))\left(1 + \pi\omega C_p R_{on}\right)^2}. \tag{3}$$

C) Device technology comparison

Following (3), it seems clear that to maximize the efficiency in class E PA, the $R_{on} \times C_p$ product should be minimized. Taking into account that the maximum frequency where class E operation is possible, $f_{\max}$, occurs when C_p is completely absorbed by device parasitic output capacitance (C_{ds} in FET families), and that the $R_{on} \times C_{ds}$ product is mainly determined by the device technology, different results would be expected if the PA is designed using LDMOS, SiC MESFETs, or GaN HEMTs.

The device parameters given per millimeter gate width are summarized in Table 1. Apparently, GaN technology is shown to be superior for realization of high-performance switched mode PAs. This is also verified in recent publications, where class E and F GaN HEMT PAs having peak PAE values of 85% are demonstrated [7, 8].

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Table 1. Device technology comparison for switched mode operation

Technology	C_{ds} [pF/mm]	R_{on} [Ω × mm]	$R_{on} \times C_{ds}$ [pF × Ω]
LDMOS	0.6	20	12
SiC	0.3	15	4.5
GaN	0.5	2.0	1.0

III. IDENTIFICATION OF TRANSISTOR LIMITING FACTORS FOR LINEAR AM MODULATION

In analogy to the AM–AM and AM–PM conversion characteristics of linear amplifiers, the amplitude and phase nonlinearities of drain-modulated switched mode PAs are quantified through the V_{dd}-to-AM and V_{dd}-to-PM curves.

A) V_{dd}/*AM* and V_{dd}/*PM* characterization

The V_{dd}/*AM* and V_{dd}/*PM* profiles are usually measured using a continuous wave RF excitation at the desired input power level and sweeping the drain to source biasing voltage. Strong deviations, as carrier feedthrough or AM saturation, may be easily identified; however, the existence of mild nonlinearities may not be that evident.

To improve the accuracy of such characterization, a procedure for experimentally extracting the coefficients of their Taylor series expansions, as appearing in (4) and (5), has been developed.

$$AM(V_{dd}) = AM_0 + m_1 v_{dd} + m_2 v_{dd}^2 + m_3 v_{dd}^3 + \cdots \quad (4)$$

$$PM(V_{dd}) = PM_0 + p_1 v_{dd} + p_2 v_{dd}^2 + p_3 v_{dd}^3 + \cdots \quad (5)$$

A low-level and low-frequency AM modulating tone was added to the DC voltage and inserted by the drain biasing path. The switching PA output was captured, using a vector signal analyzer, and the harmonic content of the amplitude and phase components of the complex envelope (obtained through FFT) used for extracting the *m's* and *p's*. In Fig. 4, as a way of illustration, the evolutions of m_1 and p_1 are presented for the Tx line class E PA in [9].

Different nonlinearities are evident from the measured profiles. Besides the expected RF carrier leakage and amplitude saturation, further nonlinearity was found. At medium drain-to-source voltages, V_{DD} around 2.5 V, the information provided by the derivatives allowed detecting a slight curvature in the V_{dd}-to-AM characteristic, a nonlinearity associated in this case to the existence of a kink effect in the employed PHEMT device.

B) Modeling V_{dd}/*AM* and V_{dd}/*PM* nonlinearities

Assuming the active device switches between a state of maximum voltage (v_{OMAX}) with minimum (ideally null) current, located in cut-off, and another one, located in the triode zone of FETs, where the current is maximum (i_{OMAX}) and the voltage reaches its minimum (v_{Omin}), the device current may be approximated by a semi-sinusoidal arc and the output voltage by a square wave (the case of a class F PA).

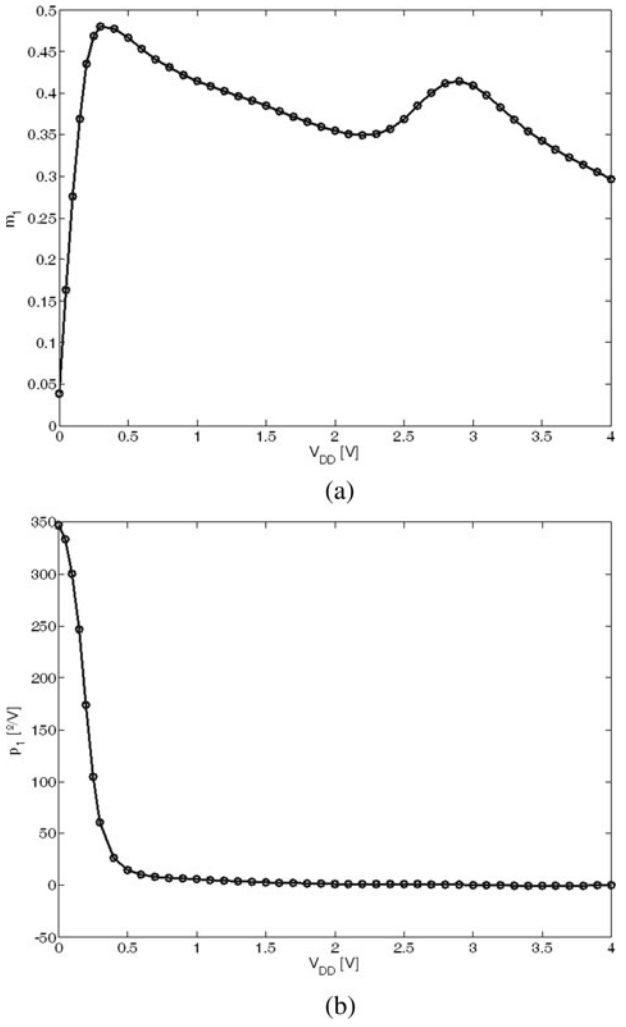


Fig. 4. Evolution of (a) m_1 and (b) p_1 for a PHEMT-based Tx line class E PA.

As was demonstrated in [10], the device fundamental output current will be the sum of a channel and a gate-to-drain current component:

$$I_o(\omega) = \frac{v_{DD}}{2R_{ON} + R_L}\left[1 + j\omega\frac{4}{\pi}R_L C_{gd}\right] - j\omega C_{gd} V_i(\omega). \quad (6)$$

This simplified model shows that, for high v_{DD} values, i.e., when the resistive channel current dominates, the output fundamental component amplitude will be proportional to v_{DD}, while its phase will be close to zero (or to any other constant offset). When v_{DD} tends to zero, the capacitive current dominates over the channel current and the PA shows an evident feedthrough. There, the output amplitude tends to a constant (i.e., independent of $v_{DD}(t)$), while the phase tends to -90°. Using a simple nonlinear model for C_{gd} and a polynomial for the resistive part of $a_y(v_{DD})$, see [10] for details, a good reproduction of the V_{dd}/*AM* and V_{dd}/*PM* characteristics for the above-introduced Tx line class E PA was obtained, as depicted in Fig. 5.

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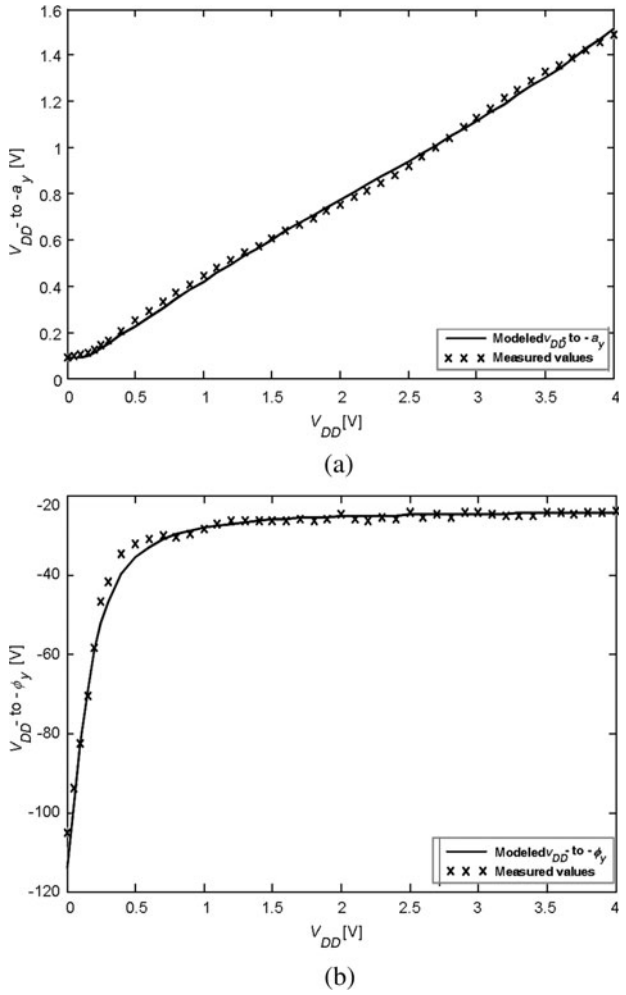


Fig. 5. Measured and modeled (a) v_{DD}(t)-to-a_y(t) and (b) $v_{DD}(t)$-to-$\phi_y(t)$ characteristics of the PHEMT-based class E PA circuit.

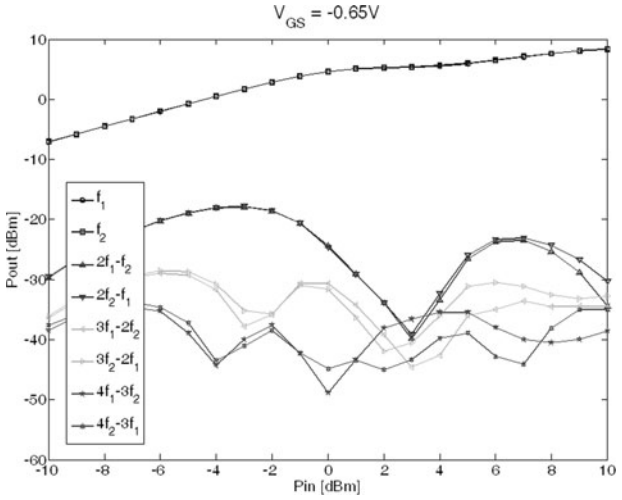


Fig. 6. Modulating stage linearity evolution with the RF power level.

IV. CIRCUIT DESIGN GUIDELINES

A) Optimum operating conditions in the RF PA

For a certain gate-to-source biasing voltage, using too much input drive could exacerbate the feedthrough nonlinearity at low output levels (low values in the amplitude signal). However, using too little RF excitation could take the device out of the switched mode of operation at high values of the modulating component, resulting in increased nonlinearity at high output levels.

Thus, an optimum operating region could be expected, observed around 3.5 dBm for the already modeled PA – see Fig. 6. The desired tones do not vary with the RF drive and the intermodulation distortion components are minimized.

B) Design of a high-efficiency modulator

Included in the system level diagram of Fig. 1, an EA is needed to provide the supply modulating voltage. Since the total efficiency of a polar amplifier is given by $\mathrm{PAE_{TOT}} = \mathrm{PAE}_{PA} \times \eta_{EA}$, it is therefore extremely critical to also maximize the EA efficiency (η_{EA}).

As a result from the nonlinear Cartesian-to-polar transformation, the new signal components $a_x(t)$ and $\phi_x(t)$ no longer have the same properties as the original I/Q data. Most importantly, the AM envelope and RF input signals are much more wideband than the original signal.

Taking a closer look at the envelope signal, it can be seen that most of its energy is concentrated at low frequencies. As a way of example, Fig. 7 shows the fractional energy content evolution versus bandwidth for the envelope of a 5 MHz WCDMA signal. Indeed, 95% of the signal energy is concentrated below a 100 kHz bandwidth.

The two types of EA topologies most commonly considered in polar transmitter applications are class S modulator based, and switch mode-assisted linear amplifiers, whose simplified schematics are depicted in Fig. 8. Both have evolved from high-power/high-efficiency audio applications [11, 12].

In a class S modulator, a pulse train is generated whose low-pass filtered content corresponds to the desired signal envelope. The pulse train is amplified via a totem-pole arrangement of two transistors. The basic configuration uses complementary transistors, but since the modulator sampling clock needs to be much higher than the bandwidth of the envelope in order to maintain high signal fidelity, this tends to degrade the efficiency at wide bandwidths. This arrangement has been used for realization of EAs in low-power

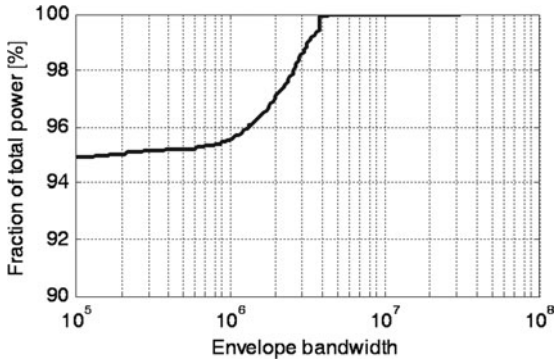


Fig. 7. Fractional energy content versus bandwidth for the envelope of a 5 MHz WCDMA signal.

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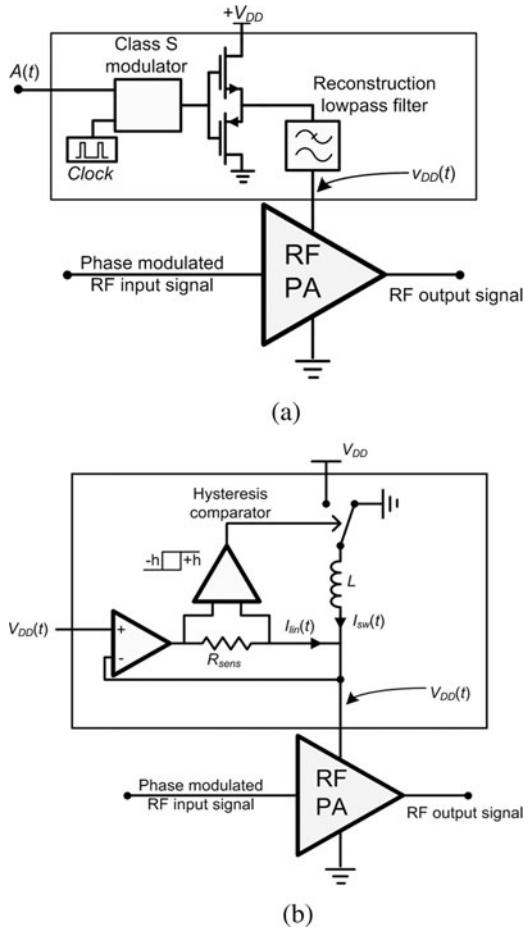


Fig. 8. (a) Class S and (b) switch mode-assisted linear amplifiers.

handset applications [13], but has not yet been demonstrated in high-power applications.

In the case of the switch mode-assisted linear amplifier, represented in Fig. 8(b), the topology consists of a linear stage (represented by an operational amplifier) in parallel with a switching stage.

The switching stage is controlled so as to minimize the current from the linear one. The current through the linear stage is sensed via a resistor and a hysteresis comparator. The switching block will thereby toggle state whenever the current through the linear stage exceeds the hysteresis threshold. The time constant determining the switching speed is controlled by the sense resistor, the inductance, the load resistor, and hysteresis.

The linearity of the EA is maintained by introducing a feedback from the output node to the negative input of the linear stage. The switching noise is thereby automatically canceled in the output signal, which is an important advantage compared with the class S modulator concept.

A switch mode-assisted linear EA prototype has been designed at the Chalmers University of Technology, following the topology in Fig. 8. In Fig. 9, a picture of its implementation is included.

Simulations have verified the switch mode-assisted linear amplifier concept for EAs in polar transmitters.

There are a number of design parameters to be considered and to be optimized to maximize its performance. In general,

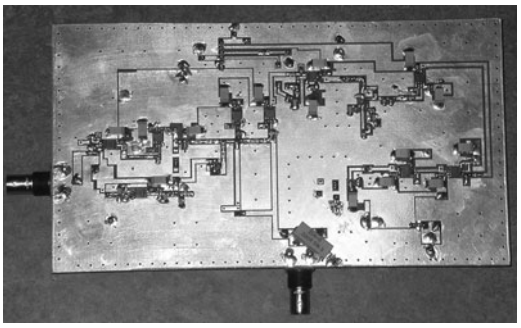


Fig. 9. EA PCB layout with switching, linear, and current sensing stages included.

in order to significantly improve the EA efficiency beyond the 55% obtained from simulations, it is necessary to increase the switching frequency. In this way, contributions from the less efficient linear stage can be minimized. However, this requires fast switching devices and a fast feedback loop with wide bandwidth.

V. SYSTEM-LEVEL CONSIDERATIONS IN POLAR TRANSMITTERS

A) Analytical model of the nonlinear distortion

The model considered herein was developed in [9, 10], based on the system level description of the transmitter shown in Fig. 1. The model includes the distortion caused by the $a_x(t)$ bandwidth limitations, differential delay, $v_{DD}(t)$-to-$a_y(t)$, and $v_{DD}(t)$-to-$\phi_y(t)$ nonlinearities. An ideal behavior of the baseband circuitry and PM modulator was assumed. Figure 10 reports measured and simulated results of the fundamental, third-, and fifth-order IMD, obtained for varying the differential delay between paths, τ, also including the complete nonlinear model briefly discussed in section III.B. It helps us understand the relative influence of the $v_{DD}(t)$-to-$a_y(t)$ and

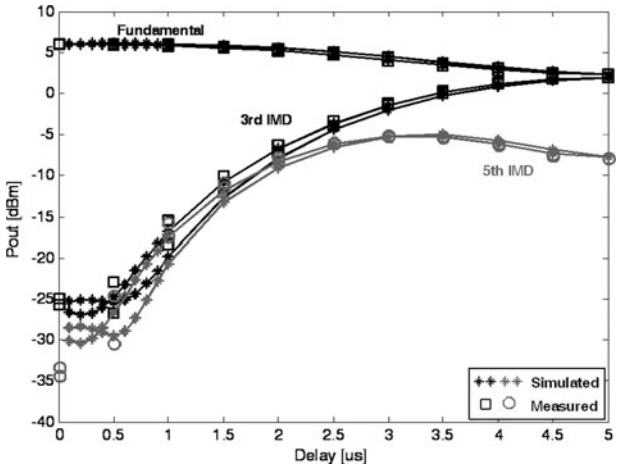


Fig. 10. Measured and simulated fundamental, third-, and fifth-order IMD, when τ was varied from 0 up to 5 μs $[2\pi/(4\omega_m)]$, including both the $v_{DD}(t)$-to-$a_y(t)$ and $v_{DD}(t)$-to-$\phi_y(t)$ nonlinearities.

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$v_{DD}(t)$-to-$\phi_y(t)$ nonlinearities when considering the modulating stage as part of the polar transmitting architecture.

As can be appreciated from Fig. 10, and according to the explanation given by the authors in [10], not only the distortion floor, but also the asymmetry, may be predicted when the model employed in the simulations also includes the phase nonlinearity.

Attention was then turned to the effects of the low-pass reconstruction filter, $F(\omega)$. For that, a 3 dB ripple third-order Chebyshev approximation was supposed. Figure 11 illustrates the corresponding responses predicted by the complete nonlinear model.

The agreement between measured, simulated, and analytically predicted results is very good, which fully validates the model proposed in [10].

B) Polar transmitter simulation results under real telecommunication signals

The results presented in the above section were extended to the use of different real telecommunication signals as WCDMA, EDGE, and OFDM, all derived from ADS2005A. The main system-level nonidealities described by Raab [2] and previously studied for a two-tone excitation were considered:

(1) delay mismatch between amplitude and phase paths;
(2) filter in the envelope path for bandwidth limitation; and
(3) combination of both the delay and filter effects.

To quantify the results the error vector magnitude (EVM) and the adjacent channel power ratio (ACPR) figures were used. The *DC*/*DC* converter in the envelope path was modeled as a low pass filter due to the required filter for harmonic suppression.

As a way of illustration, Fig. 12 shows simulation results under WCDMA when both the filter and delay effects were included into the envelope path.

The graphs show ACPR and EVM results versus delay for different filter cut-off frequencies. The ACPR graph shows that increasing the delay and decreasing the filter bandwidth increases the out-of-band distortion as predicted before. The top ACPR curve has a cut-off frequency of 0.1 MHz and therefore experiences a large amount of distortion due to the filter cut-off frequency being far less than the bandwidth of the signal (3.84 MHz).

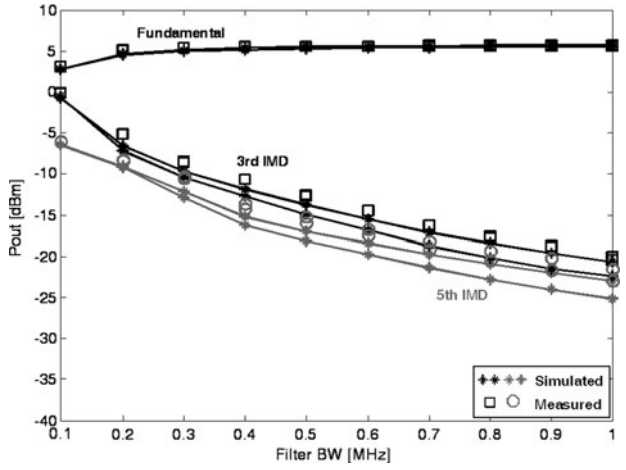


Fig. 11. Measured and simulated fundamental, third-, and fifth-order IMD, when the pass-band edge frequency of the reconstruction filter was varied from $\Omega = \omega_o/\omega_m = 2$ up to 20, including both the $v_{DD}(t)$-to-$a_y(t)$ and $v_{DD}(t)$-to-$\phi_y(t)$ nonlinearities.

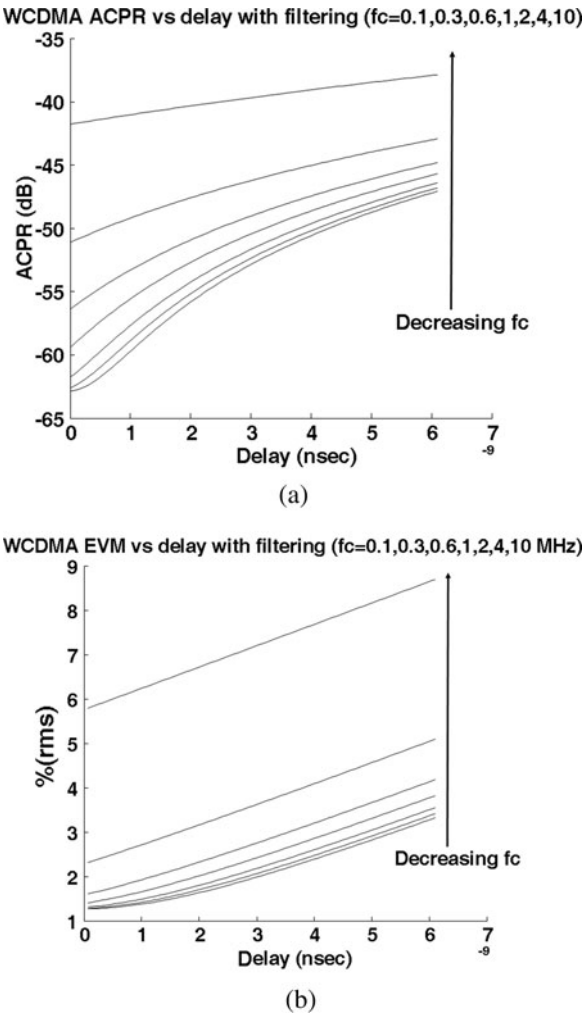


Fig. 12. Plot of (a) ACPR and (b) EVMs versus delay and cut-off frequency for WCDMA.

Analyzing the impact of delay and bandwidth over different communication standards, strict requirements have been obtained for achieving the desired ACPR. The results for the case of delay are summarized in Table 2.

To fit the linearity requirements of modern standards, strict control over the architecture nonidealities is required. However, the remaining nonlinear distortion sources, associated to the modulating stage (including also the EA), demand the use of correcting or predistorting functions. Several research lines in this sense have been recently opened with the participation of the groups involved in this work [14–16].

Table 2. Impact of differential delay

	WCDMA	EDGE	OFDM
ACRP	50 dB	40 dB	40 dB
DELAY	4 nsec	30 nsec	1.5 nsec
EVM	2.2%	4.2%	3.5%

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VI. CONCLUSION

In this paper, a dedicated study of polar transmitters, as emerging and promising wireless transmitter architecture, has been presented. In theory, this technique may help overcome the current limit on achievable linearity and efficiency figures. Device, circuit, and system-level aspects have been extensively treated. Based on an accurate characterization and identification of the limiting factors of transistor operation as a RF switch, AM modulated through the supply voltage, some guidelines have been offered for selecting the optimum operating conditions of the modulating stage. Special attention has also been focused on the impact and critical design of the EA. The system-level nonidealities have been finally evaluated with both two-tone closed-form expressions and real telecommunication signal simulations.

These results were obtained as part of the work developed inside Task D of TARGET Work Package 2.3.2 WiSELPAs, a WP initially aimed to envisage future perspectives of collaboration research beyond TARGET NoE.

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