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Analysis of continuous mode class-B/J efficiency model for broadband rectifier

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Research Paper

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Abstract

This paper presents a broadband rectifier based on GaN high electron mobility transistor (HEMT). The continuous class-B/J rectifier operation mode is analyzed in detail. The relationship between the continuous mode class-B/J rectification efficiency and the output capacitance C_{out} and the on-state resistance Ron is built and the rectification model is firstly presented. Then, the available impedance design space can be determined based on the rectification efficiency model. Considering the package parameters of the CGH40010F, design space at the package plane has been presented. Moreover, a broadband phase tuning network (PTN) is adjusted to satisfy this impedance space. Thus, a broadband transistor-based rectifier can be designed using the continuous class-B/J mode and the PTN. For validation, a rectifier working in 2.4–3.3 GHz was fabricated using CGH40010F. The rectification efficiency varies from 66% to 78% when RF input power is 10 W. Compared with other transistor-based rectifiers, the presented rectifier has a competitive working bandwidth.

Introduction

Wireless power transfer (WPT) is the technology of delivering energy to electrical loads through electric fields, magnetic fields and electromagnetic waves [1, 2]. As an emerging technology, WPT has been widely applied in emerging scenarios such as solar power stations, electric vehicle charging, and drone power supply. This also necessitates rectifiers with higher power handling capabilities. The rectifier plays an important role in the whole system and is essential for the development of WPT.

Diodes and transistors are two essential rectifier devices. The former is not capable of supporting high-power wireless energy transmission [3–6]. The Schottky diode rectifier in reference [7] utilizes power distribution technology to improve its power processing capability. But the maximum power is still limited to 29 dBm. The transistor-based rectifier can effectively enhance power handling capability. According to the time-reversal duality principle proposed by Hamill, RF rectifiers designed by reversing the power flow of power amplifiers will maintain high efficiency while coping with high-power capacity scenarios [8]. The GaN HEMT rectifier has significantly improved the high-power handling capability. A bias voltage for the transistor is needed, but the gate itself consumes no power. However, most rectifiers based on GaN HEMT still aim for high RF-DC conversion efficiency in a narrow band, which significantly restricts their applications [9–11]. Therefore, it is necessary to design rectifiers to achieve broadband energy conversion. In [12], the necessity of a 180° phase difference is demonstrated. Hence, a broadband phase shifter is applied in the rectifier to expand the rectifier bandwidth [13]. However, the previous works only focus on the broadband phase shift network [12, 13] and the broadband rectification efficiency model has not presented. In particular, the operation mode will affect the bandwidth and efficiency. The continuous mode class-B/J power amplifier (PA) proposed by Cripps further extends the impedance region, making it more suitable for broadband design [14]. The class-F/F-1PA has been applied to design rectifiers in previous works [10, 13, 15]. Based on the time reversal duality principle, it is possible to expand the bandwidth of rectifiers by reversing continuous mode class-B/J PA. The continuous class-B/J operation mode in the rectifiers needs to be investigated due to a different loss mechanism compared to PAs.

This letter aims to extend the continuous mode class-B/J theory to the design of broadband rectifiers. The rectification efficiency model for a broadband rectifier has been presented for the first time. Based on the selected rectification efficiency, we establish the continuous mode class-B/J design space. In addition, the phase tuning network (PTN) is designed considering input and output matching networks. This paper further investigates the impact of port impedance variations on phase-shifting values. After accounting for package parameters, the impedance is converted from the current generator plane to the package plane. Finally, the designed rectifier exhibits high RF-DC conversion efficiency at the 10 W input power level over a wide frequency band.

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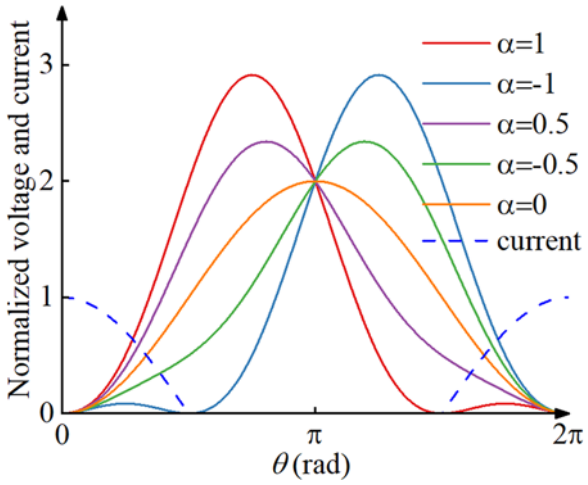


Figure 1. Continuous mode class-B/J current and voltage waveforms.

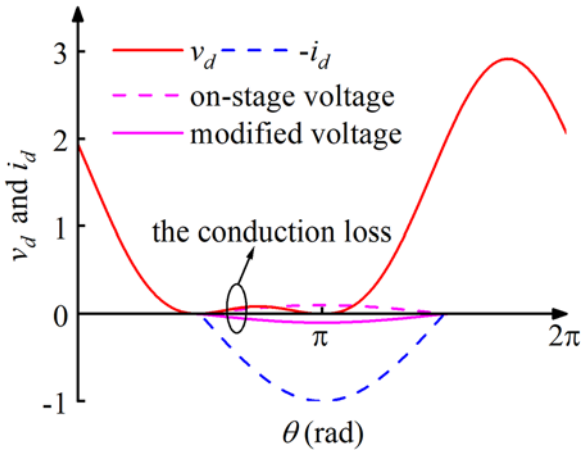


Figure 2. Current and voltage waveforms in class-B/J rectifier ($\alpha = 1$).

Analysis of the proposed rectifier

The continuous mode class-B/J PA has a flexible design space, which tends to expand bandwidth. Based on the time-reversal duality principle, the power flow of the switching device can be reversed. The PA's output receives the input power, and after RF-DC conversion, the DC signal is delivered from the drain terminal.

Theory of continuous class-B/J mode

The class-J operation mode applies a phase shift to the fundamental and second harmonic components in class-B operation mode, while maintaining the class-B output power and efficiency [16]. The continuous class-B/J mode introduces a variable factor to the class-B voltage waveform. The drain voltage and current waveforms in the continuous class-B/J mode are given by Equations (1) and (2):

$$v_d = V_{\max}(1-\cos\theta)(1-\alpha\sin\theta) \tag{1}$$

$$i_d = \begin{cases} I_{\max}\cos\theta, 0 \le \theta \le \frac{\pi}{2} \& \frac{3\pi}{2} \le \theta \le 2\pi \\ 0, \frac{\pi}{2} \le \theta \le \frac{3\pi}{2} \end{cases} \tag{2}$$

where $V_{\max}$ represents the maximum voltage of the device and $I_{\max}$ is the peak amplitude of the current flowing through the device. The variation of α creates a continuous design space for the fundamental and second harmonic components at the device terminals. Figure 1 shows the voltage and current waveforms of continuous class-B/J mode as α varies from −1 to 1 in 0.5 steps.

The expression for the fundamental and second harmonic impedance of the continuous class-B/J operation mode at the current generator plane is given by [17]

$$Z_{f_0} = \frac{2}{\omega C_{\text{out}}}(1+j\alpha), \tag{3}$$

$$Z_{2f_0} = -j\frac{3\pi\alpha}{4\omega C_{\text{out}}}, \tag{4}$$

where $\alpha \in [-1,1]$, C_{out} is the nonlinear output capacitance. C_{out} can be expressed as $C_{\text{out}} = C_{\text{out0}} + A[1 + \tanh(B^*V_{\text{ds}} + C)]$, where $C_{\text{out0}} = 1.95$, $A = 1192.4$, $B = -0.0594714$, and $C = -2.94696$ [18, 19].

For non-ideal switches, similar to PA, the conduction loss of the rectifier is evident in the voltage waveform [15]. The time-reversed voltage and current of the class-B/J rectifier are shown in Fig. 2. In the rectifier, the half sinusoidal pulse generated by the conduction resistance (the magenta dashed line) is modified to a negative half sinusoidal pulse (the magenta solid line) because the rectifier cannot generate negative power. The conduction loss caused by the on-state resistance Ron in continuous mode class-B/J rectifier is

$$P_{R_{\text{on}}} = \frac{1}{2\pi}\int_0^{2\pi} R_{\text{on}} i_d^2 d\theta = R_{\text{on}}\left(\frac{I_{\max}}{2}\right)^2. \tag{5}$$

The capacitive switching losses need to be taken into account due to the output capacitance C_{out} in the switching devices. The output capacitance C_{out} is charged to $V_{\max}$ and then discharged to 0 V before the switch turns on, as determined by the drain current and voltage waveforms. Therefore, the capacitive switching loss of the rectifier can be expressed as

$$P_{\text{cap}} = \frac{1}{2}C_{\text{out}}V_{\max}^2\frac{\omega}{2\pi}. \tag{6}$$

The dc terms in the Fourier series of the drain voltage v_{d} and current i_{d} mentioned in (1) and (2) can be obtained as

$$V_{\text{dc}} = V_{\max} - R_{\text{on}}\frac{I_{\max}}{\pi}, \tag{7}$$

$$i_{\text{dc}} = \frac{I_{\max}}{\pi}. \tag{8}$$

Furthermore, the dc output power of the rectifier is

$$P_{\text{dc}} = (V_{\max} - R_{\text{on}}\frac{I_{\max}}{\pi})\frac{I_{\max}}{\pi}, \tag{9}$$

Compared to the power loss mechanism of PA, rectifiers have no overlapping losses [15]. Therefore, in the rectifier, the total power is the sum of the power delivered to the load and the power consumed. The rectification efficiency should be

$$\eta = \frac{P_{\text{dc}}}{P_{\text{dc}} + P_{\text{on}} + P_{\text{cap}}} = \frac{1}{1 + \frac{R_{\text{on}}\left(\frac{I_{\max}}{2}\right)^2}{(V_{\max} - R_{\text{on}}\frac{I_{\max}}{\pi})\frac{I_{\max}}{\pi}} + \frac{\frac{1}{2}C_{\text{out}}V_{\max}^2\frac{\omega}{2\pi}}{(V_{\max} - R_{\text{on}}\frac{I_{\max}}{\pi})\frac{I_{\max}}{\pi}}}, \tag{10}$$

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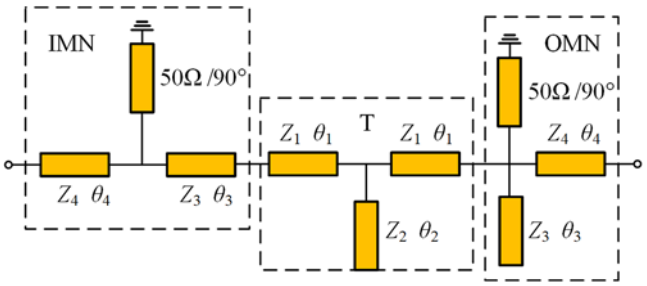


Figure 3. Phase tuning network.

C_{out} is negatively correlated with V_{ds} [19]. The capacitive switching loss of the device increases with the increase of C_{out}. A larger R_{on} will reduce the rectification efficiency. In this paper, we assume the transistor operates in the saturation region with a drain voltage of 28 V and drain current of 1.5A.

Analysis of phase tuning network

For the self-synchronous rectifier, the gate of the transistor requires an RF input signal from the drain with a 180° phase difference. An external phase shifter will degrade the rectification efficiency due to impedance mismatch at the connection. Therefore, a broadband phase shift network should be designed for the rectifier. Figure 3 shows the PTN of the rectifier, which consists of the input matching network (IMN) and output matching network (OMN) of the PA.

As shown in Fig. 3, the ABCD parameters of the T-type structure IMN and OMN can be expressed as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_T = \begin{bmatrix} \cos 2\theta_1 + \frac{Z_1}{2Z_2}\sin 2\theta_1 \tan\theta_2 & jZ_1 \sin 2\theta_1 + \frac{jZ_1{}^2 \sin^2\theta_1 \tan\theta_2}{Z_2} \\ \frac{j\sin 2\theta_1}{Z_1} - \frac{j\cos^2\theta_1 \tan\theta_2}{Z_2} & \cos 2\theta_1 + \frac{Z_1}{2Z_2}\sin 2\theta_1 \tan\theta_2 \end{bmatrix} \tag{11.a}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{IMN} = \cos\theta_3 \cos\theta_4 * \begin{bmatrix} 1 - \frac{Z_4 \tan\theta_3 \tan\theta_4}{Z_3} & jZ_3 \tan\theta_3 + jZ_3 \tan\theta_4 \\ \frac{j\tan\theta_4}{Z_4} + \frac{j\tan\theta_3}{Z_3} & 1 - \frac{Z_3 \tan\theta_3 \tan\theta_4}{Z_4} \end{bmatrix} \tag{11.b}$$

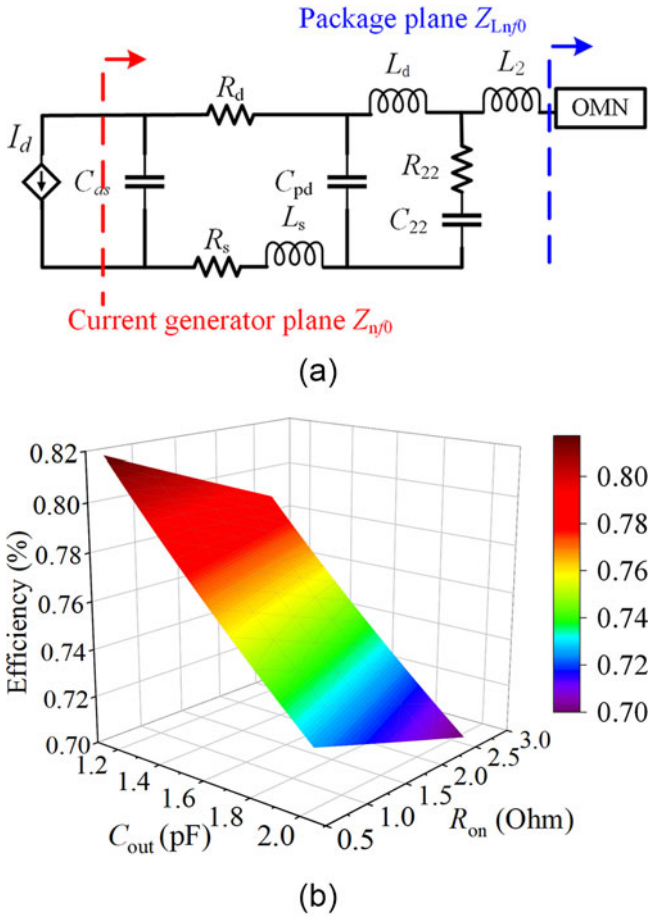


Figure 4. The external package parameters of the transistor and the rectification efficiency model. (a) Equivalent output circuit of CGH40010F. (b) Rectification efficiency at 2.85 GHz versus C_{out} and R_{on}.

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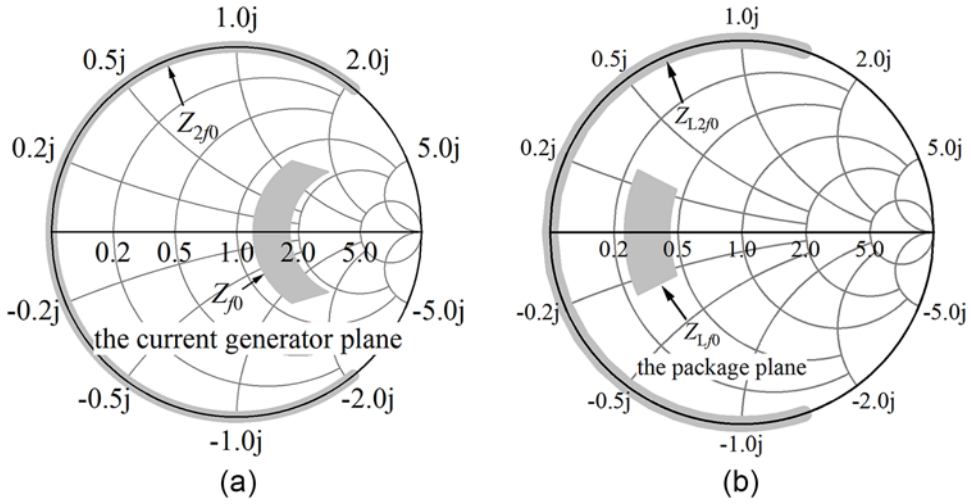


Figure 5. Design space of continuous mode class-B/J rectifier with $\eta > 70\%$. (a) At the current generator plane. (b) At the package plane.

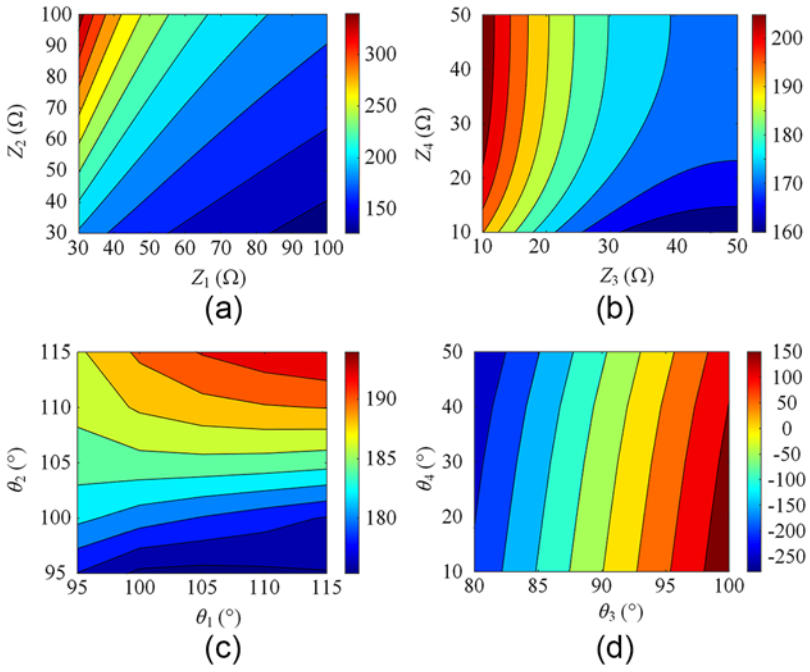


Figure 6. Relationship between phase value and design parameters. (a) Z_1 and Z_2. (b) Z_3 and Z_4. (c) θ_1 and θ_2. (d) θ_3 and θ_4.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\mathrm{OMN}} = \begin{bmatrix} \cos\theta_4 & jZ_4\sin\theta_4 \\ \frac{-jZ_3\cos\theta_4}{\tan\theta_3} + \frac{j\sin\theta_4}{Z_4} & \cos\theta_4 + \frac{Z_3Z_4\sin\theta_4}{\tan\theta_3} \end{bmatrix} \quad (11.c)$$

Further, the phase of PTN is a summation of the input, T-type and output networks. The ABCD parameters of the PTN can be inferred as [20, 21]

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\mathrm{PTN}} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\mathrm{IMN}} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\mathrm{T}} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\mathrm{OMN}}. \quad (12)$$

For the phase response, the formula of insertion phase for the PTN can be derived as

$$\phi_{\mathrm{PTN}} = -\arctan\left(\frac{B + CZ_0^2}{j(A+D)Z_0}\right)_{\mathrm{PTN}}. \quad (13)$$

The 180° phase difference between the drain and gate of the transistor needs to be satisfied in the operating frequency band, which can be expressed as

$$\Delta\phi = \phi_{\mathrm{IMN}} + \phi_{\mathrm{T}} + \phi_{\mathrm{OMN}} - \theta_{\mathrm{m}} = \pi, \quad (14)$$

where θ_{m} is the electrical length of 50 Ω reference line. In order to ensure a constant phase over a wide frequency band, the phase slope should satisfy

$$\frac{d\phi_{\mathrm{IMN}}}{df} + \frac{d\phi_{\mathrm{T}}}{df} + \frac{d\phi_{\mathrm{OMN}}}{df} - \frac{\theta_{\mathrm{m}}}{f_0} = 0. \quad (15)$$

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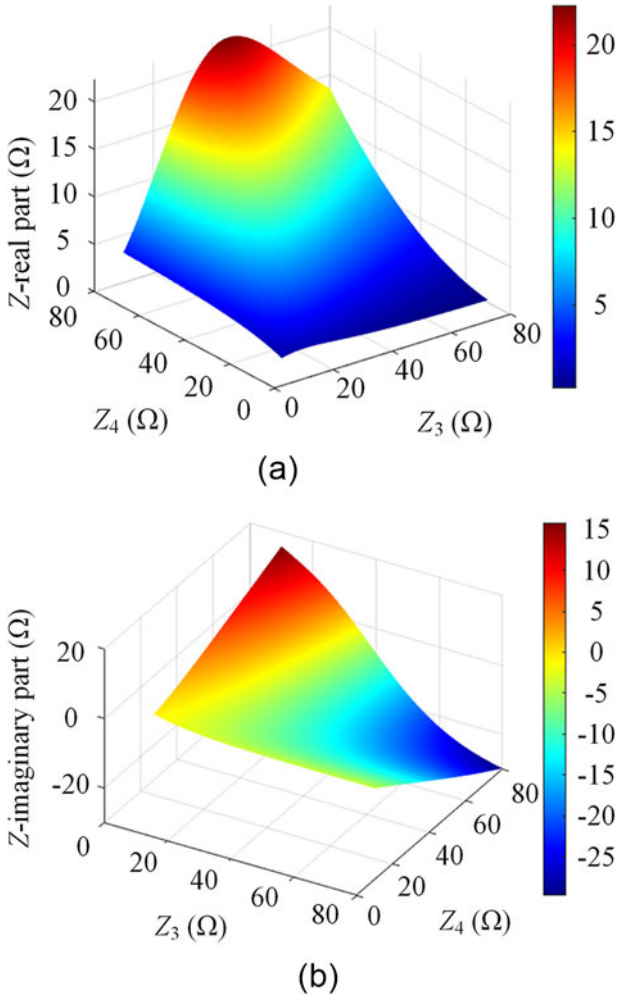


Figure 7. The terminal impedance of the OMN. (a) Real part. (b) Imaginary part.

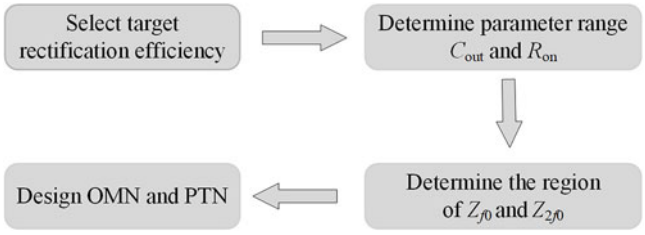


Figure 8. The design flow diagram.

The 2.4–3.3 GHz band is strategically significant for wireless systems, such as such as Wi-Fi and wireless power supply for civilian radar. In the following, the 2.4–3.3 GHz broadband rectifier is selected as an example to validate the effectiveness of this efficiency model. This design employs the CGH40010F transistor. The electrical equivalent circuit of the transistor is illustrated in Fig. 4(a). From the efficiency model as established in Equation (10), the output capacitance and on-resistance can be inferred. Figure 4(b) shows the relationship between the rectifier efficiency and the transistor parameters at 2.85 GHz. For $\eta > 70\%$, C_{out} varies between 1.18 pF and 2.05 pF, while R_{on} ranges from 0.5 Ω to 2.5 Ω. Then, using (3) and (4), the desired load impedance can be obtained

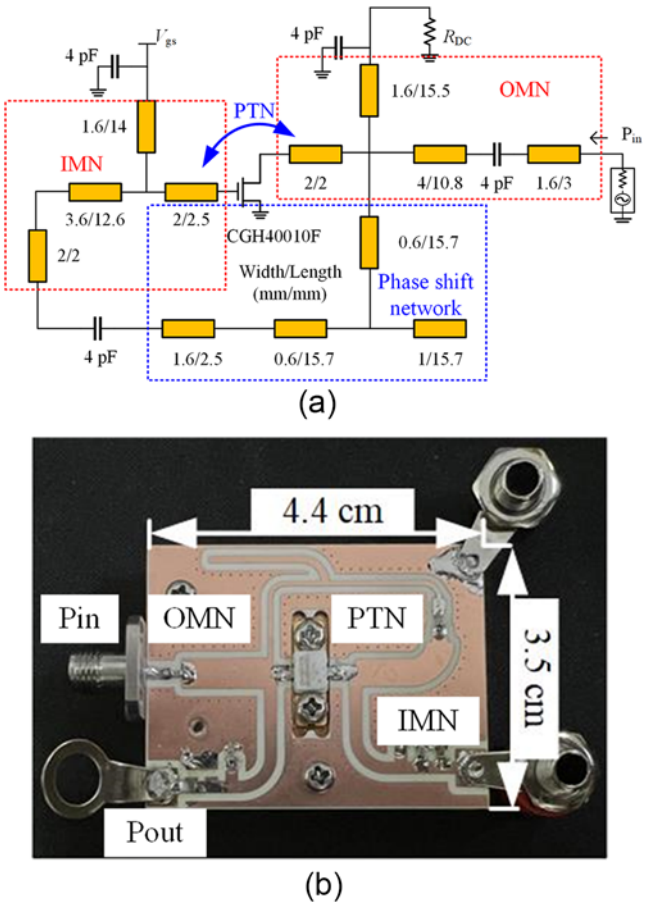


Figure 9. The designed rectifier. (a) Schematic diagram of rectifier. (b) fabricated rectifier.

based on these C_{out}. Figure 5(a) shows the corresponding design space (grey area) at the current generator plane.

It can be seen that the impedance of the package plane can be obtained by connecting the current generator plane impedance in parallel with the equivalent circuit of the transistor. The calculation formula is as follows:

$$Z_{L@nf_0} = \frac{(R_{22} + Z_{nC_{22}}) * Z_{n-b}}{(R_{22} + Z_{nC_{22}}) - Z_{n-b}} - Z_{nL_2}, \tag{16}$$

where:

$$Z_{n-b} = \frac{Z_{nC_{pd}} Z_{n-a}}{Z_{nC_{pd}} - Z_{n-a}} - Z_{nLd} \tag{17.a}$$

$$Z_{n-a} = \frac{Z_{nC_{ds}} Z_{nf0}}{Z_{nC_{ds}} - Z_{nf0}} - (R_s + R_d + Z_{nLs}) \tag{17.b}$$

$$Z_{nC_{22}} = \frac{-j}{n\omega C_{22}}, Z_{nC_{pd}} = \frac{-j}{n\omega C_{pd}}, Z_{nC_{ds}} = \frac{-j}{n\omega C_{ds}} \tag{17.c}$$

$$Z_{nL_2} = jn\omega L_s, Z_{nL_d} = jn\omega L_d, Z_{nL_s} = jn\omega L_s \tag{17.d}$$

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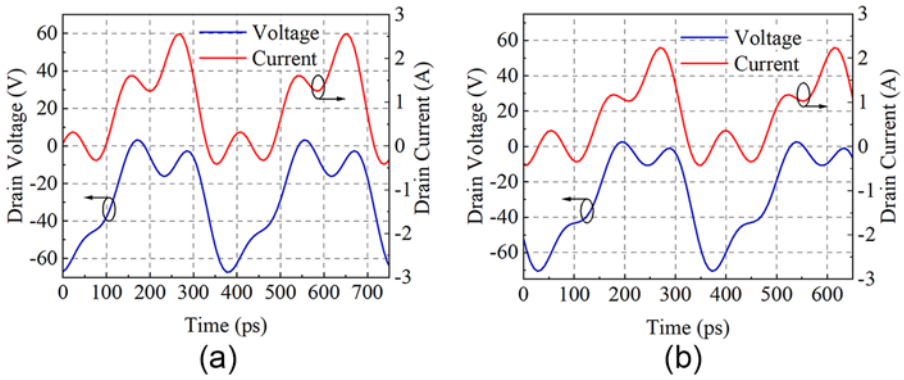


Figure 10. Drain voltage and current waveforms. (a) 2.6 GHz. (b) 2.9 GHz.

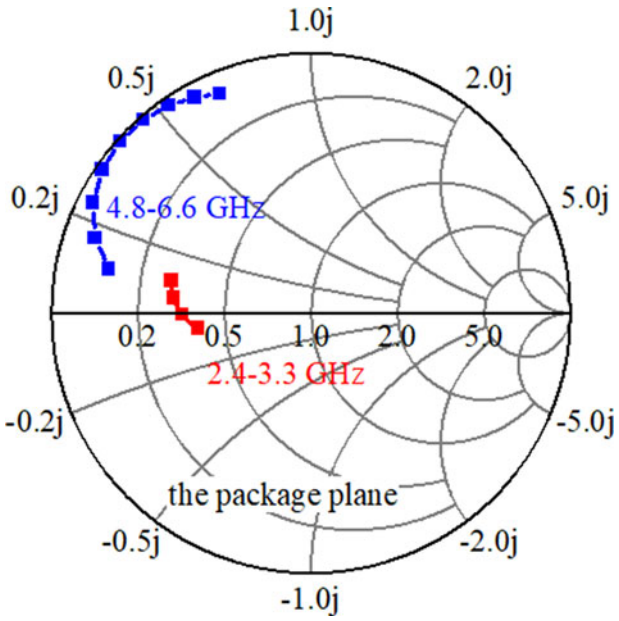


Figure 11. The impedance trajectory at the transistor package plane.

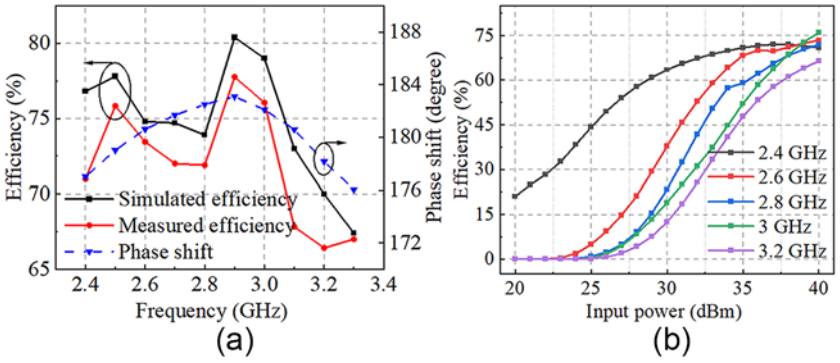


Figure 12. Performance of the designed rectifier. (a) Simulated phase shift of PTN and maximum rectification efficiency with 10 W input power. (b) Measured efficiency.

After accounting for the package parameters of the CGH40010F, the package plane design space corresponds to the grey area in Fig. 5(b). For bandwidth extension, the drain terminal impedance needs to be designed within the aforementioned space.

Based on Equations (14) and (15), the relationship between parameters and predetermined phase shift values in the PTN can be illustrated in Fig. 6. The microstrip line impedance can be determined as $30 \le Z_1 \le 50\ \Omega$, $40 \le Z_2 \le 70\ \Omega$, $18 \le Z_3 \le 30\ \Omega$ and $20 \le Z_4 \le 50\ \Omega$. The electrical length of the microstrip line can be determined as $95 \le \theta_1 \le 115°$, $95 \le \theta_2 \le 102°$, $70 \le \theta_3 \le 83°$ and $10 \le \theta_4 \le 50°$. In addition, it can be observed that the phase value is less affected by θ_1 and θ_4.

The terminal impedance of the OMN needs to be designed within the fundamental and second harmonic regions mentioned in Fig. 5(b). The OMN is analyzed based on the transmission line

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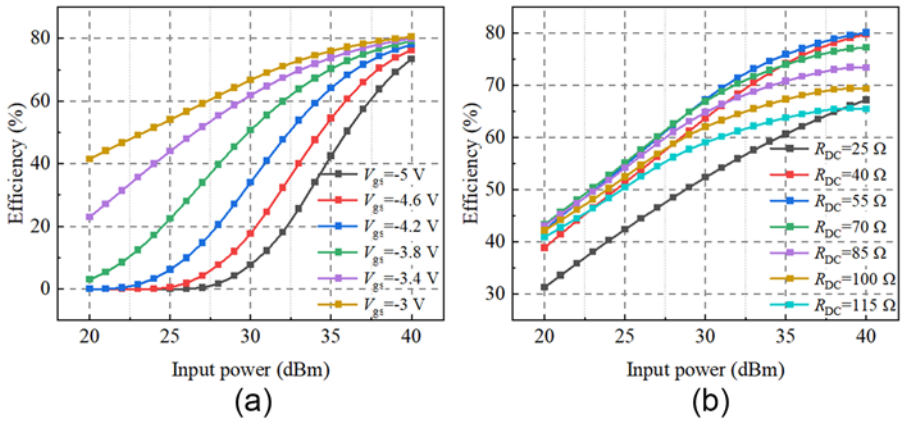


Figure 13. Measured rectification efficiency at 2.9 GHz versus (a) different V_{gs} and (b) different R_{DC}.

Table 1. Comparison with other rectifiers

Ref	Device	Frequency (GHz) /FBW (%)	Pin (W)	Efficiency (%)	Mode	CFPB	Model
[3]	S. d	1.6–2.8 /54.5	0.06	60–78			No
[4]	S. d	2.1–3.3 /44.4	0.025	70–76			No
[12]	G. H	2.65–2.95 /10.7	10	62–85		8.4	No
[13]	G. H	2–3 /40	10	70–86	F^{-1}	25	No
[15]	G. H	0.6–1.15 /62.9	8	70–80	F^{-1}	3.85	No
[22]	G.H	1.6–2.6 /47.6	10	72.1–82.4	GF^{-1}	21	No
[23]	G.H	1.8–2.8/43.4	10	60.4–88.2	C-G F^{-1}	23	No
T.W	G. H	2.4–3.3/31.6%	10	66–78	C-B/J	25.7	Yes

Notes: C-B/J = continuous mode class-B/J; CFBP = center frequency*Pin *bandwidth; S. d = Schottky diode; G. H = GaN HEMT.

impedance formula. Figure 7 shows the terminal impedance and corresponding parameters in the OMN. There is an overlapping region with the impedance requirements in the PTN, ensuring both output matching and phase shift are achieved simultaneously. Z_3 and Z_4 are required to be within the range of 20–70 Ω at the fundamental frequency region of continuous class-B/J operation mode. In addition, this design takes full account of the OMN terminal impedance in Fig. 5(b).

Design of the rectifier

To validate the design methodology, the rectifier operating at 2.4–3.3 GHz is designed with CGH40010F. It is implemented on the Rogers 4350B with a thickness of 0.762 mm. The design flow is shown in Fig. 8. A source-pull simulation was performed to obtain the input impedance for designing the IMN. Based on the required efficiency, the output capacitance C_{out} and conduction resistance R_{on} were selected from Fig. 4(b). Furthermore, the fundamental and second harmonic design spaces are obtained from Fig. 5 to design the OMN. In the actual PCB design, we need to account for the welding and layout of components such as capacitors and transistor. To address these practical requirements, we made appropriate modifications, including adding solder pads and adjusting the positions of certain components. In this design, the phase of PTN is the sum of the IMN, phase shift network and OMN. It is worth noting that the PTN port impedance varies with frequency. The PTN should be adjusted to achieve 180° phase shift values over a wide frequency band. According to the above requirements, the final simulation parameters of the rectifier were optimized. The final design schematic diagram is given in Fig. 9 with a size of 3.5 × 4.4 cm^2.

The simulated drain voltage and current waveforms at 2.6 and 2.9 GHz at the current generator plane are shown in Fig. 10. The simulated impedance traces at the package plane are plotted in Fig. 11, with the fundamental (the red line) and second harmonic (the blue line) impedance located near the theoretical continuous mode class-B/J regions. These results confirm that the designed rectifier is consistent with the continuous-mode class-B/J theory.

For the GaN rectifier, only the transistor gate needs to be supplied with initial DC bias and the gate has no power consumption. In Fig. 12(a), the designed PTN can provide a phase shift of 176°–183°. At 2.4–3.3 GHz, when the input power is 10 W, the measured saturation rectification efficiency is 66%–78%. The optimum gate voltage and load impedance at different frequency points need to be slightly adjusted. Figure 12(b) illustrates the rectification efficiency at different input powers with R_{DC} = 50 Ω and V_{gs} = −3.6 V.

The relationship between rectifier performance at 2.9 GHz and various V_{gs} and R_{DC} values is shown in Fig. 13. It can be seen that when V_{gs} = −3 V and R_{DC} = 55 Ω, the optimal rectification efficiency at 2.9 GHz can be obtained as the input power increases.

Table 1 presents the comparison results between the proposed broadband rectifier and other designs. Unlike Schottky diode-based rectifiers, the GaN HEMT transistor rectifier demonstrates greater input power capacity. In this article, the transistor operating mode is associated with the efficiency model of the rectifier, and

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the output capacitance and on resistance are divided and guided by the target rectification efficiency for design. Although its maximum saturation efficiency is slightly lower than some previously reported designs, it offers a broader impedance matching range. The proposed rectifier attains a frequency and power-weighted bandwidth (CFPB) that is either superior to or comparable to previously reported works. More importantly, the continuous-mode class-B/J efficiency model has been developed for this rectifier, providing a novel approach to broadband rectifier design.

Conclusion

In this letter, a continuous mode class-B/J efficiency model for broadband self-synchronous rectifier is presented. The rectification efficiency is analyzed as a function of the capacitance C_{out} and the on-state resistance R_{on}. Based on the rectification efficiency model, the continuous mode class-B/J design space at the package plane is derived. The PTN is designed to conform to this impedance space. The designed broadband rectifier achieves 66%–78% rectification efficiency at an input power of 10 W with a competitive operating bandwidth. Finally, the effectiveness of the continuous class-B/J operation mode in broadband rectifiers is demonstrated.

Competing interests. The authors declare none.

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