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RESEARCH PAPER

Nonlinear modeling, time-domain analysis and simulation of non-Foster elements

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In this paper, the structure of a common field-effect transistor (FET)-based negative impedance converter (NIC) that behaves as a negative capacitor is presented. The nonlinear modeling, analysis, and simulation of this non-Foster structure are presented in the time domain and the transient response of the circuit can be used to study the stability of the circuit. For the analysis of the circuit performance, the linear time-dependent modeling approach is used. This method is based on determination of the circuit parameters at each step according to parameters of the previous steps, bias voltages, and the input signal. Results of the proposed method for analysis of non-Foster circuit are compared with those of nonlinear analysis using commercial software, which shows a good agreement together and the proposed method is validated. Based on the analysis, the nonlinear capacitance of non-Foster circuit is extracted and based on the simple second order model of current source of FET, the analytic model of negative capacitor is extracted and improved by curve fitting. The proposed model results have a good agreement with simulation results of NIC's circuit.

Keywords: Non-Foster elements, Negative impedance converter (NIC), Nonlinear model of negative capacitor, Nonlinear time domain analysis

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I. INTRODUCTION

According to Foster theory, reactance of passive and lossless single-port network increases with frequency and this was first proved by Foster in 1924 [1]. If the reactance or susceptance of an element decreases with frequency, this circuit represents non-Foster element and behaves as negative capacitor or inductor. The concept of non-Foster circuit is not new at all. It is based on the concept of negative impedance converter (NIC) that was proposed in the 1950s by Linvill [2].

Non-Foster circuits are widely used to improve the performance and bandwidth of various circuits. The applications include matching of electrically small antenna [3], active dispersion-less metamaterial [4], increasing the tuning range of a varactor diode by using a negative capacitance [5] and enhancement of gain of distributed amplifiers with negative capacitance [6]. The stability of non-Foster circuits has been mentioned as the greatest practical problem [7]. These circuits are based on positive feedback structure and this may cause system instability due to the change of operating point or other parameters of circuits. For this reason, modeling and analysis of non-Foster circuits and their stability have a great importance. Investigation of non-Foster circuits' stability is generally performed on the basis of small-signal and linear model that may not be appropriate in all cases [7–11].

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Modeling and nonlinear analysis of circuit in the time domain are used for achieving transient response of the circuit that investigates the stability and the actual behavior of the circuit while other analysis approaches like harmonic balance (HB) are only used to analyze the steady state response of circuit, which for the instability condition the response never tends to it. In this paper, modeling and analysis of nonlinear non-Foster elements in the time domain are investigated and the results are compared and evaluated with the commercial software, which shows a good compatibility.

II. NON-FOSTER STRUCTURE

The structure of a NIC used to create the negative capacitance, is shown in Fig. 1 [5].

By considering the linear and small-signal model of transistors, the equivalent circuit of NIC circuit is obtained as shown in Fig. 2. The equivalent negative capacitance (C_n) based on the heart of the transistor (g_m), ignoring the effects of the parasitic elements (r_o and C_{gs}) is expressed as [5]:

$$C_n = -g_m^2 L, \tag{1}$$

In literatures and recent papers [7–11], analysis of non-Foster circuits and their stability are generally based on linear model, while with increasing the signal level and time-varying operating point, the linear model is invalid and the stability analysis may be void, hence the necessity of nonlinear analysis of non-Foster circuits and their stability based on time domain transient behavior of the circuit, are felt. These are argued in the rest of the paper.

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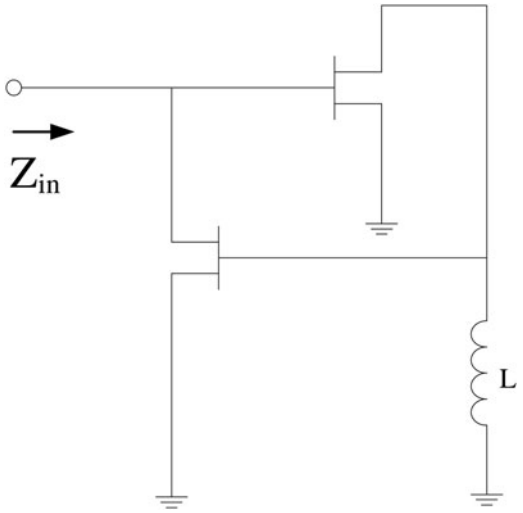


Fig. 1. The structure of NIC creating a negative capacitance.

III. NONLINEAR MODELING OF NON-FOSTER CIRCUITS

The first step in analysis of a structure, is modeling of its elements. Here, the introduced negative capacitance converter includes two field-effect transistors (FETs) and one inductance (L). The famous nonlinear models such as Curtice2, Curtice3, Statz, TOM, Tajima, Advanced Curtice Model, etc. are used to model the performance of FETs based on the various parameters. In this paper, based on Curtice2 model and considering the heart of transistor i.e. nonlinear current source, the behavior of the circuit will be discussed. In the Curtice2 model, the nonlinear current source (I_{ds}) is described according to voltages of the transistor (2), knowing that if the V_{gs} is smaller than V_{To} then the current source is zero [12].

$$I_{ds}(V_{gs}, V_{ds}) = \beta(V_{gs} - V_{To})^2(1 + \lambda V_{ds})\tanh(\alpha V_{ds}). \quad (2)$$

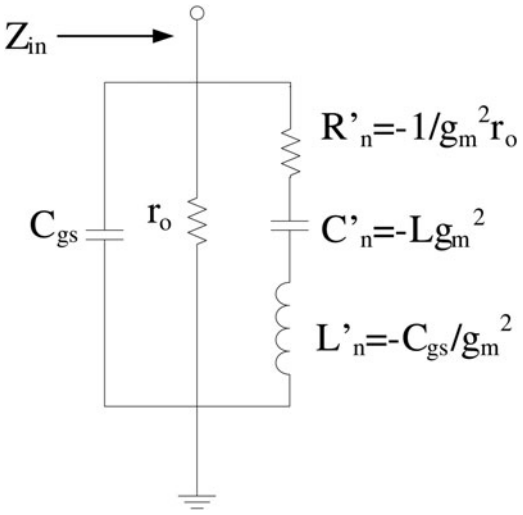


Fig. 2. Equivalent impedance of the negative capacitor converter.

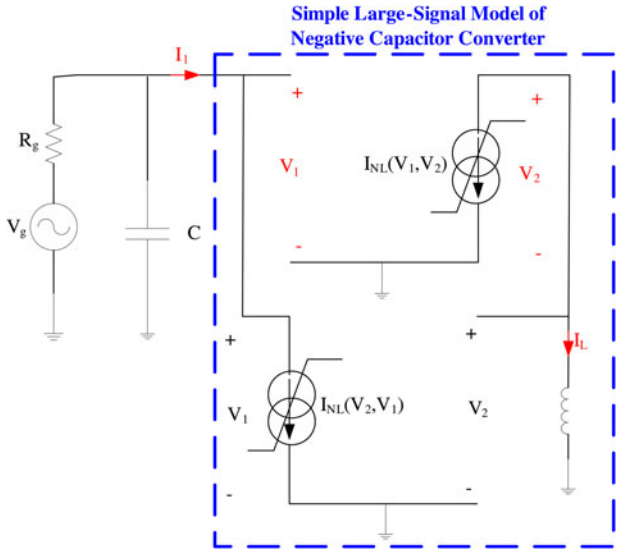


Fig. 3. Large-signal model of NIC with placing the capacitor C to stabilize performance of circuit.

Mutual conductance (g_m) and output conductance (g_{ds}) are obtained in the following expressions [12].

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = I_{ds}\left(\frac{2}{V_{gs} - V_{To}}\right), \quad (3)$$

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} = \beta(V_{gs} - V_{To})^2\ \lambda\tanh(\alpha V_{ds}) + \beta(V_{gs} - V_{To})^2\ (1 + \lambda V_{ds})\left(\frac{\alpha}{\cosh^2(\alpha V_{ds})}\right). \quad (4)$$

In these equations α, β, and λ are fixed parameters of the model and V_{To} is the pinch-off voltage of transistor. The term $(V_{gs} - V_{To})^2$ describes I_{ds} with respect to V_{gs} as a quadratic polynomial and this is why this model is called Curtice2 [12].

The large-signal model of the NIC, as shown in Fig. 3, is obtained based on simple large-signal model of FETs. Other parasitic elements such as capacitors are ignored. The time-domain analysis is used to analyze the nonlinear performance of NIC.

The capacitor C is added in the input of NIC, to prevent instability of circuit. The time constant of equivalent resistor–capacitor (RC) circuit is calculated as:

$$\tau = R(C + C_n). \quad (5)$$

The positive value of the time constant and the total capacitor of circuit is the necessary condition of stability of circuit.

To analyze the circuit based on Fig. 3, the state variables including the inductor current (I_L) and the capacitor voltage (V_1) are achieved based on the circuit relations (6–8).

$$V_2 = L\frac{dI_L}{dt}, \quad (6)$$

$$I_L = -I_{NL}(V_1, V_2), \quad (7)$$

$$C\frac{dV_1}{dt} + \frac{V_1 - V_g}{R_g} + I_{NL}(V_2, V_1) = 0. \quad (8)$$

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By considering these relations and analyzing the circuit, the behavior of NIC is modeled as a negative nonlinear capacitor that is determined according to the voltage applied to it.

IV. NONLINEAR ANALYSIS OF NEGATIVE CAPACITANCE CONVERTER IN THE TIME DOMAIN

In this section we focus on nonlinear analysis of NIC in time domain based on the obtained relations and nonlinear model of FETs. The behavior of negative capacitance and stability of circuit would be examined from the transient response.

In the time-domain analysis, based on the relations of circuits and dividing the total analysis time to Δt steps, according to the maximum existing frequency, the parameters of circuit (V_1, V_2, I_1, and I_L) are obtained in each step from parameters of current and previous steps. In the proposed method, it is assumed that the differences of parameters in each step are small. The parameters in the current step are achieved from their previous values that are mentioned in the relations (9–13).

$$t(i) = (i-1)\Delta t, \tag{9}$$

$$V_1^i = V_1^{i-1} + \Delta v_1, \tag{10}$$

$$V_2^i = V_2^{i-1} + \Delta v_2, \tag{11}$$

$$I_1^i = I_1^{i-1} + \Delta i_1, \tag{12}$$

$$I_L^i = I_L^{i-1} + \Delta i_L. \tag{13}$$

Nonlinear current source values i.e. I_{NL1} and I_{NL2} are obtained at every step from the applied voltages V_1 and V_2 and bias voltages V_{GS} and V_{DS} from (14, 15).

$$\begin{aligned} I_{NL1}^i &= I_{NL}(V_{GS} + V_2^i, V_{DS} + V_1^i) \\ &= I_{NL}(V_{GS} + V_2^{i-1} + \Delta v_2, V_{DS} + V_1^{i-1} + \Delta v_1), \end{aligned} \tag{14}$$

$$\begin{aligned} I_{NL2}^i &= I_{NL}(V_{GS} + V_1^i, V_{DS} + V_2^i) \\ &= I_{NL}(V_{GS} + V_1^{i-1} + \Delta v_1, V_{DS} + V_2^{i-1} + \Delta v_2). \end{aligned} \tag{15}$$

Assuming small variations of V_1 and V_2 (Δv_1 and Δv_2) in each step, the Taylor expansion is used to obtain the nonlinear current source relations (16, 17). G_m and G_d are time-varying parameters that are changed in each step.

$$\begin{aligned} I_{NL1}^i &= I_{NL}(V_{GS} + V_2^{i-1}, V_{DS} + V_1^{i-1}) + \frac{\partial I_{NL}}{\partial V_2}\Delta v_2 \\ &\quad + \frac{\partial I_{NL}}{\partial V_1}\Delta v_1 = I_{NL1}^{i-1} + G_{m1}^{i-1}\Delta v_2 + G_{d1}^{i-1}\Delta v_1, \end{aligned} \tag{16}$$

$$\begin{aligned} I_{NL2}^i &= I_{NL}(V_{GS} + V_1^{i-1}, V_{DS} + V_2^{i-1}) + \frac{\partial I_{NL}}{\partial V_1}\Delta v_1 \\ &\quad + \frac{\partial I_{NL}}{\partial V_2}\Delta v_2 = I_{NL2}^{i-1} + G_{m2}^{i-1}\Delta v_1 + G_{d2}^{i-1}\Delta v_2. \end{aligned} \tag{17}$$

By using linear time-varying model of current sources and the negative capacitor converter circuit equations, relations (6–8) are re-written in inter-step $(i - 1/2)$ between i, $i-1$ and the equations for the time-domain analysis of circuit are provided (18–20). The DC bias currents are supplied by the feeding networks, which are not shown to prevent complexity of network, but their effects are seen by subtracting I_{DC} from current sources in drain nodes.

$$\begin{aligned} &V_2 = L\frac{dI_L}{dt} \\ &V_2^{i-1/2} = \frac{V_1^i + V_1^{i-1}}{2} = V_2^{i-1} + \frac{\Delta v_2}{2} = L\frac{\Delta i_L}{\Delta t}, \\ &\Delta v_2 = 2L\frac{\Delta i_L}{\Delta t} - 2V_2^{i-1} \\ &C\frac{dV_1}{dt} + \frac{V_1 - V_g}{R_g} + I_{NL}(V_2, V_1) - I_{DC} = 0, \end{aligned} \tag{18}$$

$$\begin{aligned} &C\frac{V_1^i - V_1^{i-1}}{\Delta t} + \frac{(V_1^i + V_1^{i-1}) - (V_g^i + V_g^{i-1})}{2R_g} \\ &\quad + I_{NL}^{i-1/2}(V_2, V_1) - I_{DC} = 0 \\ &\qquad C\frac{\Delta v_1}{\Delta t} + \frac{(2V_1^{i-1} + \Delta v_1) - (V_g^i + V_g^{i-1})}{2R_g} + I_{NL1}^{i-1} \\ &\qquad\quad + G_{m1}^{i-1}\Delta v_2/2 + G_{d1}^{i-1}\Delta v_1/2 - I_{DC} = 0 \\ &\qquad C\frac{\Delta v_1}{\Delta t} + \frac{(2V_1^{i-1} + \Delta v_1) - (V_g^i + V_g^{i-1})}{2R_g} + I_{NL1}^{i-1} \\ &\qquad\quad + G_{m1}^{i-1}\left(2L\frac{\Delta i_L}{\Delta t} - 2V_2^{i-1}\right)\Big/2 \\ &\qquad\quad + G_{d1}^{i-1}\Delta v_1/2 - I_{DC} = 0, \end{aligned} \tag{19}$$

$$\begin{aligned} &I_L = -I_{NL}(V_1, V_2) \\ &I_L^{i-1} + \frac{\Delta i_L}{2} + I_{NL}^{i-1/2}(V_1, V_2) - I_{DC} = 0 \\ &I_L^{i-1} + \frac{\Delta i_L}{2} + I_{NL2}^{i-1} + G_{m2}^{i-1}\Delta v_1/2 + G_{d2}^{i-1}\Delta v_2/2 - I_{DC} = 0 \\ &I_L^{i-1} + \frac{\Delta i_L}{2} + I_{NL2}^{i-1} + G_{m2}^{i-1}\Delta v_1/2 \\ &\quad + G_{d2}^{i-1}\left(2L\frac{\Delta i_L}{\Delta t} - 2V_2^{i-1}\right)/2 - I_{DC} = 0. \end{aligned} \tag{20}$$

Using these relations, Δv_1 and Δi_L at each step are achieved based on voltage, current and other time-varying parameters in the previous steps, the corresponding matrix equations are shown in (21, 22).

$$\begin{aligned} &\begin{bmatrix} \frac{C}{\Delta t} + \frac{1}{2R_g} + G_{d1}^{i-1}/2 & G_{m1}^{i-1}\frac{L}{\Delta t} \\ G_{m2}^{i-1}/2 & \frac{1}{2} + G_{d2}^{i-1}\frac{L}{\Delta t} \end{bmatrix} \begin{bmatrix} \Delta v_1 \\ \Delta i_L \end{bmatrix} \\ &= -\begin{bmatrix} \frac{2V_1^{i-1} - (V_g^i + V_g^{i-1})}{2R_g} + I_{NL1}^{i-1} - G_{m1}^{i-1}V_2^{i-1} - I_{DC} \\ I_L^{i-1} + I_{NL2}^{i-1} - G_{d2}^{i-1}V_2^{i-1} - I_{DC} \end{bmatrix}, \end{aligned} \tag{21}$$

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$$\begin{bmatrix}\Delta v_1\\ \Delta i_L\end{bmatrix} = -\begin{bmatrix}\frac{C}{\Delta t}+\frac{1}{2R_g}+G_{d1}^{i-1}/2 & G_{m1}^{i-1}\frac{L}{\Delta t}\\ G_{m2}^{i-1}/2 & \frac{1}{2}+G_{d2}^{i-1}\frac{L}{\Delta t}\end{bmatrix}^{-1} \begin{bmatrix}\frac{2V_1^{i-1}-(V_g^i+V_g^{i-1})}{2R_g}+I_{NL1}^{i-1}-G_{m1}^{i-1}V_2^{i-1}-I_{DC}\\ I_L^{i-1}+I_{NL2}^{i-1}-G_{d2}^{i-1}V_2^{i-1}-I_{DC}\end{bmatrix}. \quad (22)$$

V. ANALYSIS RESULTS IN THE TIME DOMAIN

According to the proposed method for modeling negative capacitance converter in the time domain as the linear time-varying model, in this section we analyze the behavior of a negative capacitance in the time domain and compare the results with those of commercial software. They have good agreement with each other and the proposed method is validated. Parameters of nonlinear model of FETs are shown in Table 1. In this model, the parameters of the nonlinear current source as the heart of transistor are considered and other parasitic elements are ignored [13].

In Table 2, the values of parameters of circuit such as DC bias voltages, inductor and capacitor are shown. The parameters of input signal are presented in Table 3.

The input signal (V_g) with 3 V peak voltage and other specifications as detailed in Table 3, is shown in Fig. 4.

Table 1. Parameters of curtice 2 model.

Parameter	Value
β	0.0162 A/V^2
α	1.3 V^{-1}
λ	0.001 V
V_{To}	−2.35 V
V_{bi}	0.85 V

Other parasitic elements such as capacitors are ignored.

Table 2. Negative capacitance converter circuit parameters.

Parameter	Value
V_{GS}	−1 V
V_{DS}	5 V
L	1 nH
C	8 pF
R_g	50 Ω

Table 3. Specifications of the input signal.

Parameter	Value
Kind of signal	Pulse-amplitude modulation
Carrier frequency	1 GHz
V_{peak}	3 V
t_{delay}	10 ns
t_{rise}	10 ns
t_{fall}	10 ns
Pulse width	10 ns
Period	50 ns

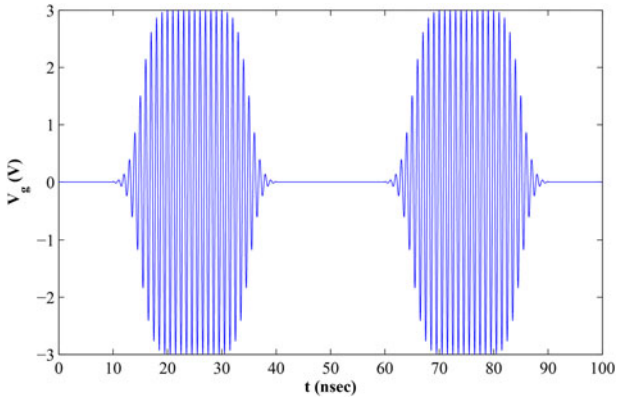


Fig. 4. The input signal, the modulated pulse with 1 GHz carrier frequency and 3 V peak voltage.

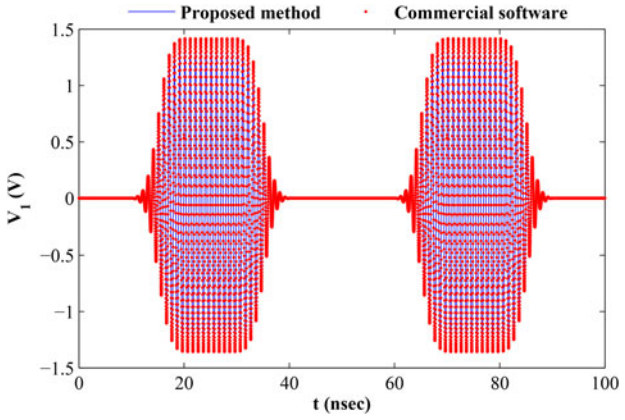


Fig. 5. The voltage at the input of negative capacitance converter (V_1) that is analyzed by the proposed method and commercial software.

The results of circuit analysis with linear time-varying model are shown in Figs 5 and 6, which are compared with the results of commercial software that have a good agreement with each other and the proposed method is validated. These results are voltage and current at the input of negative capacitance converter (V_1 and I_1), that the nonlinearity can be seen well in them, especially in I_1, due to the large amplitude of the input signal.

By validating the linear time-varying model for analysis of non-Foster capacitors, the proposed approach is used in modeling and extraction of the negative capacitor.

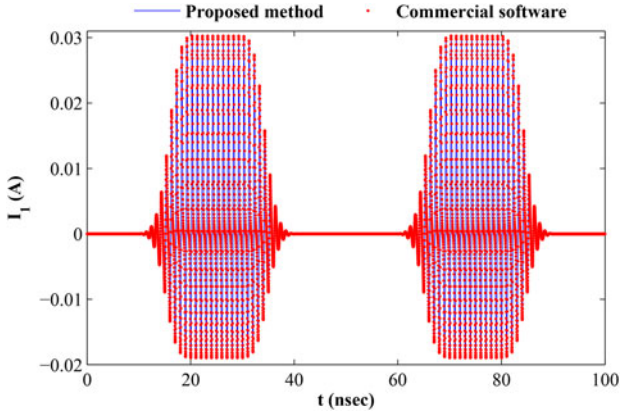


Fig. 6. The current at the input of negative capacitance converter (I_1) that is analyzed by the proposed method and commercial software.

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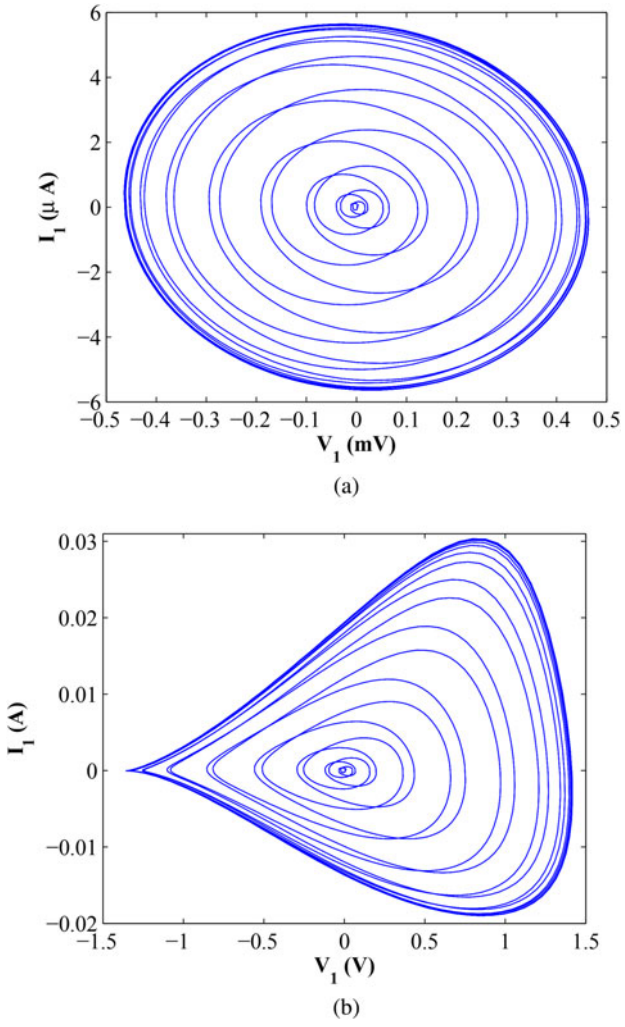


Fig. 7. Lissajous curve ($x = V_1(t)$ and $y = I_1(t)$) of the negative capacitance converter, (a) input signal with the 1 mV peak voltage, (b) input signal with the 3 V peak voltage.

Lissajous curve ($x = V_1(t)$ and $y = I_1(t)$) is shown in Fig. 7 that is obtained by eliminating the time as the independent variable. The outer rings of the curve, which were repeated several times, are the steady state response of pulses while the central parts of ring belong to the rise time and fall time of the pulse. The direction of curve as a function of time is counter-clockwise that represent the circuit function as a negative capacitance. In Fig. 7(a), the curve for the 1 mV peak voltage plotted while the peak voltage is 3 V in Fig. 7(b), and nonlinearity of circuit is well evident with increasing the signal amplitude.

VI. EXTRACTION OF NONLINEAR NEGATIVE CAPACITOR FOR STABILITY STUDY

As shown in Fig. 8, the simple second order model of current source of FETs is used in analysis of NIC. The current source (Ids) is represented by:

$$I_{ds} = g_1 v_{gs} + g_2 v_{gs}^2, \tag{23}$$

$$g_1 = \frac{2I_{ds}}{V_{gs} - V_{To}}, \tag{24}$$

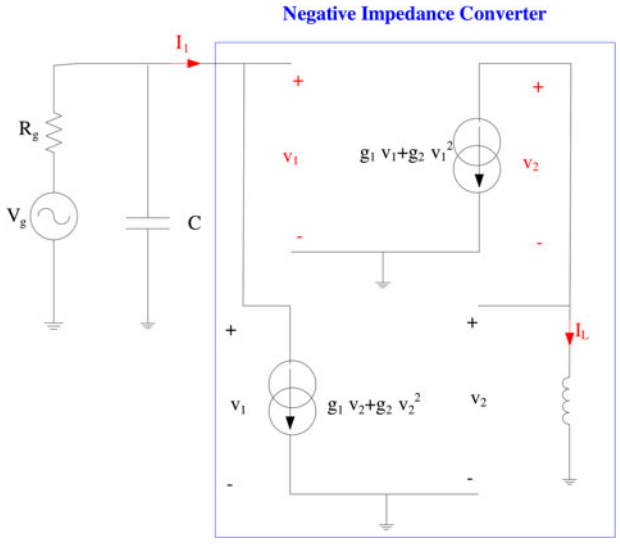


Fig. 8. Large-signal model of NIC with simple second order nonlinear model of FETs.

$$g_2 = \frac{I_{ds}}{(V_{gs} - V_{To})^2}. \tag{25}$$

By applying circuit relations, based on Kirchhoff's current law and Kirchhoff's voltage law, and considering second order representation of I_{ds}, the I_1 is obtained by (28). Assuming a capacitive behavior of NIC (28), the nonlinear model of negative capacitor is achieved as (30).

$$I_L = -(g_1 v_1 + g_2 v_1^2), \tag{26}$$

$$v_2 = L\frac{dI_L}{dt} = -L(g_1 + 2g_2 v_1)\frac{dv_1}{dt}, \tag{27}$$

$$I_1 = (g_1 v_2 + g_2 v_2^2) = -Lg_1(g_1 + 2g_2 v_1)\frac{dv_1}{dt} + L^2 g_2(g_1^2 + 4g_1 g_2 v_1 + 4g_2^2 v_1^2)\left(\frac{dv_1}{dt}\right)^2, \tag{28}$$

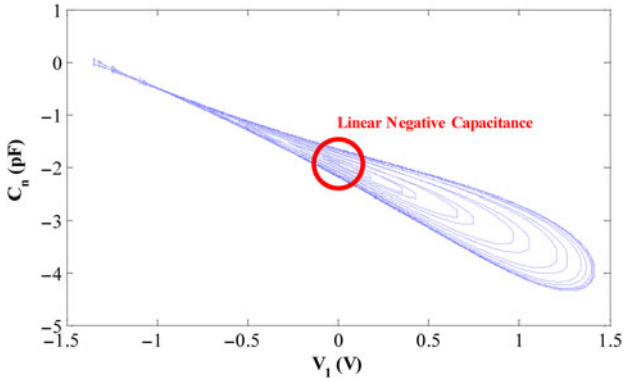


Fig. 9. The curve of negative capacitor $C_n(t)$ versus $V_1(t)$.

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Table 4. Parameters of nonlinear model of negative capacitor.

$B_n \times 10^{-23}$ and $C_n \times 10^{-12}$			
Parameter	**Analytic**	**Formula**	**Curve fitting**
C_0	$-Lg_1^2$	−1.9360–1.9325	
C_1	$-2Lg_1g_2$	−1.4344	−1.4338
C_2	–	–	−0.0017
C_3	–	–	−0.0005
C_4	–	–	0.0007
C_5	–	–	0.0008
B_0	$L^2g_1^2g_2$	3.1557	3.1801
B_1	$4L^2g_1g_2^2$	4.6761	4.8176
B_2	$4L^2g_2^3$	1.7323	1.6169

$$I_1 = C\left(v_1, \frac{dv_1}{dt}\right)\left(\frac{dv_1}{dt}\right), \tag{29}$$

$$C\left(v_1, \frac{dv_1}{dt}\right) = C_0 + C_1 v_1 + \left[B_0 + B_1 v_1 + B_2 v_1^2\right]\frac{dv_1}{dt}. \tag{30}$$

In this section, by using the results of the analysis based on proposed method in time domain, the nonlinear negative capacitor is extracted, according to voltage and other parameters (31, 32).

$$C(t) = \frac{dq(t)}{dv(t)}, \tag{31}$$

$$q(t) = \int_0^t i(t)dt. \tag{32}$$

With certain considerations in numerical calculation such as avoiding divide by zero (too small $dv(t)$) and considering the neighborhood $(t-h, t+h)$, Δq, Δv, and $C_n(t)$ are calculated according to equations (33–36).

$$\Delta v(t) = V(t+h) - V(t-h), \tag{33}$$

$$\Delta q(t) = \int_{t-h}^{t+h} i(t)dt, \tag{34}$$

$$C_n(t) = \frac{\Delta q(t)}{\Delta v(t)}, \tag{35}$$

$$V(t) = \frac{[V(t+h) + V(t-h)]}{2}. \tag{36}$$

By eliminating the time as the independent variable, the curve of $V(t) - C(t)$ is obtained, which is shown in Fig. 9, like the curve of V-I, middle rings belong to rise and fall

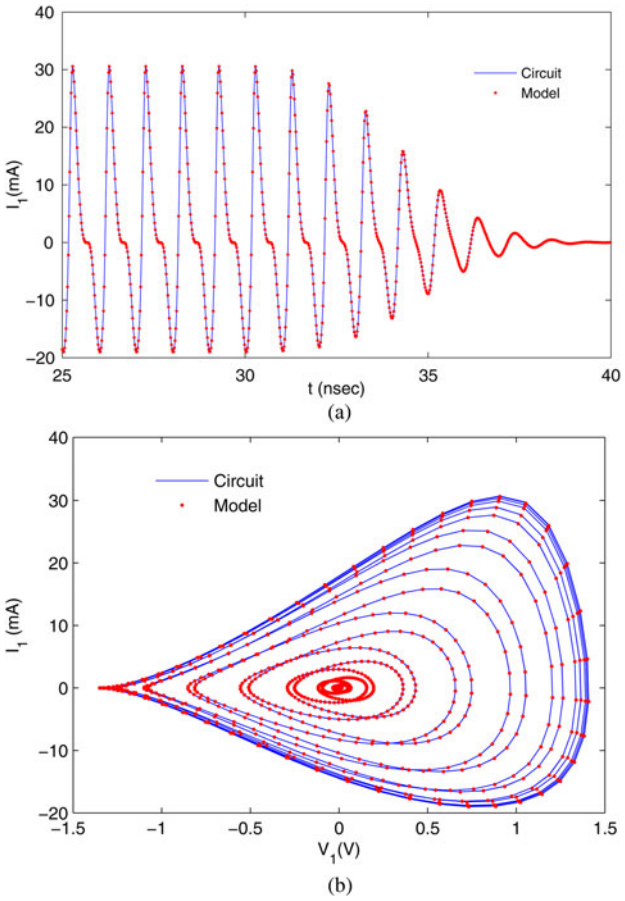


Fig. 10. Simulation results of circuit and model of negative capacitance ($V_p = 3$ V, $f_c = 1$ GHz), (a) $I_1(t)$, (b) $I_1(t)$ versus $V_1(t)$.

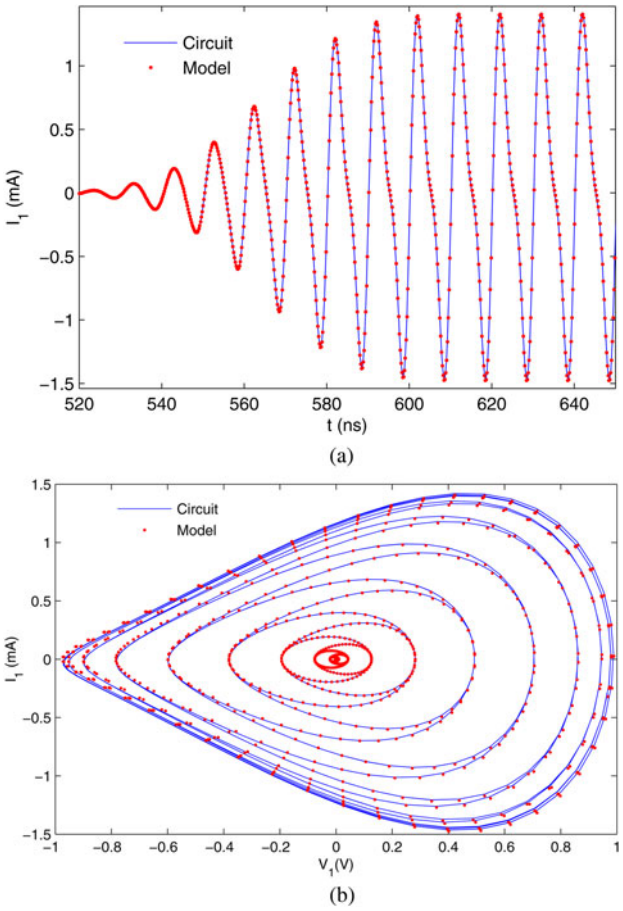


Fig. 11. Simulation results of circuit and model of negative capacitance ($V_p = 1$ V, $f_c = 100$ MHz), (a) $I_1(t)$, (b) $I_1(t)$ versus $V_1(t)$.

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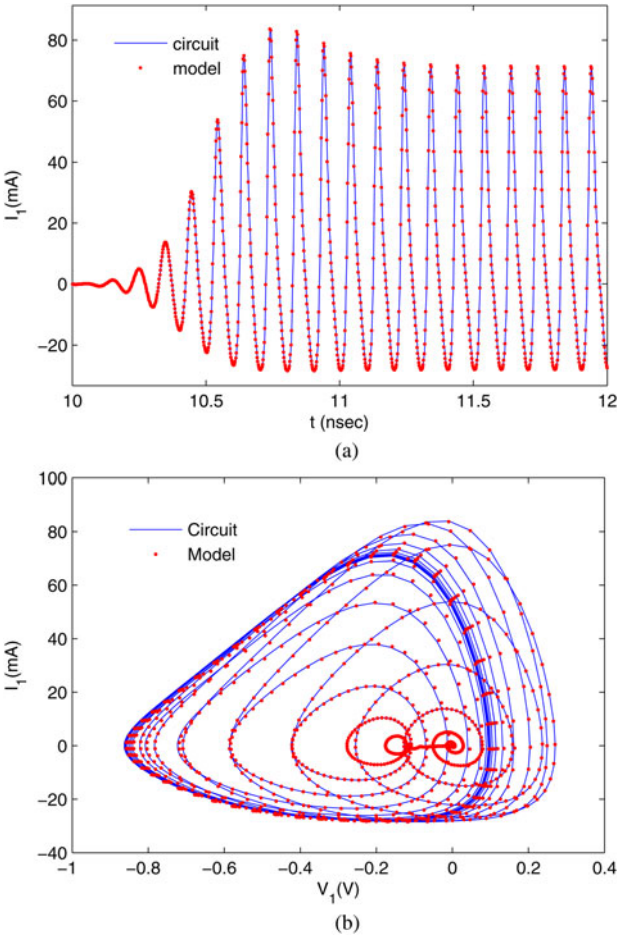


Fig. 12. Simulation results of circuit and model of negative capacitance ($V_p = 10$ V, $f_c = 10$ GHz), (a) $I_1(t)$, (b) $I_1(t)$ versus $V_1(t)$.

times of pulse while outer rings belong to the steady state response of the circuit. In this figure, the nonlinear negative capacitance in each ring, is a function of $V_1(t)$ and its temporal changes and at a distinctive ring for a certain voltage, the upper part of $C_n(t)$ belongs to upward change of $V_1(t)$ and the downward part is related to decline of $V_1(t)$ with time.

Table 5 Comparsion of the results of the HB and the transient analysis for input signal with $V_p = 3$ V and $f_c = 1$ GHz.

Fourier transform of transient analysis					
frequency	**1 GHz**	**2 GHz**	**3 GHz**	**4 GHz**	**5 GHz**
$\lvert V_{1(circuit)}\ (mV)\rvert$	1387.6	115.7	24.35	9.85	4.15
$\lvert V_{1(model)}\ (mV)\rvert$	1387.5	115.7	24.42	9.80	4.10
$\lvert I_{1(circuit)}\ (mA)\rvert$	17.91	11.86	3.704	1.992	1.048
$\lvert I_{1(model)}\ (mA)\rvert$	17.91	11.86	3.716	1.981	1.033
HB analysis					
Harmonic number	**1st**	**2nd**	**3rd**	**4th**	**5th**
$\lvert V_{1(circuit)}\ (mV)\rvert$	1383.8	114.9	23.99	9.53	3.70
$\lvert V_{1(model)}\ (mV)\rvert$	1383.7	114.8	24.03	9.44	3.54
$\lvert I_{1(circuit)}\ (mA)\rvert$	17.66	11.78	3.650	1.925	0.934
$\lvert I_{1(model)}\ (mA)\rvert$	17.65	11.77	3.635	1.907	0.892

According to the operation point of circuit and the relation of negative capacitance in the linear regime, the corresponding value is obtained (38).

$$g_m = 44\ \mathrm{m}/\Omega, \tag{37}$$

$$C_n = -g_m^2 L = -1.93\mathrm{pF}. \tag{38}$$

In the V-C diagram, at inner rings and for $V_1(t) = 0$, the negative capacitance is obtained equal to that of the linear regime. While by increasing the amplitude of V_1, the absolute value of the negative capacitance increases.

Based on the analytic formula, the representation of negative capacitor with more parameters as degrees of freedom is shown as:

$$C\left(v_1, \frac{dv_1}{dt}\right) = C_0 + C_1 v_1 + C_2 v_1^2 + C_3 v_1^3 + C_4 v_1^4 + C_5 v_1^5 + \left[B_0 + B_1 v_1 + B_2 v_1^2\right]\frac{dv_1}{dt}. \tag{39}$$

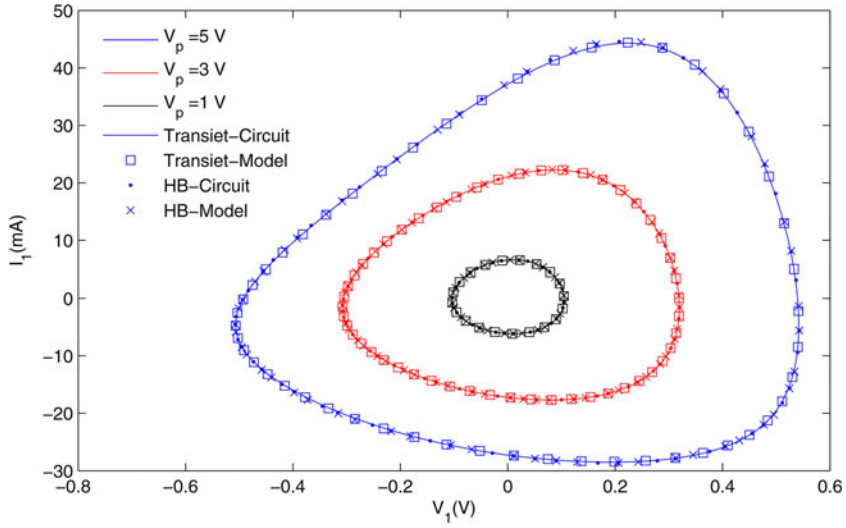


Fig. 13. Simulation results of transient and HB analysis of circuit and proposed model of negative capacitance for various amplitudes of input signal ($V_p = 1,\ 3,\ 5$ V) at $f_c = 5$ GHz.

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By applying least square method (LSM) to curve fitting the function (39), the parameters of model were obtained as shown in Table 4, that have a good agreement with analytic coefficients of model.

Based on simulation results ($V_p = 3$ V, $f_c = 1$ GHz), the C-V diagram is obtained and the coefficients of model are calculated. In Fig. 10, the simulation results of NIC circuits and negative capacitor model are compared and have a good agreement.

In Fig. 11 ($V_p = 1$ V, $f_c = 100$ MHz) and Fig. 12 ($V_p = 10$ V, $f_c = 10$ GHz), the results of model and circuit simulation are compared in other frequencies to validate model behavior.

For extra validation of proposed model, the HB analysis of circuit and model are studied. The values of all harmonics are compared with Fourier transform of steady state response of transient analysis in each harmonic frequency. The results are shown for ($V_p = 3$ V, $f_c = 1$ GHz) in Table 5.

By applying inverse Fourier transform, the time domain response of circuit are calculated from HB results. These results are compared with steady state response of sinusoidal input signal in transient analysis. The V-I steady state cycles for sinusoidal input signal for transient and HB analysis are shown in Fig. 13. The simulations are performed for diffrent amplitudes of input signal in $f_c = 5$ GHz. These results show very good agreements with each other, that validated proposed nonlinear model of negative capacitor.

The total capacitance and the time constant of the circuit will be negative and the circuit becomes unstable if the capacitor at the input of circuit is not large enough. By extraction and modeling of negative capacitance in the nonlinear regime and choosing suitable input capacitor and other parameters, the circuit stability can be obtained.

VII. CONCLUSION

Nonlinear analysis of non-Foster structures can be an important step for applying them in circuits with high power level such as power amplifiers and electrically small antennas in the transmitting mode. The analysis in the time domain and the transient response of the circuit helps us to study the stability of circuit and it can be analyzed by using the extracted nonlinear negative capacitor. At the first step, a simple nonlinear model for the transistor was used to analyze these structures. Then by adding parasitic elements to the model, more accurate analysis of the circuit will be presented.

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