THERMAL AND ELECTRICAL CHARACTERIZATION OF POWER MOSFET MODULE USING COUPLED FIELD ANALYSIS

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ABSTRACT

Temperature resulting from the joule heating power and the turn-on and turn-off dissipation of high-power, high-frequency applications is the root cause of their thermal instability, electrical performance degradation, and even thermal-fatigue failure. Thus, the study presents thermal and electrical characterizations of the power MOSFET module packaged in SOT-227 under natural convection and forced convection through three-dimensional (3D) thermal-electric (TE) coupled field analysis. In addition, the influences of some key parameters like electric loads, ambient conditions, thermal management considerations (heat sink, heat spreader) and operation conditions (duty cycle and switching frequency) on the power loss and thermal performance of the power module are addressed. The study starts from a suitable estimation of the power losses, where the conduction losses are calculated using the temperature- and gate-voltage-dependent on-state resistance and drain current through the device, and the switching losses are predicted based on the ideal switching waveforms of the power MOSFETs applied. The effectiveness of the theoretical predictions in terms of device's power losses and temperatures is demonstrated through comparison with the results of circuit simulation and thermal experiment.

Keywords: Power MOSFET, Thermal Performance, Power Loss Estimation, Coupled Thermal-electric Analysis, Natural and Forced Convection

1. INTRODUCTION

Power electronics applies power semiconductor devices, such as bipolar junction transistor (BJTs), gate turn-off thyristor (GTO), silicon-controlled rectifier (SCR), triode for alternating current (TRIAC), diode alternating current (DIAC), metal-oxide semiconductor field effect transistor (MOSFET) and insulated-gate bipolar transistor (IGBT) etc., for electrical power management and conversion. Among them, power MOSFET and IGBT semiconductor devices have been drawing great interest and attention in contemporary power electronics due to fast technological evolution. Compared to IGBTs [1-3], though having larger on-state resistance and so conduction losses, power MOSFETs have advantages of lower switching loss and faster switching speed, which extends power conversion switching frequencies to beyond 100kHz [4]. Consequently, power MOSFETs are more favorable for use in high switching frequency applications. They have become the leading device in power electronics for power electronic switches.

The current development trend of power electronics is toward high power, high switching frequency, and high operation temperature. In particular, for improving fuel efficiency, a kilowatts (kWs) range of power is being applied. On the other hand, power electronics are being engineered to attain high reliability, low cost, minimal energy loss, reduced weight and miniaturization. The high power and downsizing of power electronics lead to high power density. Presently, high power density has been one of the crucial drivers for the development of power conversion technology. High power density inevitably leads to high power losses. In addressing the thermal

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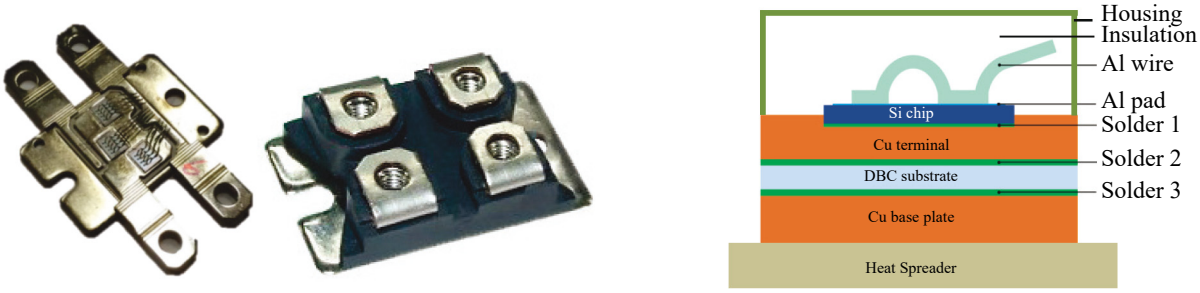
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issues of power devices and even their electrical and mechanical performances, power losses are the main heat sources. Power losses in power devices mainly comprise two portions: the conduction loss caused by the on-state resistance and the switching loss by the charging and discharging of the input capacitance. In order for achieving minimized power losses, both on-state resistance and input capacitance need to be reduced. On-state resistance can be reduced through an increased die size and a lowered specific on-state resistance, which can be accomplished by a large critical breakdown electric field and high carrier mobility [5]. Unfortunately, the trade-off of increased die size is the increase in the input capacitance and also the switching loss. Switching loss is linearly proportional to the switching frequency, and high switching loss may restrict semiconductor devices from high-frequency operation. Temperature also plays a significant role in the power losses and performance of power devices. Because of increased phonon concentration and lattice scattering, elevated temperature would degrade the carrier mobility and so increase the on-state resistance [6]. Typically, the on-state and gate resistances possess a large positive temperature coefficient [2], where, e.g., the on-state resistance of power devices follows a power law relation with temperature [7]. High power losses lead to high junction temperature rise, which would in turn cause additional power losses, and further produce an increase in the junction temperature. The cycle would eventually result in thermal runaway if the generated heat is not effectively removed. From the perspective of thermal stability, junction temperature is the crucial parameter for high power density power devices [8]. High junction/operation temperature would not only cause power devices' thermal instability and electrical performance degradation but also deteriorate their mechanical and thermal fatigue behaviors, due to the induced thermal stresses by mismatch in coefficient of thermal expansion (CTE) among the component materials [9]. It has been extensively reported that temperature is the primary cause (as high as 55%) of the failure of electronic components.[3,10,11] As reported in military standardization handbook [12] that if the temperature of electronic components increases by 2°C at a threshold temperature, their fatigue life would drop about 10%. Similarly, for power electronics components, a rise of operating temperature of 10˚C would approximately double the failure rate [13]. Thus, the top design considerations for power devices include: 1) the device junction temperature should not exceed the rated one, which is generally determined mainly based on the limit of the maximum leakage current (see, e.g., [5]), and 2) the power loss and thermal management would not result in thermal runaway and thermal fatigue failure. In other words, the power device's power handling capability is limited by the maximum junction temperature rating (typically 150°C) [14]. Therefore, there is an increasing concern on the thermal performance of power devices, especially high power, high operation temperature and high switching frequency devices [15]. A clear understanding of their thermal performance allows for better and effective thermal management to ease the potential of thermal instability and even thermal fatigue failure.

Prior to comprehending the thermal performance of power devices, it is of importance to accurately characterize their power losses. However, accurate power loss estimation of power devices is still a challenging task today. This can be attributed to that 1) the current and voltage waveforms profiles are highly determined by several key factors like junction temperature, load condition and physical parameters of the power devices, and 2) the switching timescale is on the order of hundreds to thousands of nanoseconds, which is millions to billions times smaller than the thermal time constant of the power conversion devices, i.e., on the order of tens to hundreds minutes [16]. This indicates that millions to billions of switching events are required for the modeling, which is by no means straightforward. Over the past years, extensive efforts have been made to assess the power losses and thermal performance of power semiconductor devices and modules through various experimental and numerical approaches [2,5,13,14,17-20]. For instance, Fang et al. [2] numerically and experimentally performed a DC power cycling test to evaluate the temperature distribution of an IGBT power module under different current loads, and besides, the temperature variations in the electronic components were examined based on the relationship between temperature cycles and thermal resistance; Wang [5] proposed several power density figures of merit for power MOSFET and IGBT from the standpoint of junction temperature, power loss and package, followed by the test and analysis of the electrical characteristics and thermal stabilities; Kibushi et al. [17] investigated the thermal behaviors of power Si MOSFET using electro-thermal analysis; Bouzida et al. [19] conducted an estimate of IGBT's and diode's losses in a switching operation as a function of the circuit and the temperature variation during operation using a feasible loss model. The loss model was further coupled with an RC (Foster) network using the thermal impedance to construct an electro-thermal model for junction temperature calculation; Liao et al. [20] studied the electrical, thermal and mechanical behaviors of an IGBT power module due to joule heating during high current conditions using electro-thermal finite element analysis.

Temperature arising from power dissipation is the main cause of the thermal instability, electrical performance degradation and thermal-fatigue failure of high-power, high-frequency power modules. According to the literature survey, there remains limited understanding and study of the power losses and thermal stability of power MOSFET devices. Thus, the objective of the study is to investigate the electrical and thermal behaviors of a power MOSFET module packaged in SOT-227 at various electric loads, PWM duty cycles, ambient conditions, thermal management considerations (heat sink/spreader, forced air) and cooling conditions (natural convection and forced convection) through numerical analysis and experimental validation. To prevent thermal runaway, the maximum junction temperature rating, 150°C, is considered as the limit of thermal stability. In this study, a three-dimensional (3D) coupled field analysis model is

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(a) Prototype (b) Vertical structure

Fig. 1 100V 350A SOT-227 power MOSFET module

proposed, which integrates the coupled thermal-electric (TE) analysis in ANSYS® and the flow simulation in Solidworks®. In the investigation, both conduction and switching losses are taken into account and calculated, respectively, based on the temperature- and gate-voltage-dependent on-state resistance and the root-mean-square (RMS) on-state drain current depending on the duty cycle through the device, and based on the ideal switching transients and the corresponding datasheets [21,22]. The switching loss of power MOSFETs increases much insignificantly with temperature, as compared to bipolar power devices such as IGBT [5]; as a result, its temperature dependence is not included. The theoretical predictions in terms of the device's power losses and temperatures are validated against the circuit simulation using ANSYS Simplorer® and thermal experiment using thermocouple.

2. GEOMETRY AND STRUCTURE OF POWER MOSFET MODULE

Three 100 V 350 A Si power MOSFET semiconductor devices are employed in the SOT-227 power MOSFET module shown in Fig. 1 (a). For heat dissipation, the power modules are mounted onto either an aluminum (Al) heat spreader with a size of 160×145×6 (mm) or an Al or copper (Cu) heat sink. Two different sizes of heat sinks are considered, and the dimension of them can be found in Fig. 5. The SOT-227 power MOSFET module has four terminals (one gate, one drain, and two sources) with captive nuts for electrical connections. As pointed out by Wang [9], low power device can be utilized to fulfill high switching frequency and high-power devices through parallel connection. Chou et al. [22] found that two parallel HEMT cells are operated at a safe working distance from thermal runaway to prevent destruction of the hottest cell, and besides, the thermal stability and switching behavior of these cells are balanced. Thus, in order to increase the current rating, the module consists of three parallel-connected power MOSFETs.

A schematic of the vertical structure of the modules is given in Fig. 1(b). In addition to the silicon power MOSFETs and Al wires, the power modules consist of seven other layers of materials, namely, Al pads, Cu terminal leads, a direct bonded copper (DBC) substrate, a Cu base plate, a polyphenylene sulfide (PPS) housing, a quick-drying rubber based adhesive (cement) used to fill the space between the housing and the DBC/Cu terminal leads for insulation, and three SAC305 solder layers (i.e., Solder 1, 2, 3) used to bond the silicon MOSFETs and the Cu terminal leads, the Cu terminal leads and the DBC substrate and the DBC substrate and Cu cold plate, respectively. The core material between the upper and bottom copper of the DBC is Al_2O_3. The corresponding thicknesses are 0.33 (chip), 0.01 (pad), 0.8 (terminal leads), 0.45 (substrate), 2.0 (base plate), 0.05 (solder 1), 0.1 (solder 2) and 0.1 (solder 3) (mm). Twelve Al wires are bonded to the Al pads on these three MOSFETs. The power module on heat spreader is applied as the test sample in the subsequent thermal experiment. For MOSFET transistors, a voltage at the gate regulates the current that flows between the drain and source. In an MOSFET transistor, two depletion zones are formed by the two PN junctions (source/bulk and drain/bulk) between the drain and source terminals. The electrical resistance between the junctions is considerably high when they are reverse-polarized. The MOSFET transistor is turned off, where no electron conduction takes place. As the gate voltage is above the threshold voltage, i.e., the minimum gate-to-source voltage needed to generate a channel of electrons between the source and drain terminals, the MOSFET transistor is turned off. Because of the controlling terminal, it allows for signal controls in electronic circuits. It should be noted that unlike IGBT devices, power MOSFETs use their intrinsic body diodes.

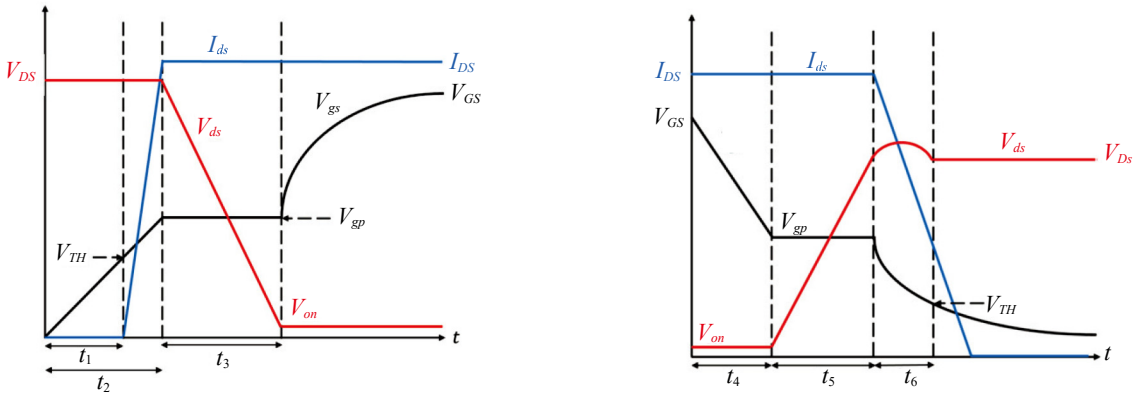
3. POWER LOSS ESTIMATION

The power losses of power MOSFET devices need to be first estimated. The estimation of the conduction loss P_C and switching loss P_S of MOSFET devices operating in the switch-mode can be briefly described below.

3.1 Conduction Loss Estimation

Conduction loss occurs in the manner of Joule's heating when the MOSFET is turned on with a conducting current (I_{DS}) (i.e., the MOSFET on-state current). The main contribution of the conduction loss is the equivalent resistance in power devices. The conduction loss at a period of switching cycle t_{sw} can be approximately described by the conduction dissipation for an MOSFET

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(a) Turn-on waveform (b) Turn-off waveform

Fig. 2 Switching transients of the power MOSFET

with a conductive resistance $R_{DS(on)}$ (i.e., the drain-to-source on-state resistance),

$$P_C = \frac{1}{t_{sw}} \int_0^{t_{sw}} I_{DS}^2(t) R_{DS(on)}(T) dt = I_{DS}^2 R_{DS(on)}(T) . \quad (1)$$

The on-state resistance is highly temperature-sensitive. The assumptions behind the formula are that the leakage current is negligible, the switching frequency is high and the on and off switching time of MOSFETS and diodes are insignificant compared to the switching cycle time t_{sw}. The temperature-dependent on-state resistance raises a crucial thermal challenge in power module design, i.e., the conduction loss produces a temperature rise, which in turn, generates more conduction loss due to the increase of the on-state resistance with temperature. Thus, the temperature dependence of the conduction loss should be considered in the thermal modeling.

PWM is a modulation technique to control the power fed to electrical devices, such as inductance motors. The current (or voltage) supplied to the electrical devices is regulated by rapidly turning on and off the switch between them. An "on" time period (on-time pulse width) longer than an "off" time period (off-time pulse width) in a PWM cycle allows more electrical power to be given to the electrical devices. The ratio between the on-time pulse width and the switching cycle time is denoted as duty cycle (*D*). Accordingly, the conduction loss calculated in Eq. (1) should be modified by multiply the duty factor. For modeling simplification, an average power dissipation using an RMS average current (I_{RMS}) across a PWM cycle is applied. For a square-wave PWM technique, the RMS average current is expressed as,

$$I_{RMS} = I_{DS} (D)^{1/2} . \quad (2)$$

With the RMS average value of the MOSFET on-state current, the conduction loss can be rewritten as,

$$P_C = I_{RMS}^2 R_{DS(on)}(T) . \quad (3)$$

3.2 Switching Loss Estimation

Switching loss of power semiconductor devices during the switching transition can be divided into two parts: the turn-on (E_{on}) and turn-off energy dissipation (E_{off}). The turn-on energy dissipation is mainly attributed to the increase in the current of MOSFETs from the trivial leakage current up to the on-state current and at the same time, the drop in the voltage from the high off-state voltage to the very small on-state voltage. On the other hand, the turn-off energy dissipation can be due to the current fall from the on-state current to the small leakage current and meanwhile, the voltage rise from the small on-state voltage to the high off-state voltage. Also, there is a positive linear dependence between the switching energy losses and switching frequency. For a high switching application, the switching loss may even play a more important role in the thermal behavior than the conduction loss, and thus, should be included in the thermal analysis and design. The total switching energy loss E_{sw} can be denoted as,

$$E_{sw} = E_{on} + E_{off} = \int_0^{t_{sw}^{on}} I_{ds}(t) V_{ds}(t) dt + \int_0^{t_{sw}^{off}} I_{ds}(t) V_{ds}(t) dt , \quad (4)$$

where t_{sw}^{on} and t_{sw}^{off} are the turn-on and turn-off switching peiods. The total swiching loss is the sum of the turn-on and turn-off energy dissipations,

$$P_S = f_{sw} E_{sw} , \quad (5)$$

where f_{sw} is the switching frequency.

In literature, a few approaches have been proposed to rigorously characterize the switching loss in MOSFETs (see, e.g., [21,22]). Despite usually being effective for the switching loss estimation, they are not quite efficient for a long-period driving profile. Instead, a simple analytical approach is proposed based on the ideal voltage and current waveforms of the power MOSFETs in the turn-on and turn-off periods and the corresponding datasheets, as shown in Fig. 2, where the nonlinear curves are approximated by a piecewise-linear function. The following gives a brief introductoin of the turn-on

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characteristics. Assume the switch is open at $t=0$, the gate-to-source capacitance C_{gs} begins to charge, and the gate-to-source voltage V_{gs} increases. As soon as the voltage V_{gs} reaches the threshold voltage V_{TH} at $t=t_1$, current starts to flow in the drain. At $t>t_1$, charge of the C_{gs} goes on, the V_{gs} continues to raise, and the drain current I_{ds} rises correspondingly until attaining the specified drain current I_{DS} and the V_{gs} reaches the gate plateau voltage V_{gp} at $t=t_2$. At $t>t_2$, the I_{ds} and V_{gs} keep staying at I_{DS} and V_{gp}, respectively, while the drain-source voltage V_{ds} has a significant gradual fall from the supply voltage V_{DS}. Since the drain current remains at I_{DS} at the period, the V_{gs} stays at the gate plateau voltage V_{gp}, suggesting that there is no further charge on the C_{gs}. At $t=t_3$, the V_{ds} drop down to the conduction voltage V_{ON} that is equal to $I_{DS}R_{DS(on)}$.

Assume the turn-off period begins at t=0. In the first stage of turn-off, the V_{gs} starts to fall and discharges the device capacitances C_{gs} and C_{gd} through R_g and L_s. At this stage, the I_{ds} and V_{ds} remain constant (i.e., I_{DS} and V_{ON}, respectively) until V_{gs} decreases to the V_{gp} at t=t_4. As $t>t_4$, V_{ds} starts climbing. Ideally, the I_{ds} would stay at I_{DS}, and V_{gs} remains equal to V_{gp}. As soon as the V_{ds} reaches the supply voltage V_{DS} at t=t_5, the I_{ds} and also V_{gs} start falling off from I_{DS} and V_{gp}, respectively. At t=t_6, the V_{gs} attains the threshold voltage V_{TH}.

Assume that the effects of parasitic inductance that exists in each pin of the power MOSFETs are neglected and no external gate resistance is applied. The switching loss can be analytically approximated from the typical voltage and current waveforms (turn-on and turn-off periods) based on Baliga [21] and Brown [22],

$$t_1 = R_g C_{iss} \ln\left(1\Big/\left(1-\frac{V_{TH}}{V_{GS}}\right)\right), \tag{6}$$

$$t_2 = R_g C_{iss} \ln\left(1\Big/\left(1-\frac{V_{gp}}{V_{GS}}\right)\right), \tag{7}$$

$$t_3 = R_g C_{gd}\left(\frac{V_{DS}}{V_{GS}-V_{gp}}\right), \tag{8}$$

In Eqs. (6)-(8), R_g is the internal gate resistance and C_{iss} is the input capacitance equal to $C_{gd}+C_{gs}$, where C_{gd} denotes the gate-to-drain capacitance,. With these three turn-on time periods, the turn-on power loss can be given as,

$$P_{S(on)} = \frac{1}{2} I_{DS} V_{DS} f_{sw}(t_2 - t_1 + t_3). \tag{9}$$

The turn-off power loss can be obtained using the same principle,

$$P_{S(off)} = \frac{1}{2} I_{DS} V_{DS} f_{sw}(t_5 + t_6), \tag{10}$$

where

$$t_5 = R_g C_{gd} \times \frac{V_{DS}}{V_{gp}}, \tag{11}$$

$$t_6 = R_g C_{iss} \times \ln\left(\frac{V_{gp}}{V_{TH}}\right), \tag{12}$$

The above simple models are to give a preliminary switching loss prediction of power devices in the initial design phase. A more rigorous prediction model for the final design phase should be made based on the power-temperature calculation that takes into account the effects of reverse recovery current and parasitic inductance.

3.3 Conduction Losses in Cu terminal leads and Al wires

Power flows from the drain to the source, passing through the long tiny Al wires and Cu terminal leads, and the lessening in voltage due to their equivalent resistances causes energy dissipation. The power dissipation creates a temperature rise in the long tiny Al wires and Cu terminal leads and even the power MOSFET devices, which further affects the resistances. Due to large current, the equivalent resistances may not be ignored. The conduction power losses can be calculated using coupled TE analysis with the derived on-state resistance from the approximate formula,

$$R^L = \frac{\varsigma L}{A}, \tag{13}$$

where R^L is the equivalent resistance of the long tiny Al wires and Cu terminal leads, L is the length, ς is the resistivity, and A is the cross-sectional area.

4 ANALYSIS APPROACHES

A precise estimation of the junction temperature of the power MOSFET plays a significant role in the design and optimization of the power modules. Besides, the junction temperature of power MOSFET semiconductor devices affects the amount of power losses (and so the current), which in turn determines the junction temperature. Hence, there is a crucial need of performing TE coupled filed analysis. In this investigation, together with the prediction results of switching loss, a 3D coupled TE FE model is created using ANSYS® to simulate the current density (and hence the temperature-dependent conduction loss) and also temperature of the power MOSFET devices in both forced and natural convection cooling.

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Table 1: Electrical and thermal material properties of the SOT-227 power MOSFET module

Part	Material	Thermal conductivity (W/m·K)	Resistivity (Ω·m)
Housing	PPS 40%G.F.	1.2	1×10^{12}
Insulation	Cement	0.15	1×10^{12}
Wire	Aluminum	210	3.10×10^{-8} at 25℃ 4.55×10^{-8} at 150℃
Pad	Aluminum	210	3.10×10^{-8} at 25℃ 4.55×10^{-8} at 150℃
Chip	Silicon	130	Fig. 4
Solder	SAC305	58	1.32×10^{-7}
Terminal	Copper	391.1	1.88×10^{-8} at 25℃ 2.74×10^{-8} at 150℃
DBC substrate	Al_2O_3	24.7	1×10^{12}
Base plate/ Heat spreader	Copper	391.1	1.88×10^{-8} at 25℃ 2.74×10^{-8} at 150℃
Heat spreader/sink	Aluminum(ADC12)	96.2	2.50×10^{-8}

4.1 Coupled TE Analysis [23]

The thermal transport equation applied in the coupled TE analysis is given as follows:

$$\rho C_p \frac{\partial T}{\partial t} + \nabla \cdot \mathrm{q} = \dot{q}\,, \tag{14}$$

where ρ, C_p and T are the density, specific heat, and temperature, and $\mathbf{q}$ and $\dot{q}$ the heat flux vector and heat generation rate per unit volume, respectively. By Fourier's law, the heat flux vector $\mathbf{q}$ is proportional to the product of the negative temperature gradient $-\nabla T$ and the thermal conductivity k,

$$\mathrm{q} = -k\nabla T. \tag{15}$$

For an anisotropic material, thermal conductivity along different geometrical axes may present a different value.

The continuity equation for an electromagnetic problem is defined as,

$$\nabla \cdot \mathrm{J} + \frac{\partial \mu}{\partial t} = 0\,, \tag{16}$$

where $\mathbf{J}$ stands for the electric current density vector and μ the free electric charge density defined as,

$$\nabla \cdot \mathbf{D} = \mu\,. \tag{17}$$

Eq. (17) is Gauss's law, where $\mathbf{D}$ denotes the electric flux density vector. It should be noted that the time-varying electric flux density (alternatively termed displacement current density) $\partial D/\partial t$ is included, which is particularly essential for the present fast transient switching process.

The above governing equations of thermoelectricity are coupled with the following constitutive laws of thermoelectric and dielectric materials,

$$\mathrm{q} = -[\mathrm{K}]\cdot\nabla T + [\Pi]\cdot \mathrm{J}\,, \tag{18}$$

$$\mathbf{J} = [\sigma]\cdot\left(\mathbf{E} - [\alpha]\cdot\nabla T\right), \tag{19}$$

$$\mathbf{D} = [\varsigma]\cdot\mathbf{E}\,, \tag{20}$$

where $\mathbf{E}$ is the electric field intensity vector, $[\mathrm{K}]$ the thermal conductivity matrix, $[\alpha]$ the Seebeck coefficient matrix, $[\Pi]$ the Peltier coefficient matrix equal to $T[\alpha]$, $[\sigma]$ the electric conductivity matrix, and $[\varsigma]$ the dielectric permittivity matrix.

For a steady magnetic field, the third of Maxwell's equation, also termed Faraday's law can be written as

$$\nabla \times \mathbf{E} = 0\,. \tag{21}$$

The irrotational electric field can be expressed from an electric potential ϕ as,

$$\mathbf{E} = -\nabla\phi\,. \tag{22}$$

With Eq. (22), the constitutive law of a dielectric material can be rewritten as,

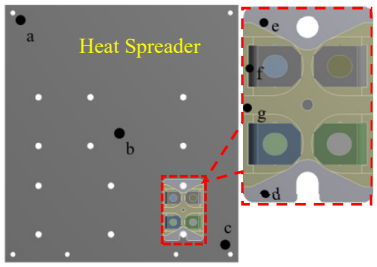
$$\mathbf{D} = -[\varsigma]\cdot\nabla\phi\,. \tag{23}$$

Then, substituting Eqs. (21)-(23) into Eqs. (18) and (19) yields a set of strongly coupled equations of thermoelectricity:

$$\rho \mathrm{C_p}\frac{\partial \mathrm{T}}{\partial \mathrm{t}} + \nabla\cdot\left(-[\mathrm{K}]\cdot\nabla \mathrm{T} + [\Pi]\cdot \mathrm{J}\right) = \dot{\mathrm{q}}\,, \tag{24}$$

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Table 2: Temperature comparison among thermal measurements and coupled TE analysis at 40 A and 50 A currents

Location		Thermocouple		Coupled TE analysis	
		40 A	50 A	40 A	50 A
	a	39.3	49.7	38.9	46.1
	b	41.5	49.9	40.0	47.8
	c	42.9	53.8	42.1	51.3
	d	41.5	52.4	42.1	51.3
	e	41.9	52.0	41.8	50.9
	f	40.0	46.1	42.0	51.1
	g	40.8	47.9	40.7	49.0
	chip	-	-	43.4	53.5

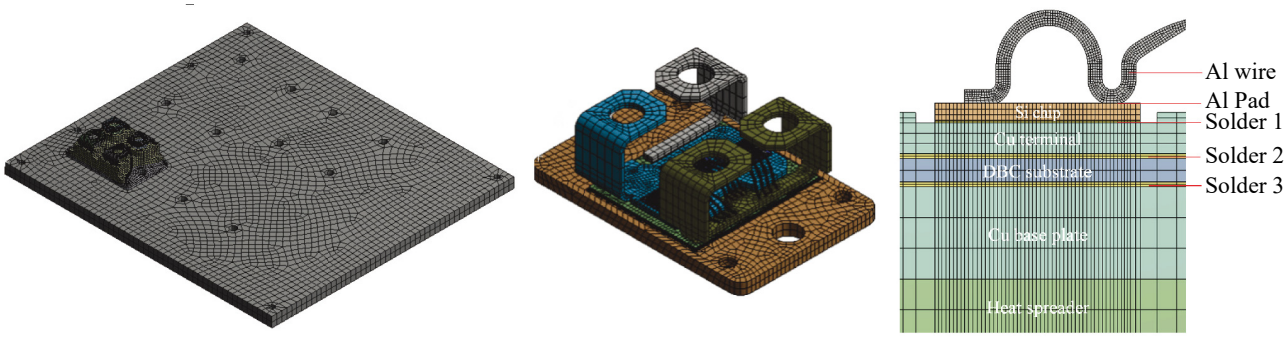


Fig. 3 3D TE FE models of the SOT-227 power MOSFET module on heat spreader

$$\nabla\cdot\left(\left[\varepsilon\right]\cdot\nabla\frac{\partial\phi}{\partial t}\right)+\nabla\cdot\left(\left[\sigma\right]\cdot\nabla\phi+\left[\sigma\right]\cdot\left[\alpha\right]\cdot\nabla T\right)=0\,, \quad (25)$$

The electric power (i.e., $\mathbf{J}\cdot\mathbf{E}$) is included in the heat generation term $\dot{q}$ in Eq. (24).

4.2 Heat Conduction FE Modeling

3D TE FE models are created for the SOT-227 power MOSFET module with the heat spreader and heat sink. The former is used only for the thermal experiment, and its 3D TE FE model is shown in Fig. 3, in which it comprises all the major components, namely the three silicon MOSFETs, Al wires, Al pads, Cu terminal leads, direct bonded copper (DBC) substrate, Cu base plate, three SAC305 solder layers, PPS housing and cement insulation. The FE model consists of 174628 elements and 464920 nodes. The material properties of the power MOSEFT module used in the coupled TE analysis are presented in Table 1. The equivalent output characteristics of the power module with the 100 V 350 A power MOSFETs at temperatures of 25 °C and 150 °C are measured and displayed in Fig. 4. The slope of the I_d–V_{ds} curves denotes the inverse of the equivalent on-state resistance, which can be further used to determine the temperature-dependent electrical resistivity of the silicon power MOSFET chips. It is clear to see that the on-state resistance presents high temperature dependence. The temperature-dependent equivalent on-state resistances are implemented in the coupled field analysis for determining the temperature-dependent conduction loss of the power MOSFETs.

4.3 Surface Heat Transfer

For natural convection heat transfer, the following convective heat transfer model h_{nc}^{c} introduced by Ellison [24] is applied to depict the heat dissipating from the surface of packages to the external environment,

$$h_{nc}^{c}=0.83f\left(\left(T_w-T_a\right)/\overline{L}\right)^{n}, \quad (26)$$

where T_a denotes the ambient temperature, T_w is the surface temperature of module, $\overline{L}$ is the characteristic length, and f and n are constants [24].

For radiation heat transfer, the standard radiative heat transfer model h_r is used,

$$h^{r}=\overline{B}\varphi\xi\left(T_w+T_a\right)\left(T_w^2+T_a^2\right), \quad (27)$$

where $\overline{B}$ represents the Stephen-Boltzmann constant equivalent to 5.678×10^{-8} (W/m^2-K^4), ξ the surface emissivity ($0<\xi<1$), and φ the radiative view factor ($0<\varphi<1$). The emissivities of the surface materials of the SOT-227 power module, i.e., the PPS housing, Cu terminal leads and DBC and Al heat streader, are 0.95, 0.22 and 0.27. The emissivities of the surface materials of the three-phase bridge inverter, namely polyamide shell and the Al conductive columns (and also heat spreader), are 0.92 and 0.27, respectively.

The effective heat transfer coefficient $\overline{h}$ for depicting

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Table 3: Switching losses of the SOT-227 power MOSFET module at three different supply currents

V_{DS}=50 V		Turn-on loss (W)	Turn-off loss (W)	Total switching loss (W)
75 A	Analytical	3.44	4.67	8.11
	Modeling	3.80	4.43	8.23
100A	Analytical	4.65	6.19	10.84
	Modeling	5.07	5.91	10.98
125A	Analytical	5.90	7.73	13.63
	Modeling	6.34	7.38	13.72

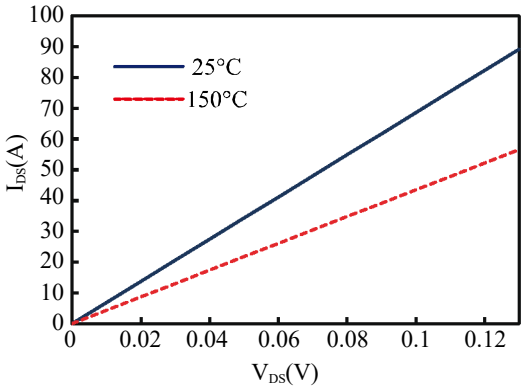


Fig. 4 Equivalent output characteristics (I_{DS}-V_{DS}) of the three-parallel connected SOT-227 power MOSFETs

the total surface heat transfer in a natural/forced convection environment can be calculated by summing the radiative and convective heat transfer coefficients.

4.4 Thermal Experiment

The surface temperatures of the SOT-227 power MOSFET module on the heat spreader, as shown in Fig. 3, are characterized using thermocouples. Seven K-type thermocouples are attached to different locations on the top surface of the power module on a heat spreader using a proper amount of silver-filled epoxy attachment, as schematically shown in Table 2. Specifically, three of them (i.e., points "a", "b", and "c" in the figure) are placed on the top surface of the heat spreader, two (i.e., points "d", and "e") on that of the Cu base plate, one (i.e., point "f") on that of the drain terminal, and one (i.e., point "g") on that of the PPS housing. The thermal resolution of the type of thermocouples is 0.1 ºC and the measurable range is 0-200 ºC. The natural convection test environment follows the EIA/JEDEC standard JESD51-2 [25,26], where in order to prevent the internal environment from external thermal disturbances, the test sample is placed in a lightproof cubic box made of black acrylic with a side length of one foot. A thermocouple of T-type with a possible measurement variation ± 0.1 ºC is placed at one inch below the test sample in the cubic box for measuring the ambient temperature.

For facilitating the thermal measurement, the power module on heat spreader is connected in series with both a DC 12 V power supply to supply an input DC supply current to the power module via the drain terminal, and a function generator to offer a square wave input via the gate terminal. The current flows from the higher to lower potential through the copper layer of the DBC, solder 2, Cu terminal leads, solder 1, MOSFET chips, Al pad, Al wires, and finally into the output voltage region. In the thermal experiments, the function generator provides 4 kHz square wave 0-10V peak to peak with a 100% duty cycle. In other words, a full conduction modulated output signal is generated such that there is no switching action and also switching loss. Accordingly, the thermal experiment only accounts for the conduction loss.

5 RESULTS AND DISCUSSION

5.1 Validation of the Proposed Coupled TE FE Model

The measured ambient temperature in the cubic box is about 27 ºC. The power MOSFET test vehicle is operated at 40 A and 50 A, and a PWM duty cycle of 100%. As soon as the temperature of the test specimen, i.e., the SOT-227 power MOSFET module on the Al heat spreader, reaches a steady state or thermal equilibrium, then the surface temperatures of the test specimen at these reference points ("a"-"g") are measured using thermocouples. The measurement results are presented in Table 2, together with the modeled data using the coupled TE analysis. Noticeably, there is a good agreement between these two results. In addition, an increasing current leads to the increase of temperature at all these reference points, where the temperatures would approximately increase about 10 ºC as the electric load rises from 40 A to 50 A.

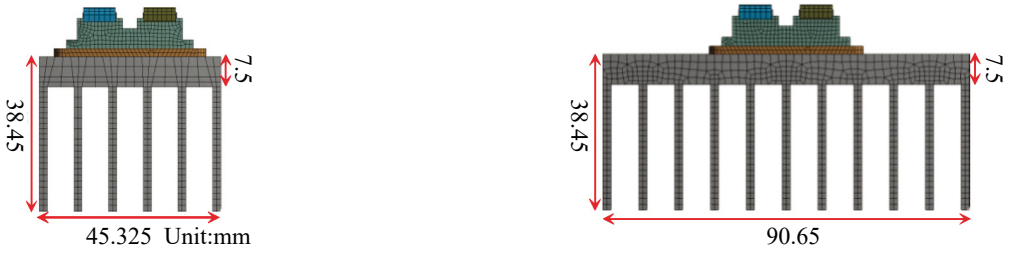
5.2 Switching Loss of Power MOSFET Module

The switching losses, namely the turn-on ($P_{S(on)}$) and turn-off ($P_{S(off)}$), of the power MOSFET module are calculated for operation with a 50 V supply voltage, three different supply currents (i.e., 75 A, 100 A and 125 A), and a 14 kHz switching frequency are calculated using the simple analytical formulae, Eqs. (9) and (10). The calculated switching losses are also compared with those obtained from the circuit simulator ANSYS Simplorer®. The results are listed in Table 3. The table shows that there is a very good consistency in the switching losses between the analytical and numerical approaches. Since the parasitic effects, like parasitic inductance, and the reverse recovery characteristics of the power MOSFET body

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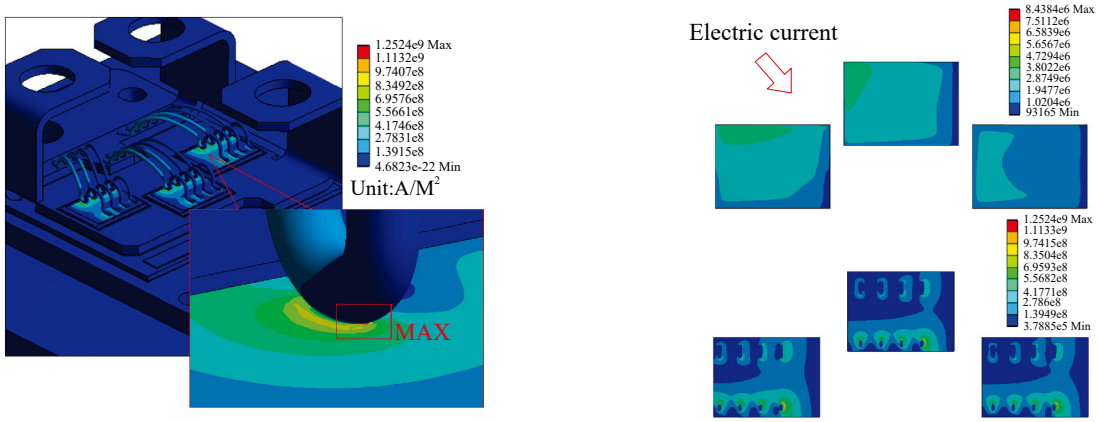
Table 4: Natural convection thermal performance of the power module with the small Al heat sink

Ambient temp.(°C)	Supply current (A)	Junction temp. (°C)	Al wire temp. (°C)
27	75	122.1	125.9
	100	170.1	178.8
	125	230.9	247.6
37	75	130.2	134.0
	100	177.8	186.6
	125	238.4	255.4
47	75	137.8	141.7
	100	185.1	194.1
	125	245.5	262.7



(a) Small heat sink (b) Large heat sink

Fig. 5 3D FE models of the power module with a small and large heat sink



(a) Power module (b) Solder (top)/A1(bottom)

Fig. 6 Current density distribution of the power module

diode were not taken into account in the modeling, there is a need of further improvement of the simple analytical approach. Besides, the effects of temperature on the switching losses deserves further attention despite that the degree of the influence on the switching losses is much less than that on the conduction losses. The table also reveals that the increasing current causes an increase in the switching losses. The turn-off loss turns out to be slightly larger than the turn-on loss. This can be simply explained based on the voltage and current waveforms in the turn-on and turn-off periods, as shown in Fig. 2. In the "t_2-t_1" period of the turn-on waveform, the drain current I_{ds} increases from zero at V_{gs}=V_{th}, up to the supply drain current I_{DS} at V_{gs}=V_{gp} while in the corresponding period of the turn-off waveform, i.e., "t_6", the I_{ds} drops from I_{DS} at V_{gs}=V_{gp} down to a non-zero value at V_{gs}=V_{th}. The drain current at V_{gs}=V_{th} makes the difference between the turn-on and turn-off power losses.

5.3 Coupled TE Analysis of Power MOSFET Module with Heat Sink under Natural Convection

The TE behaviors of the SOT-227 power MOSFET module with a heat sink in natural convection under different supply drain currents and ambient conditions are assessed using the verified 3D coupled TE analysis model. Two different heat sinks, each with a different size, are considered. Figure 5 illustrates the FE models of the power module attached with a small heat sink and a large heat sink. Noticeably, these two heat sinks possess an identical height and fin thickness, i.e., 38.45 mm and 2.0 mm, respectively, but have a different fin pitch and width,

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Table 5: Conduction losses of the power module with the small Al heat sink in natural convection

Ambient temp. (°C)	Supply current (A)	Conduction loss (W)			
		Si MOSFET	Al wire	Cu lead	Total
27	75	7.40	1.25	0.89	9.54
	100	14.99	2.53	1.78	19.3
	125	27.00	4.54	3.10	34.64
37	75	7.55	1.28	0.91	9.74
	100	15.22	2.56	1.80	19.58
	125	27.36	4.59	3.14	35.09
47	75	7.74	1.31	0.93	9.98
	100	15.50	2.61	1.83	19.94
	125	27.78	4.66	3.24	35.68

Table 6: Natural convection thermal performance of the power module with the large Al/Cu heat sink

Ambient temp.(°C)	Heat sink material	Supply current (A)	Junction temp. (°C)	Al wire temp. (°C)
27	Al	100	86.0	94.1
		125	109.1	123.4
	Cu	100	84.3	92.6
		125	105.9	120.4
37	Al	100	94.0	102.4
		125	117.0	131.5
	Cu	100	92.2	100.8
		125	113.9	128.7
47	Al	100	102.3	110.8
		125	125.6	140.5
	Cu	100	100.4	109.2
		125	122.7	137.8

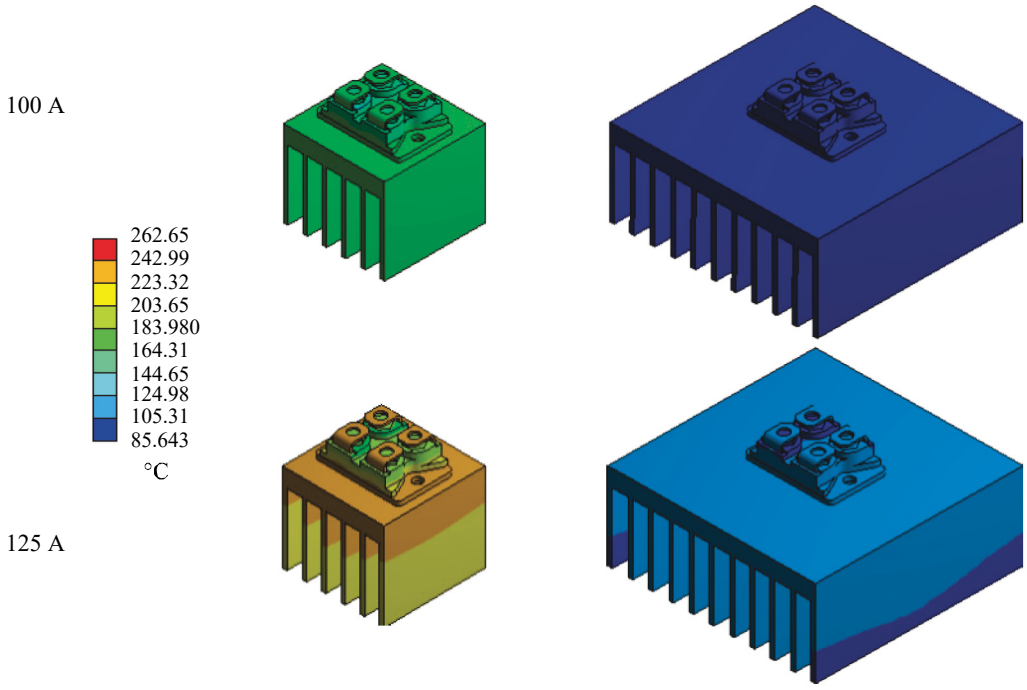
Table 7: Conduction losses of the power module with the large Al heat sink in natural convection

Ambient temp. (°C)	Supply current (A)	Conduction loss (W)			
		Si MOSFET	Al wire	Cu lead	Total
27	100	11.52	2.02	1.54	15.08
	125	19.32	3.42	2.56	25.30
37	100	11.82	2.07	1.58	15.47
	125	19.80	3.47	2.62	25.89
47	100	12.13	2.12	1.62	15.87
	125	20.33	3.55	2.69	26.57

where they are 6.665 mm and 45.325 mm for the small heat sink, and 6.865 mm and 90.65 mm for the large heat sink. Roughly, the volume of the large heat sink is four times the small one.

The current density distribution of the power module with the small Al heat sink operated at a supply current of 125 A is shown in Fig. 6(a). The peak current density is 1.2524×10^3 A/mm^2, and takes place at the edges of the Al pads and Al wires, where current crowding effect is observed. This could be mainly attributed to the dramatic size reduction as the electric current flows from the Al pads to the Al wires; as a result, current crowding occur at these regions. The peak current density falls into the reported threshold value for electromigration of Al metals [27](i.e., 10^3-10^4 A/mm^2), and thus may potentially cause the formation of voids and hillock in the Al pads in a long-term operation. At a higher electric load (>125 A), the current crowding effect would become more intense, leading to a more severe electromigration. To date, electromigration failures have become one of the key reliability issues for high-power and current applications. Furthermore, the current density distribution in the solder layers is shown in the top of Fig. 6(b), where the electric current enters the solder layers from the drain side, as shown with an "arrow" in the figure. The major part of electric current directly flows into the solder layers by way of the Cu terminal leads because of better electrical conductance, leading to a significant current density

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(a) Small heat sink (b) Large heat sink

Fig. 7 Temperature distribution of the power module on the small and large Al heat sink in natural convection at 100 A and 125 A and an ambient temperature of 47°C.

gradient across the solder. In addition, a much larger current density in the site of entry of electric current (left-top-hand side) is seen than in the site of exit, but no significant current crowding is detected. The current density distribution in the Al pads is also displayed in the bottom of Fig. 6(b). It is clear to see that there is a current crowding phenomenon in the region near the Al wire bond where the electric current flows into the Al wires.

At a 50% PWM duty cycle, the maximum junction temperatures and Al wire temperatures of the power module with the small Al heat sink at the supply currents of 75 A, 100 A and 125 A, and the ambient temperatures of 27 ºC, 37 ºC and 47 ºC are displayed in Table 4. Examples of the temperature distributions across the power module at 100 A and 125 A and an ambient temperature of 47 ºC are demonstrated in Fig. 7(a). Note that the calculated switching losses listed in Table 4 are applied in this investigation. Irrespective of the ambient conditions and supply currents, the maximum temperature all takes place at the Al wires, instead of the parallel-connected power MOSFETs, and more interestingly, the difference in temperature between the power MOSFETs and Al wires increases with the increase of the supply current. On the other hand, except the case with the supply current of 75 A, the junction temperatures of the power MOSFETs all exceed the maximum junction temperature rating, i.e., 150°C, indicating that there exists a high risk of thermal runaway for the power MOSFET module with the small Al heat sink, and also suggesting a need for a better thermal solution.

The corresponding conduction losses of the silicon power MOSFETs, Al wires and Cu terminal leads in the power module with the small Al heat sink are presented in Table 5, for these three different supply currents and ambient conditions. Evidently, the conduction losses increase substantially with the supply current but to a much lesser extent with the ambient temperature. Moreover, it is interesting to see that the silicon power MOSFETs are the major source of the conduction loss, which takes about 78% of the total conduction loss. This also suggests that the Cu terminal leads and Al bond wires would account for about 22%. The considerable contribution to the total conduction loss implies that they are important for an accurate prediction of the thermal behavior of the power MOSFET module. It is also found that an increase of 33.3% (from 75 A to 100 A) and 25% (from 100 A to 125 A) in supply current brings about 102% and 80% increases in conduction loss, respectively. This extent of increase appears to be not equal to the theoretical value given in Eq. (3), i.e., the square of the increased percentage of supply current. In addition, the increased rate in the conduction loss is larger than the theoretical value. Temperature is the main cause of the deviation or the additional increase in the conduction loss. For the 125 A, the conduction losses exceed 34 W, indicating that effective thermal design and management are of critical demand to rule out the possibility of thermal runaway. Besides, by comparing with the switching losses presented in Table 3, the conduction losses for the 75 A are comparable to the switching losses while for the 100 A and 125 A, the conduction losses become much more dominant. In other words, the conduction losses have a greater raise than the switching losses when simply increasing the electric load.

Next, a larger heat sink is utilized to improve the natural convection heat dissipation capability of the power

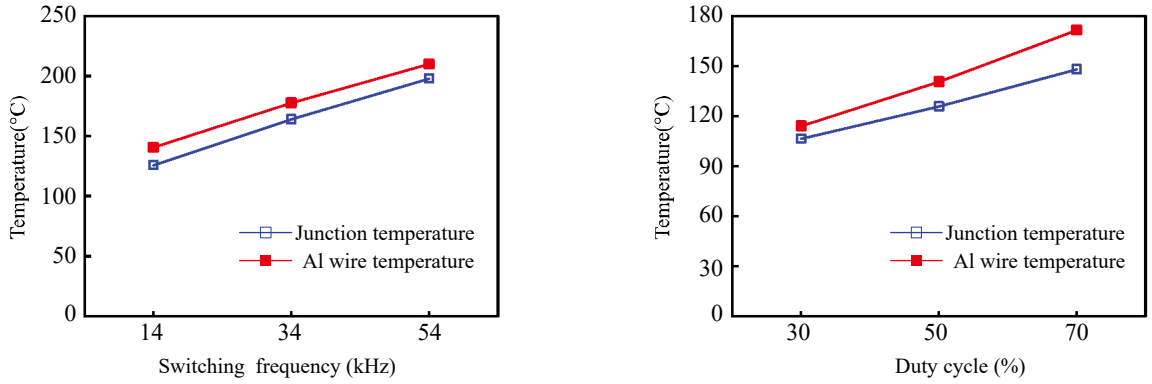
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Table 8: Forced convection thermal performance of the power module with the small Al heat sink at 125 A.

Ambient temp. (°C)	Wind speed (m/s)	Junction temp.(°C)	Al wire temp.(°C)
27	1	121.2	136.0
	2	95.8	109.5
	3	88.6	102.1
37	1	133.0	148.0
	2	107.5	121.6
	3	100.0	113.9
47	1	144.3	159.9
	2	119.1	133.7
	3	111.3	125.6

Table 9: Conduction losses of the power module with the small Al heat sink in forced convection

Ambient temp. (°C)	Wind speed (m/s)	Conduction loss (W)			
		Si MOSFET	Al wire	Cu lead	Total
27	1	20.50	3.51	2.43	26.44
	2	18.92	3.26	2.26	24.44
	3	18.51	3.19	2.21	23.91
37	1	21.20	3.62	2.46	27.28
	2	19.61	3.37	2.34	25.32
	3	19.18	3.30	2.29	24.77
47	1	21.88	3.73	2.54	28.15
	2	20.30	3.48	2.41	26.19
	3	19.85	3.41	2.36	25.62



(a) Switching frequency (b) Duty cycle

Fig. 8 Effects of switching frequency and duty cycle on the thermal performance of the power module with the large Al heat sink under natural convection.

module under the 100 A and 125 A supply currents. Two different materials of heat sink, namely Al and Cu, and the three ambient conditions (27 °C, 37 °C and 47 °C) are addressed. The results are reported in Table 6. Examples of the temperature distributions over the power module with the large Al heat sink at 100 A and 125 A and an ambient temperature of 47 °C are illustrated in Fig. 7(b). The figure clearly demonstrates that the heat removal capability of the large heat sink surpasses the small one. Moreover, both the large Al and Cu heat sinks can effectively reduce the junction temperature down to below the specific maximum junction temperature rating, thereby reducing the risk of thermal runaway. Despite much better thermal conductance, the large Cu heat sink can have only about 3 °C reduction in the junction temperatures and Al wire temperatures, compared to the large Al heat sink.

The corresponding conduction losses of the power module with the large Al heat sink are given in Table 7, for these two different supply currents (100 A and 125 A) and three ambient conditions (27 °C, 37 °C and 47 °C). Similarly, the conduction losses tend to increase greatly

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with an increasing supply current but slightly with an increasing ambient temperature. Worth noting is that under the same supply current and ambient condition, the large heat sink could considerably reduce about 4 and 10 watts of the total conduction losses for the 100 A and 125 A supply current, respectively, as compared to the small heat sink. In addition, with the use of the large heat sink, the difference in the total conduction loss between the 100 A and 125 A decreases from about 15 W down to 10 W for all these three ambient conditions. Besides, the percentage contribution of the conduction losses of the Cu terminal leads and Al wires to the total conduction loss increases from about 22 % to about 23.5 %.

5.4 Effects of Forced Convection

Active cooling is an effective alternative for heat removal from the surface of the power module to the ambient. Thus, in addition to natural convection (passive cooling), active cooling with forced air is applied. For comparison with the results of the passive cooling with the large heat sink, the thermal performance of the power module attached with the small Al heat sink under forced convection is assessed. This analysis is performed with a supply current of 125 A, three wind speeds of 1.0, 2.0 and 3.0 (m/sec) and three ambient temperatures of 27, 37 and 47 (°C). The direction of the air flow is parallel to the surface of the fin wall. The local surface heat transfer coefficients of the power module in forced convection at different wind speeds and surface temperatures are first evaluated using Solidworks fluid flow thermal simulation. The characterized local surface heat transfer coefficients are used as the thermal boundary condition in the coupled TE analysis to describe the surface heat transfer. The analysis results are listed in Table 8. The table reveals that the forced convection is also very effective in removing heat from the power module, compared to the natural convection, and an increasing wind speed increases the heat removal performance and so reduces the junction temperature of the power MOSFETs. By comparing Table 8 with Table 7, we find that the forced convection with the small Al heat sink at a wind speed of 2 m/s and above tends to outperform the natural convection with the large Al heat sink. This implies that at a wind speed of 1 m/s or less, the latter would contribute to a better heat removal than the former. It is also found that the heat removal ability of the forced convection seems to saturate as the wind speed is larger than 2 m/s.

For the forced convection, the conduction losses of the power module are presented in Table 9, for these three ambient conditions and wind speeds. Likewise, the conduction loss would increase with an increasing ambient temperature but lessen with an increasing wind speed. Compared with the conduction losses of the power module with the small Al heat sink under natural convection, their conduction losses in the forced convection become significantly reduced. Furthermore, only the conduction losses at the wind speed of 1 m/s would be larger than those with the large Al heat sink under natural convection, irrespective of the ambient conditions. This also explains why the thermal performance of the power module with the small Al heat sink under forced convection with a wind speed of 1 m/s would be worse than that with the large Al heat sink under natural convection.

5.5 Effects of Switching Frequency

The influences of the switching frequency and PWM duty cycle on the thermal performance of the SOT-227 power MOSFET module under natural convection are evaluated. The module is attached with the large Al heat sink. Three different switching frequencies and duty cycles are considered, namely 14 kHz, 34 kHz and 54 kHz, and 30%, 50% and 70%, respectively. For the investigation, the electric load is 125 A and the ambient temperature is 47 °C. The calculated results are demonstrated in Fig. 8. It shows that both these two factors have a considerable impact on the junction temperature and Al wire temperature of the power module, where the thermal performance of the power module would decrease with an increasing switching frequency and duty cycle, mainly due to the increase of the switching loss and conduction loss, respectively.

6 CONCLUSIONS

This study applies the proposed 3D coupled field analysis model to investigate the electrical and thermal behaviors of the SOT-227 power MOSFET module under various electric loads, ambient conditions, thermal management considerations and cooling conditions. The switching losses are calculated from the ideal switching current and voltage waveforms, and the conduction losses from the on-state resistance and drain current through the device. The theoretical prediction results, namely switching losses and temperatures, are compared with those obtained from the circuit simulator ANSYS Simplorer® and thermal experiments using IR thermometer and thermocouples, respectively. Besides, the effects of PWM duty cycle and switching frequency on the power losses and thermal performance are also addressed. Some essential remarks are briefed below:

- Good agreement in the switching losses between the simple analytical approach and circuit simulation and also in the temperatures between the thermal experimental and numerical results is shown, indicating the effectiveness of the simple analytical approach for power loss estimation and the proposed 3D coupled TE analysis model.
- Current crowding region is located at the edges of the Al pads and Al wires due to dramatic dimension change.
- Electromigration failure may occur in the Al pads of the power module with the small Al heat sink while operated at 125 A in a long-term period.
- The maximum temperature of the power module occurs at the Al wires, rather than the power MOSFETs.
- Thermal runaway may take place in the power module with the small Al heat sink operated at 100 A and 125 A with a 50% PWM duty cycle since the maximum junction temperatures and Al wire temperatures go

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beyond 150 °C.

- Even though the silicon power MOSFETs are shown to be the major source of the conduction loss, the Cu terminal leads and Al bond wires would also considerably contribute to the conduction loss, which could not be neglected in order for a more accurate prediction of the thermal performance.
- For a supply current of 75 A, the conduction losses of the power module are proved to be equivalent to the switching losses, while for a higher supply current, like 100 A, the conduction losses become much more prominent.
- Compared with the small heat sink, the large heat sink can be more effective in lessening the conduction losses and junction temperatures of the power module, and so minimize the thermal runaway probability even at an electric load of 125 A.
- The forced convection with the small Al heat sink at a wind speed of 2 m/s and above has a superior heat removal capability to the natural convection with the large Al heat sink.
- A decreasing switching frequency and duty cycle and an increasing wind speed would enhance the thermal performance of the power module.

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