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RESEARCH PAPER

Toward highly scaled AlN/GaN-on-Silicon devices for millimeter wave applications

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In this work, the possibility of achieving GaN-on-Si devices for millimeter wave applications operating at high bias is demonstrated. It is shown that highly scaled AlN/GaN-on-Si double heterostructure enables us to significantly improve electron confinement under high electric field as compared to single heterostructure while delivering high carrier density ($>2 \times 10^{13}$ cm^{-2}). Subsequently, trapping effects can be minimized resulting in the highest GaN-on-Si output power density up to 40 GHz and at a drain bias of 15 V together with a record f_{max} close to 200 GHz. At higher bias, infrared camera analysis clearly shows that these devices are mainly limited by self-heating effects. Furthermore, low noise figure has been assessed on this heterostructure, promising integration of cost effective low noise and high power millimeter wave amplifiers.

Keywords: GaN-on-Si, Millimeter wave, AlN/GaN, Power amplifiers

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I. INTRODUCTION

Enhancement of GaN-based devices grown on silicon frequency performance is of increasing interest since this would enable cost-effective integration of this outstanding technology with very mature CMOS Si-based devices paving the way for novel circuit architecture with higher functionalities [1]. For this purpose, an aggressive scaling of gate length is required while maintaining a high aspect ratio by reducing the gate to channel distance as well as the use of a short gate–drain distance in order to create a high electric field as needed for high frequency performance [2, 3]. An attractive solution to reduce the gate to channel distance has been proposed lately [4–6], which consists of the use of an Al-rich ultrathin barrier layer (<10 nm) delivering extremely high two-dimensional electron gas (2DEG) carrier density. This allows avoiding the well-known gate recess technique that is difficult to control for GaN devices and may induce reliability issues at a very high frequency. However, the combination of ultrathin barrier layer and high 2DEG density induces generally a large gate leakage current that has been observed by several groups [7]. Recently, this limitation has been overcome for AlN/GaN high-electron-mobility transistors (HEMTs) owing to a high AlN film quality associated to a controlled surface by using an *in-situ* grown SiN cap layer [8].

Nevertheless, even though the gate leakage current has been minimized in the AlN/GaN-on-Si devices, a high 2DEG density in highly scaled GaN HEMTs may generate poor electron confinement under high bias (e.g., high electric field). A Double-heterostructure field effect transistor (DHFET) using an AlGaN back barrier is an interesting approach to enhance electron confinement [9, 10].

In this work, dc, radio frequency (RF), pulsed, load-pull, and noise measurements up to 40 GHz of short channel AlN/GaN HEMTs and AlN/GaN/AlGaN DHFETs grown on silicon are presented. The benefits of the back barrier resulted in the first demonstration of high RF output power density at 40 GHz and a record f_{max} close to 200 GHz for a GaN-on-Si device limited by the self-heating effect at drain bias higher than 15 V as seen from thermal assessment performed with an infrared camera.

II. DEVICE DESCRIPTION

The AlN/GaN heterostructures were grown by metal organic chemical vapor deposition (MOCVD) on a highly resistive 4 inch Si (111) substrate. The HEMT structure consists of transition layers to GaN, a 1.5-μm-thick GaN buffer layer followed by a 6.0 nm ultrathin AlN barrier layer, and a 3.0-nm-thick *in-situ* Si_3N_4 cap layer (see Fig. 1). In the second structure called DHFET, the 1.5-μm-thick GaN buffer layer has been replaced with a 1.5-μm-thick $Al_{0.08}Ga_{0.92}N$ layer and a 150 nm GaN channel. Room-temperature Hall measurements showed high electron sheet concentrations of 2.2×10^{13} and 2×10^{13} cm^{-2} with mobilities of 1200 and 1400 $cm^2\ V^{-1}\ s^{-1}$ in the HEMT and DHFET heterostructures, respectively.

Ohmic contacts have been formed with a Ti/Al/Ni/Au metal stack rapidly thermally annealed at 850°C directly on top of the AlN barrier layer by etching the *in-situ* Si_3N_4 layer. Device isolation was achieved by nitrogen implantation.

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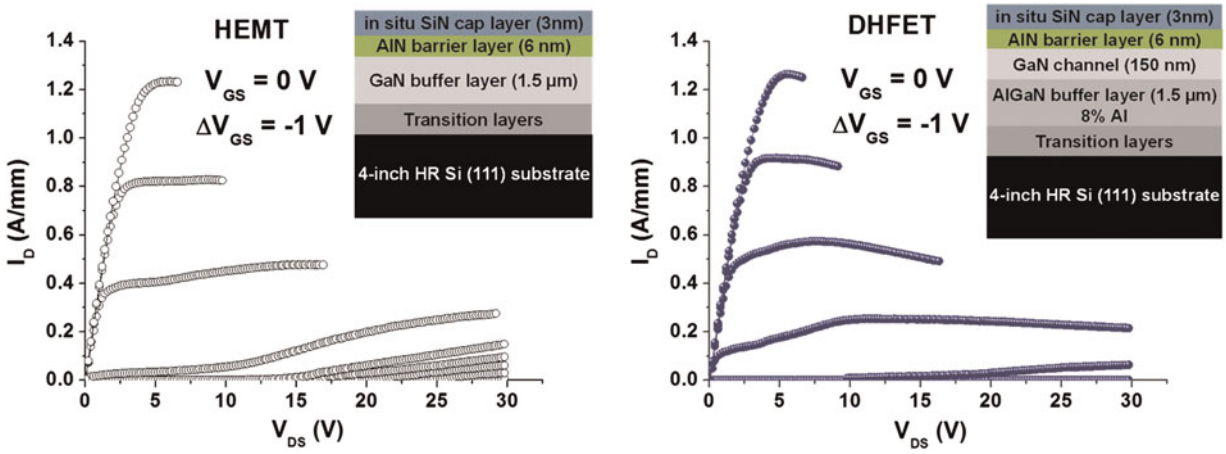


Fig. 1. DC output characteristics and cross sections of a 2 × 25 µm AlN/GaN-on-Si HEMT (left) and DHFET (right) with L_g = 0.2 µm. V_{GS} swept from pinch-off to 0 V in 1 V steps.

Ohmic contact resistance (R_c) extracted from linear transmission line model structures was as low as 0.35 Ωmm for both heterostructures. Then, 50 nm Si_3N_4 was deposited by plasma-enhanced CVD, and gate lengths (L_g) ranging from 0.2 to 0.08 µm were defined by e-beam lithography. The SiN underneath the gate was fully removed by SF_6 plasma etching. Another e-beam lithography step has been used in order to deposit Ni/Au gate metals. The gate–source and gate–drain spacings were 0.3 and 1 µm, respectively, and the device width was 50 µm. Finally, 100 nm Si_3N_4 was deposited as final passivation.

III. RESULTS AND DISCUSSIONS

A) Dc performance

Dc output characteristics of 2 × 25 µm AlN/GaN-on-Si HEMT and DHFET are shown in Fig. 1. The current density at open channel (around 1.25 A/mm at V_{GS} = 0 V) and the maximum transconductance (470 mS/mm) are comparable for both heterostructures. However, a significant punch-through effect is observed for the HEMT structure resulting in a strong shift of the threshold voltage when increasing the drain bias. This is due to electron injection into the GaN buffer layer that is subjected to extremely high electric field in these highly scaled devices. This undesirable effect does not appear in the DHFET owing to the AlGaN back barrier that prevents parasitic electron conduction into the buffer layer, which results in a sharp pinch-off and a high breakdown voltage.

Pulsed IV for different quiescent bias points highlighting the so-called gate and drain lag effects of 2 × 25 µm AlN/GaN-on-Si HEMT and DHFET are shown in Fig. 2. Reasonably low gate lag effect is observed in both cases indicating a high material and processing quality. However, a significant drain lag effect appears for the HEMT structure due to parasitic conduction under high bias. In the case of the DHFET the drain lag effect at 15 V remains fairly low owing to substantial improvement of electron confinement.

B) RF performance

Current gain extrinsic cut-off frequencies and maximum oscillation frequencies f_T = 44 and 52 GHz and f_{max} = 68 and 91 GHz for HEMT and DHFET have been extrapolated

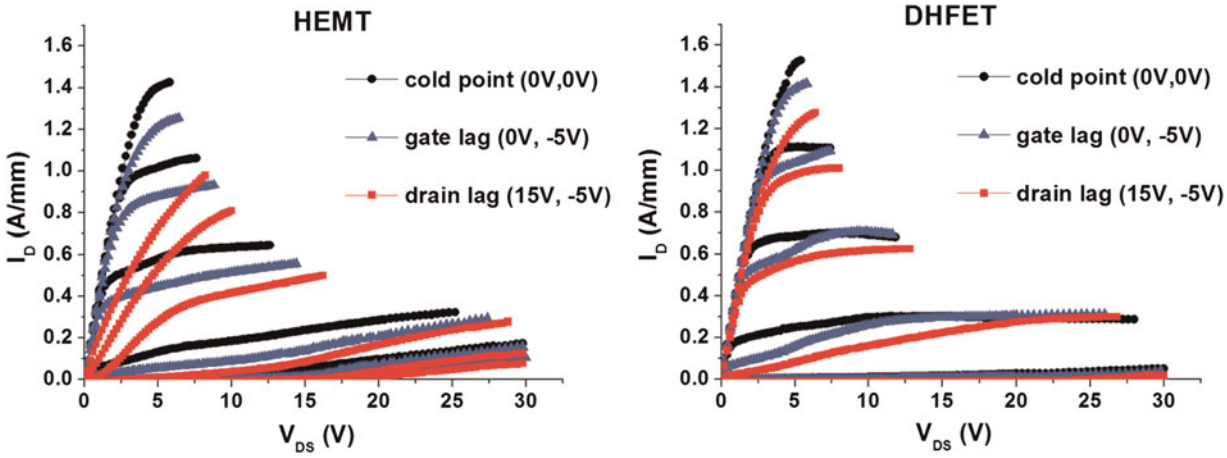


Fig. 2. Pulsed IV for different quiescent bias points highlighting the gate and drain lag effects of a 2 × 25 µm AlN/GaN-on-Si HEMT (left) and DHFET (right). V_{GS} swept from pinch-off to 0 V in 1 V steps.

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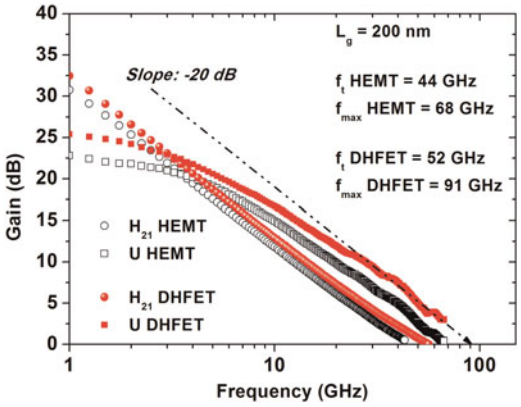


Fig. 3. RF performance of a 0.2 × 50 μm² AlN/GaN HEMT and DHFET on highly resistive silicon substrate at $V_{DS} = 6$ V and $V_{GS} = -1.6$ V.

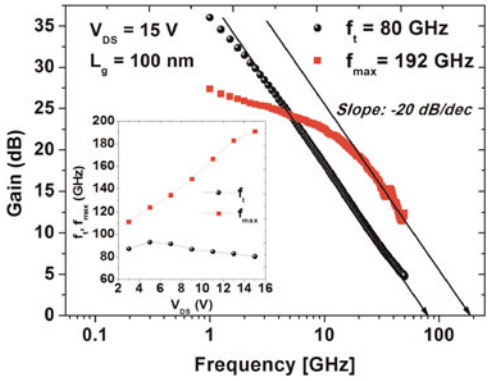


Fig. 4. RF performance of a 0.08 × 50 μm² AlN/GaN DHFET on 4-inch Si at $V_{DS} = 15$ V.

from current gain H_{21} and unilateral power gain (U) at $V_{GS} = -1.6$ V and $V_{DS} = 6$ V, respectively (Fig. 3). The reduction of short-channel effect in the DHFET results in a slightly better f_T and a decrease of output conductance that allows significant improvement of f_{max}.

The RF performances of a sub-100 nm gate length 0.08 × 50 μm² AlN/GaN DHFET on 4-inch Si have also been assessed (shown in Fig. 4). $f_T = 80$ GHz and $f_{max} = 192$ GHz have been measured at $V_{gs} = -1.5$ V and $V_{DS} = 15$ V. In spite of fairly high residual doping at the buffer/Si substrate interface resulting in RF losses of 1.5 dB/mm at 50 GHz extracted with coplanar waveguide transmission lines, excellent frequency performance has been achieved with the highest f_{max} of GaN-on-Si transistors (as illustrated in Fig. 4). This shows the high potential of this material system for mmW applications.

An active loadpull large-signal network analyzers (LSNA) up to 50 GHz [11] was used to measure RF power performances up to 40 GHz. Figure 5 depicts the on-wafer continuous-wave (CW) power sweep at 18 GHz performed on a 0.2 × 200 μm² AlN/GaN-on-Si HEMT and DHFET. At $V_{DS} = 15$ V, an output power density P_{OUT} of 1.05 W/mm with a power added efficiency (PAE) below 10% has been measured for the HEMT structure, as expected from the high drain lag effect evaluated from the pulsed measurements. On the other hand, the DHFET structure allows achieving a P_{OUT} of 3.15 W/mm and the PAE peaks above 30%, which is to the best of our knowledge the highest GaN-on-Si power density at 18 GHz with a drain bias as low as 15 V. This is due to the outstanding current density combined with a proper electron confinement.

Figure 6(a) shows the CW power measurements at 40 GHz of typical 0.1 × 50 μm² AlN/GaN-on-Si devices. An output power density of 2.5 W/mm was reached at 40 GHz when biased at 15 V which represents to our knowledge the first demonstration of high power density at 40 GHz for a GaN-on-Si transistor (as can be seen in Fig. 6(b)). The high output power results from a combination of high current density, low on-resistance, and reduced current collapse, confirmed by the dynamic load-line at $V_{DS} = 15$ V acquired with the LSNA. The PAE peaks at 18% and the linear gain is about 9 dB.

The PAE is mainly limited by self-heating as well as parasitic conduction at the buffer/Si interface causing a decrease of the power gain at 40 GHz. High power operation beyond $V_{DS} = 15$ V in these devices is essentially prevented by thermal effects since we noticed that current collapse and leakage current remain fairly low at higher biases. Part of our on-going work is focused on optimizing the Al content into the buffer layer in order to improve thermal dissipation in these devices and buffer/Si interface quality to enhance their large-signal gain at mm-wave frequencies. Indeed, 1.4 dB/mm losses at 40 GHz have been measured using standard coplanar waveguide lines. It has to be pointed out that the power measurements in Ka-band were performed under near-class A operation (500 mA/mm) with output matching

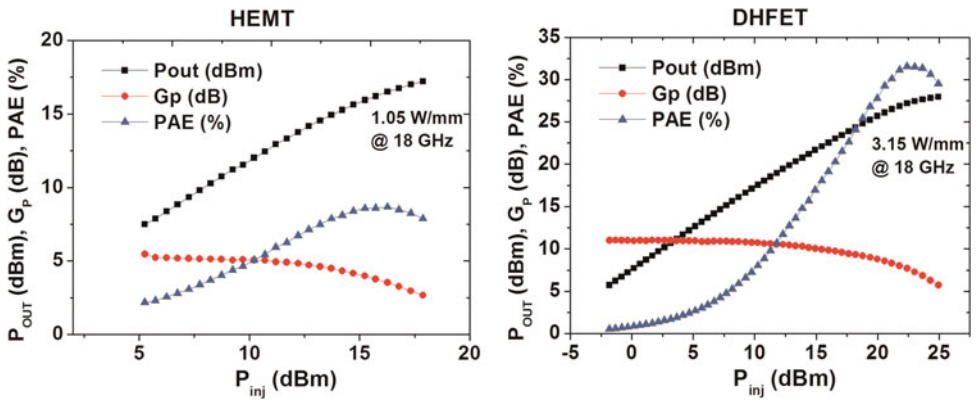


Fig. 5. CW power sweep at 18 GHz of a 0.2 × 200 μm² AlN/GaN-on-Si HEMT (left) and DHFET (right) at $V_{DS} = 15$ V.

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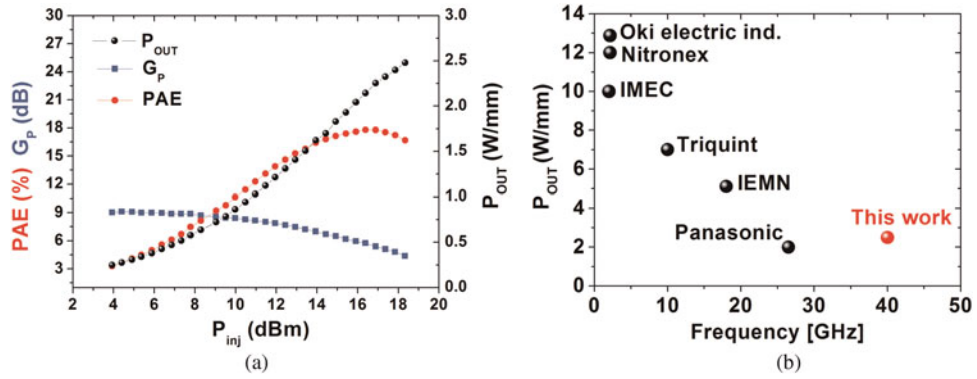


Fig. 6. (a) CW power sweep at 40 GHz of a 0.1 × 50 μm² AlN/GaN DHFET on highly resistive silicon substrate at $V_{DS} = 15$ V and $V_{GS} = -1.6$ V. (b) RF power density benchmark of GaN-on-Si transistors.

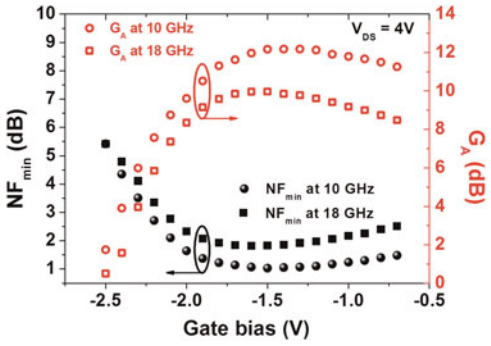


Fig. 7. Minimum-noise figure and associated gain at 10 and 18 GHz as a function of gate bias of a 0.16 × 50 μm² AlN/GaN-on-Si DHFET.

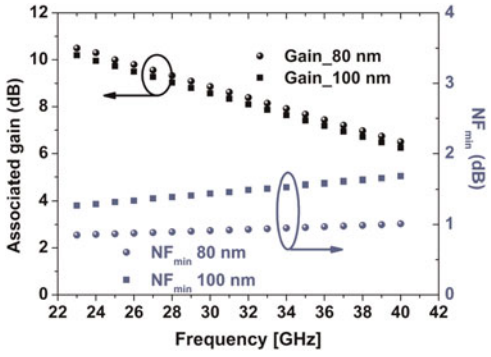


Fig. 8. Associated gain and minimum-noise figure as a function of frequency biased at $V_{GS} = -1.8$ V and $V_{DS} = 4$ V at room temperature of 100 and 80 nm AlN/GaN/AlGaN-on-Si DHFET.

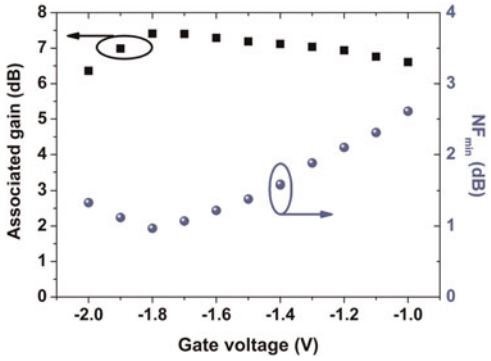


Fig. 9. Minimum-noise figure and associated gain at 36 GHz as a function of gate bias at $V_{DS} = 4$ V of an 80 nm AlN/GaN/-on-Si DHFET.

being optimized for maximum power. No improvement in PAE was observed when the devices were biased closer to pinch-off, showing the domination of RF losses at such a high frequency.

Room temperature microwave noise performance of the device has been measured at 10 and 18 GHz using the tuner method [12] that allows the extraction of fundamental noise parameters. Figure 7 shows the minimum-noise figure NF_{min} and the associated gain G_A of a 0.16 × 50 μm² AlN/GaN-on-Si transistor at $V_{DS} = 4$ V. The gate leakage current was about 0.1 μA. The device exhibits an NF_{min} of 1 and 1.8 dB with a G_A of 12 and 10 dB at 10 and 18 GHz, respectively. These data are comparable to the best reported GaN-on-Si HEMT values. It is interesting to note that the minimum noise figure corresponds systematically to the maximum G_A that may allow unique monolithic integrated circuit design.

Figure 8 shows NF_{min} and the associated gain (G_A) of a 100 nm and 80 nm AlN/GaN/AlGaN-on-Si DHFETs as a function of frequency biased at $V_{GS} = -1.8$ V and $V_{DS} = 4$ V. The gate leakage current was lower than 0.5 μA/mm under these conditions. G_A and NF_{min} scale well with gate length (L_g) owing to improved frequency performance with L_g reduction. NF_{min} reaches 1 dB (1.68 dB) at 40 GHz for $L_g = 80$ nm ($L_g = 100$ nm) with G_A remaining above 6 dB. When plotted as a function of the gate voltage, the minimum value of NF_{min} is 0.97 dB, with $G_A = 7.5$ dB, at 36 GHz (see Fig. 9). As mentioned previously the optimal NF_{min} systematically corresponds again to the maximum G_A. These datasets are the first benchmark of low noise GaN-on-Si devices in the K_a band. To the best of our knowledge, this low noise performance is the best reported so far for any GaN-based transistors at such high frequency of operation. According to Fukui's Noise figure equation [13], these results can be attributed to high frequency performance (f_t and f_{max}), low access and gate resistances in combination with a low gate leakage current [14] and low DC to RF dispersion observed in these devices as can be seen in Table 1 showing key device parameters of a 100 and 80 nm AlN/GaN/AlGaN-on-Si DHFET affecting noise performance.

C) Thermal assessment

As shown in Fig. 10, an infrared camera has been used to compare the AlN/GaN-on-Si HEMT and DHFET device temperature under high bias ($V_{DS} = 25$ V), corresponding

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Table 1. Main device parameters of a 100 nm and 80 nm AlN/GaN/AlGaN-on-Si DHFET affecting noise performance according to Fukui's Noise figure equation.

	$G_{m\ max}$ (mS/mm)	R_S (Ω .mm)	R_G (Ω)	f_t (GHz)	f_{max} (GHz)	I_{dleak} (A/mm) at $V_{GS} = -3$ V and $V_{DS} = 4$ V
$Lg = 100$ nm	565	2	0.85	95	118	8×10^{-7}
$Lg = 80$ nm	580	1.95	0.88	105	145	9×10^{-7}

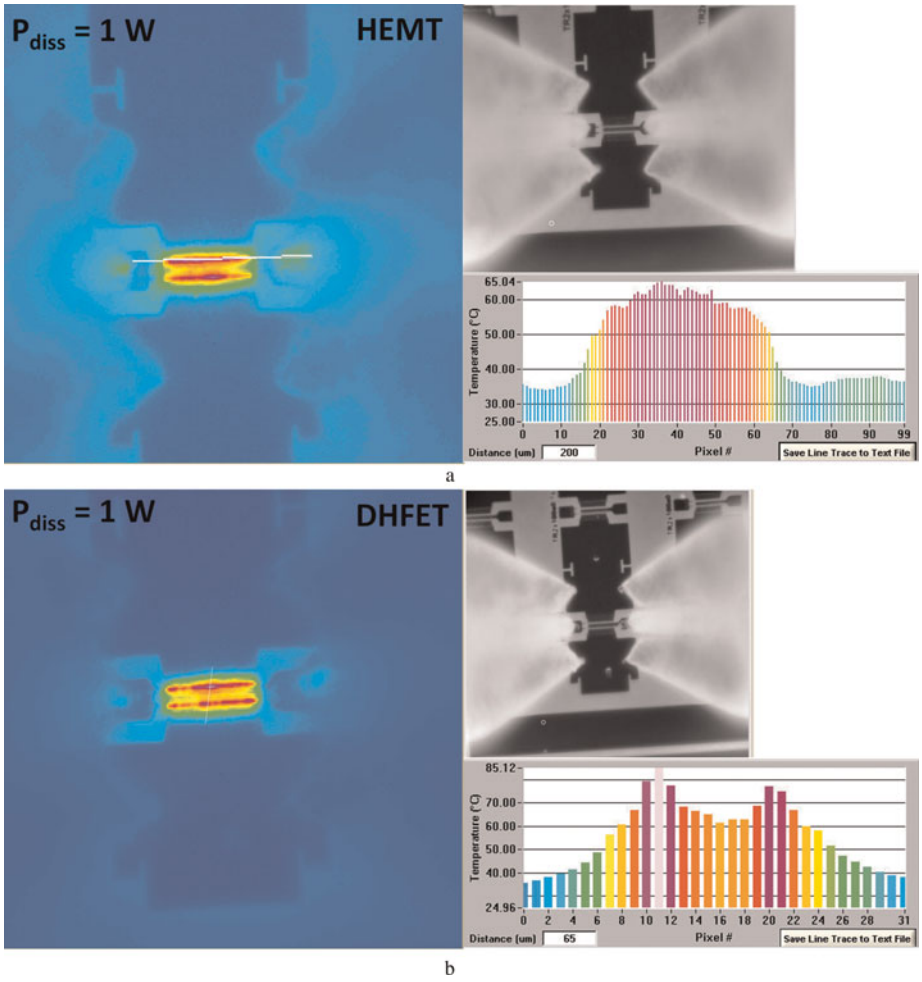


Fig. 10. Infrared camera pictures of a 2(100 μm HEMT (a) and DHFET (b) devices under bias ($P_{diss} = 1$ W). The insets show device temperature profiles.

to a dissipated power (P_{diss}) of 1 W. The device temperature profiles appear in the insets where the peak is located in the gate vicinity.

Using this set-up, the device temperature has been plotted as a function of the dissipated power for both heterostructures (Fig. 11). Similar temperatures are observed up to $P_{diss} = 0.6$ W for the HEMT and the DHFET, however, at higher drain bias a significantly higher temperature is recorded for the DHFET. This results from lower thermal dissipation of AlGaN as compared to the GaN buffer layer generating a much higher thermal resistance. Therefore, the DHFET structure is mainly limited by thermal issues under high bias ($V_{DS} > 15$ V) and thermal management needs to be performed in order to further enhance the GaN-on-Si RF device performance.

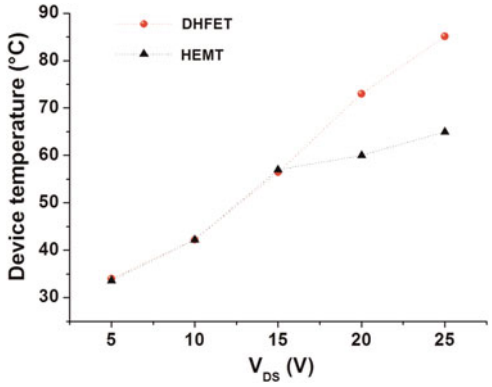


Fig. 11. 2 × 100 μm HEMT and DHFET device temperatures as a function of drain bias evaluated with an infrared camera.

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IV. CONCLUSION

We have developed an AlN/GaN/AlGaN double heterostructure that enables aggressive downscaling of GaN-on-Si devices while delivering outstanding carrier density. DC, pulsed, small and large signal measurements as well as noise assessment confirmed the benefit of the double heterostructure for such highly scaled devices. The highest AlN/GaN/AlGaN-on-Si power density has been demonstrated at 18 GHz and $V_{DS} =$ 15 V as well as the first demonstration of high RF GaN-on-Si power density at 40 GHz, thermally limited at higher bias. The lowest noise performance in the K_a band of any GaN-based transistor has been achieved with these devices Thus, the reduction of gate length and thermal management in the presented devices will allow unprecedented GaN-on-Si millimeter wave performances.

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Damien Ducatteau received an engineer degree from the University of Lille 1 in 1996 and the Ph.D degree in electronics at the Institut d'Electronique, de Microélectronique et de Nanotechnologie (IEMN) Laboratory, Villeneuve d'Ascq, France in 2008.

In 1997, during four years, he has been involved with the European Space Agency (ESA) within ROSETTA project, during which he has been developing the RF electronic part and the radar test procedures of the CONSERT instrument. In 2001, he joined IEMN where he has been in charge of the microwave and non linear test characterization of AlGaN/GaN HEMT devices for the common Laboratory between IEMN and THALES III–V Labs. His research activities concern the power behavior of electronic devices and he is mainly involved with the nonlinear characterization at high frequencies. Since 2006, he is the Head of the technical team that has in charge the common microwave facilities of IEMN.



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