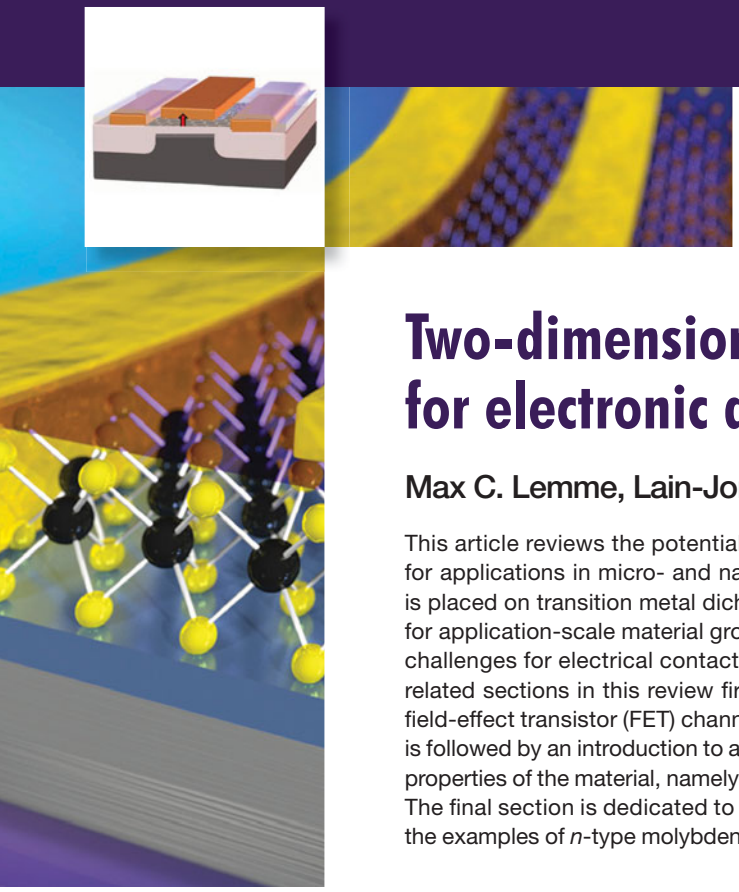


Two-dimensional materials for electronic applications

Max C. Lemme, Lain-Jong Li, Tomás Palacios, and Frank Schwierz

This article reviews the potential of graphene and related two-dimensional (2D) materials for applications in micro- and nanoelectronics. In addition to graphene, special emphasis is placed on transition metal dichalcogenides (TMDs). First, we discuss potential solutions for application-scale material growth, in particular chemical vapor deposition. We describe challenges for electrical contacts and dielectric interfaces with 2D materials. The device-related sections in this review first weigh the pros and cons of semi-metal graphene as a field-effect transistor (FET) channel material for logic and radio frequency applications. This is followed by an introduction to alternate graphene switch concepts that utilize the particular properties of the material, namely tunnel FETs, vertical devices, and bilayer pseudospin FETs. The final section is dedicated to semiconducting TMDs and their integration in FETs using the examples of *n*-type molybdenum disulfide (MoS_2) and *p*-type tungsten diselenide (WSe_2).

Introduction

The experimental demonstration of the isolation of graphene and a study of its properties in 2004 by Novoselov et al. and Berger et al. triggered tremendous worldwide scientific interest and activity on this material over the past decade.[1,2] This prototype two-dimensional (2D) material is made of carbon atoms in a hexagonal structure and displays extraordinary intrinsic properties relevant to microelectronic,[3] optoelectronic,[4] and nanoelectromechanical systems (NEMS)[5] applications (see the *MRS Bulletin* special issue on graphene, December 2012). These include high carrier mobility,[6] high current density,[7] broadband optical absorption,[8] tensile strength in excess of 1 TPa,[9] and high thermal conductivity.[10] In addition, graphene is largely compatible with current semiconductor technology, so it can be easily co-integrated with silicon devices.[11] Particular promise is seen for integration at the back end of the line, where graphene could provide added functionality to the existing complementary metal oxide semiconductor (CMOS) platform.

The most notable disadvantage of graphene is the absence of an electronic bandgap, which limits its applicability as a transistor channel material. Here, other 2D materials may step in, in particular semiconducting transition metal dichalcogenides (TMDs) with the composition MX_2 (M = Mo or W; X = S, Se, or Te, **Figure 1**). Single layers of TMDs are only three atoms thick and extremely flexible and transparent. Depending on their actual composition, the bandgap of TMDs varies from metallic to those of wide bandgap semiconductors such as *n*-type MoS_2 (bandgap energy E_g ~ 1.8–2.4 eV).[12,13] Phosphorene, another single layer 2D material exfoliated from black phosphorus crystals, has been found to perform well as the channel material in *p*-type transistors. Preliminary results show that the hole mobility is thickness dependent, with reported values up to 300 ~ 1000 cm^2/Vs.[14,15] All 2D materials share issues of high contact resistance and channel mobility reduction due to dielectric interfaces. Fundamental concerns about the former have been somewhat eased by several recent reports of low resistance contacts.[16,17] For the latter, another 2D material may come to the rescue, as insulating hexagonal boron nitride (h-BN) dielectrics show weak interaction with graphene and help maintain intrinsic properties.[18] This article reviews fabrication methods for graphene and 2D materials, describes challenges in contacting these materials electrically, and discusses the potential for their application as transistors.

Material synthesis and fabrication technology

Growth

Upon its conclusive experimental discovery, graphene was mechanically exfoliated—or peeled—from graphite crystals.[1] While this method still yields the highest graphene quality

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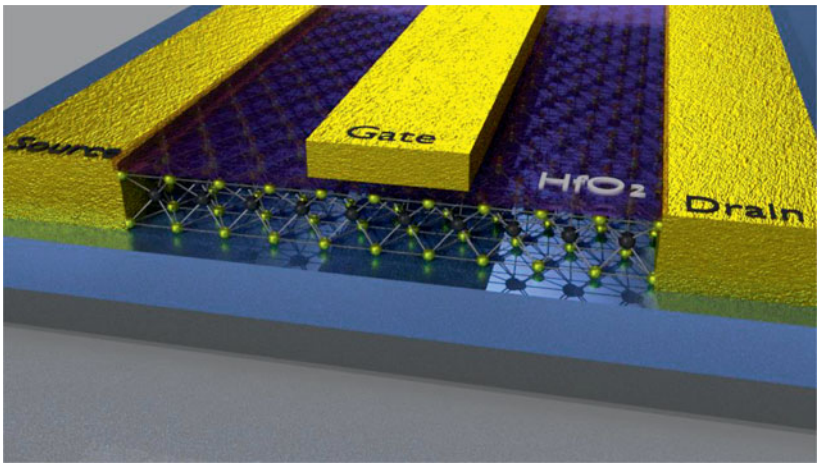


Figure 1. Schematic representation of a field-effect transistor with a transition metal dichalcogenides channel. Black spheres represent metal atoms, while yellow spheres represent sulfur, selenium, or tellurium.

today, it is limited to flakes of random thickness, size, and uniformity. Epitaxial graphene can be grown on a large scale by thermal decomposition of silicon carbide (SiC).[2] Graphene grown by this method exhibits good electronic properties and is suitable for monolithic graphene devices on SiC substrates. Limitations of this method include a lack of suitable transfer methods, high process temperatures, and high cost of SiC substrates with limited size scalability.

In contrast, chemical vapor deposition (CVD) has a high potential for large-scale production of graphene and may be viewed as a pathway for graphene commercialization.[19–21] The main steps of CVD graphene growth are the decomposition of hydrocarbons such as methane (CH_4) and the subsequent formation of graphene on catalytic surfaces that lower the energy barrier of the chemical reactions. These catalytic conditions are mostly satisfied by transition metals such as Cu, Ni, Pt, Pd, Rh, Fe, or Co.[22] The specific growth mechanism is determined by the solid solubility of carbon in the catalyst. If the solubility is negligible at the growth temperature, as in Cu at up to 1000°C, graphene forms at the surface, and growth is quasi self-limited as the growing graphene film prevents further carbon atoms from reaching the catalytic surface. If the solubility is substantial, as in Ni, carbon atoms diffuse into the bulk of the transition metal and precipitate to the surface during cooling. Uniformity and thickness control are more difficult in such a diffusion-precipitation dominated process compared to the surface diffusion limited process on Cu. Therefore, and because of the wide availability and low cost, Cu is the mostly used catalyst for CVD graphene growth today.

The necessity of large-area growth processes is obviously identical for TMD layers. Recent advances in the growth of highly crystalline MoS_2 monolayer flakes of up to few tens or hundreds of micrometers by the gas phase reaction between molybdenum oxides and sulfur powders[23,24] have shed light on the large-area preparation of other TMD monolayer materials such as WSe_2.[25] However, the wafer-scale growth of high-quality TMD layers remains an important issue to be solved.

In addition to high-quality CVD growth, industrial scale transfer methods for graphene and TMDs from the catalytic growth materials to the desired substrates will be a key aspect for future applications. Most approaches rely on the use of polymers as transfer layers,[26] and TV-screen-size graphene with 65 cm diagonals[27] as well as 100 m long rolls of graphene[28] have been produced in roll to roll processes. Very recently, graphene growth on germanium substrates has been demonstrated up to the wafer scale,[29–31] but this method also relies on subsequent transfer. Nevertheless, this option may be an important step to avoid contamination issues with catalytic metal residues. In general, progress in the growth and—if needed—in the transfer of large-area graphene is rapid and essential for its future commercialization.

Electrical contacts

High access resistance limits the extrinsic performance of electronic devices of any type, no matter how good the intrinsic performance. The formation of low resistivity ohmic contacts between 2D monolayers and metals therefore is one of the key challenges in device engineering. Two-dimensional materials are only one or a few monolayers thick. Their Fermi energy is therefore extremely sensitive to the underlying substrate and the environment, and the realization of ohmic contacts depends strongly on their Fermi level. Along these lines, device measurements supported by *ab initio* density functional theory indicate that the d-orbitals of the contact metals play a huge role in forming low ohmic contact resistance with the 2D monolayer. For example, lower work function metals such as Ni and Au show ohmic contact behavior to *n*-doped MoS_2, while higher work function Pd contacts show Schottky behavior.[32]

The high contact resistance (R_C) seen in metal-graphene contacts typically arises due to the low density of states (DOS) available in the graphene under the contact and the metal—graphene coupling plays a significant role in increasing contact resistance.[33–36] Various studies have been carried out to increase the transmission from the contact metal into the graphene by using metals with a large work function difference, compared to graphene, to heavily dope the graphene under the metal to increase the DOS and reduce R_C.[35,37] Thermal annealing and ozone treatments also help in reducing the contact resistance,[38–40] as does a double contact geometry with contact metals above and below the graphene layers, which reduces the contact resistance by 40%.[41] Theoretical work suggests that graphene contacted just at its edges will result in reduced R_C,[42] and this was experimentally confirmed

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by Smith et al., who formed cuts in the graphene within the contact region.[43] Following this idea, Leong et al. employed a metal-catalyzed etching process, which resulted in multiple nano-sized pits with zigzag edges under the metal.[16] The resulting contact resistance was as low as 100 Ωμm in single-layer graphene and 11 Ωμm in bilayer graphene, which is lower than the required value for silicon MOSFET technology at the 22 nm node.[44] Moon et al. also demonstrated metal-graphene contact resistance below 100 Ωμm.[17] Here, a Ti/Pt/Au stack was thermally evaporated to form metal contacts with the graphene. In summary, even though low contact resistance to graphene has been achieved occasionally, a reliable standard contact technology for 2D materials has yet to be developed.

Graphene field-effect transistors

Digital electronics

Current digital electronics is dominated by the silicon metal oxide semiconductor field-effect transistor (MOSFET) arranged in CMOS circuits, which contain up to several billions of individual transistors. Key to proper CMOS operation is that these transistors show excellent switching behavior with a large ratio of on-state to off-state current (I_{on}/I_{off}), typically between 10^4 and 10^7. It is important to recognize that such I_{on}/I_{off} ratios can only be achieved if the transistor channel is semiconducting with a wide enough bandgap of at least 400 to 500 meV. Since large-area graphene is gapless, conventional graphene MOSFETs (GFETs) with large-area channels do not switch off properly. They typically show I_{on}/I_{off} ratios of only 2–10, which is not sufficient for complex logic circuits. Nevertheless, there are several options to enable graphene transistor logic, including (1) opening a bandgap by using graphene nanoribbons (GNRs) for the channel, (2) using two graphene layers (bilayer) and applying a vertical electric field, and (3) introducing graphene transistors with fundamentally different operating principles that do not rely on a bandgap for switching.

In extremely narrow GNRs of 5 nm width or less, a bandgap of several hundred meV opens due to quantum confinement, and MOSFETs with GNR channels and I_{on}/I_{off} ratios exceeding 10^6 have been demonstrated.[45] The fabrication of such GNRs, however, presents serious processing challenges today, because different crystal orientations, line edge roughness, and random edge termination will lead to different electronic properties for individual GNRs and therefore to intolerable device variability. Moreover, the carrier mobility decreases dramatically with GNR width. Thus, while GNRs may achieve the I_{on}/I_{off} ratios required for logic circuits, one of the biggest advantages of graphene compared to silicon, the ultrahigh carrier mobility, is lost.

Bilayer graphene FETs may exhibit a transport gap if a vertical electric field is applied across the two layers. This may be done with an actual bias in a double gate structure, or via chemical or electrostatic doping. In this way, a small bandgap of up to 250 meV may be achieved.[46] While this gap is most likely not sufficient for logic operation, it may have merits for radio frequency (RF) devices or tunnel FETs (see below). Graphene transistors with non-MOSFET operation principles (i.e., related to option 3) will be discussed later.

RF electronics

In contrast to FETs for digital electronics, FETs for RF applications do not need to switch off, which makes gapless graphene a strong contender in this field.[47] RF FETs are typically in the on-state biased, and a small RF signal (the signal that is to be amplified) is fed into the transistor input. The ability of a transistor to amplify RF signals is described by the current gain h_{21} and the power gain, which both degrade with increasing frequency. The most frequently used RF transistor figures of merit are the cutoff frequency f_T (the frequency at which the magnitude of h_{21} has dropped to unity [i.e., 0 dB]) and the maximum frequency of oscillation f_{max} (the frequency at which the unilateral power gain U equals unity). It should be noted that for most RF applications, power gain and f_{max} are more important than current gain and f_T.

The first GFET with a cutoff frequency f_T in the GHz range was reported in late 2008,[48] and since then, the RF performance of GFETs has been improved continuously. **Figure 2**

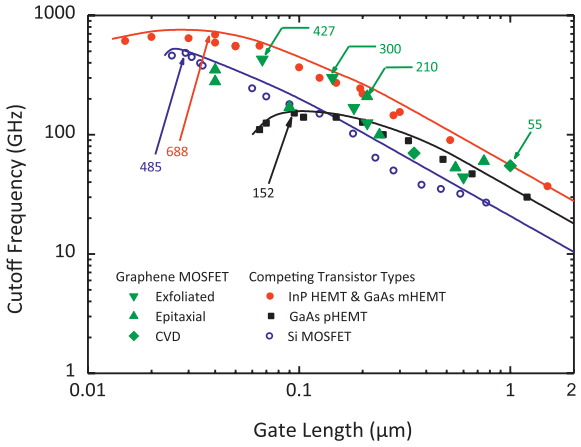


Figure 2. Cutoff frequency f_T of graphene metal oxide semiconductor field-effect transistors (MOSFETs) versus gate length L. Also shown is the f_T performance of three classes of conventional radio frequency (RF) FETs: (1) InP HEMTs (high electron mobility transistors) and GaAs mHEMTs (metamorphic HEMTs), (2) GaAs pHEMTs (pseudomorphic HEMTs), and (3) Si MOSFETs. The numbers indicate f_T in GHz. The solid lines are a guide to the eye and represent the current upper f_T limit for the three competing transistor types. For transistors with long gates (L > 200 nm), the cutoff frequencies of the different transistor types is roughly proportional to L^{-1} (L is the gate length). Here, the intrinsic device (i.e., the channel) governs the RF performance, and the channel mobility is very important (e.g., Si MOSFETs show the lowest channel mobility and the lowest cutoff frequency of the transistor types shown). For shorter gates, the shape of the f_T curves deviates from the L^{-1} dependence. In short-gate transistors, the external device part, parasitics, and short-channel effects become relevant, while the role of the mobility gradually declines. Based on information from References 53 and 106. Note: CVD, chemical vapor deposition.

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compares the cutoff frequencies of the best GFETs reported to date with the f_T performance of competing materials and technologies. GFETs compete extremely well down to about a 100 nm gate length with InP high-electron-mobility transistors (HEMTs) and GaAs metamorphic HEMTs, which are state-of-the-art technology. The current record is a 67-nm-gate GFET with an intrinsic f_T after de-embedding parasitic capacitances of 427 GHz.[49]

In contrast to their impressive f_T performance, GFETs behave rather poorly in terms of the maximum frequency of oscillation f_{max}. The highest f_{max} data reported so far for GFETs is in the range of 40–105 GHz,[50–52] compared to several hundreds of GHz for the competing FET types (**Figure 3**). The reason for the relatively low f_{max} of GFETs lies in a weak saturation of the drain current of the DC output characteristics, possibly combined with high source/drain series and gate resistances.[53] The poor drain current saturation is a consequence of the gapless nature of graphene, and a theoretical study concluded that a moderate bandgap of approximately 100 meV would greatly improve matters.[54] As mentioned previously, that kind of bandgap can be achieved by using bilayer GFETs. This was confirmed in a recent experiment that showed improved current saturation in bilayer GFETs.[55] Based on these results, it has been predicted that bilayer GFETs may compete or outperform state-of-the-art RF technology in terms of f_{max}, if the contact resistance issue is resolved.[56]

In addition to discrete GFETs, integrated graphene RF circuits have been reported that utilize the ambipolar behavior of GFETs to replace more complicated silicon MOSFET circuits. Examples include frequency doublers,[57] mixers,[58] and even an integrated three-stage receiver circuit for operation around 4 GHz, consisting of only three graphene MOSFETs and eight passive elements.[59] A striking feature of the receiver

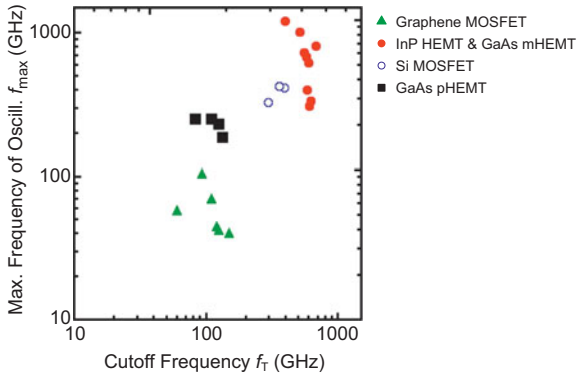


Figure 3. Maximum frequency of oscillation f_{max} versus cutoff frequency f_T of graphene metal oxide semiconductor field-effect transistors (MOSFETs) and competing radio frequency (RF) FETs. It can be seen that the high cutoff frequencies of GFETs do not translate into high f_{max}. The main reasons for this behavior are the unsatisfying drain current saturation in GFETs and the resulting high drain conductance g_{ds}. Based on information from Reference 107. Note: HEMT, high electron mobility transistor; mHEMT, metamorphic HEMT; pHEMT, pseudomorphic HEMT.

circuit is that it has been fabricated in a silicon fabrication line with a silicon CMOS compatible process. The interest in GFETs for RF applications has manifested in increasing work toward transistor models that can be used in circuit design.[60–62]

Alternative graphene switches

Tunneling field-effect transistors

An interesting option for graphene logic transistors is the concept of the tunnel MOSFET (TFET). In TFETs, the gate voltage controls the band-to-band tunneling across the source-channel junction instead of the carrier concentration in the channel as in conventional MOSFETs. This operating principle allows steeper subthreshold swings below the 60 mV/dec limit of conventional MOSFETs and potentially lower power consumption of TFET circuits. Si and III–V TFETs are currently intensively investigated, and experimental devices have been presented.[63] Since a precondition for proper TFET operation is a semiconducting channel, either GNRs or bilayer graphene must be used for graphene TFETs. Experimental graphene TFETs have not been realized yet, but their potential has been investigated by device simulations.[64–66] While GNRTFETs suffer from the same problems as conventional GNR MOSFETs (narrow ribbons needed, edge roughness effects), the bilayer graphene TFET shows promise since narrow ribbons are not needed; the limited gap opening should be sufficient to enable safe switch-off; and high on-off ratios may be possible thanks to the subthreshold swing below 60 mV/dec.[64] TMD-based FETs have also been suggested for TFETs,[67] and the wide variety of material options seems to be an optimal precondition for future experiments.

Vertical devices

Vertical devices based on graphene and 2D materials, including Schottky barrier devices such as the "Barristor,"[68] have received considerable attention lately.[69] One such candidate, a graphene-based hot electron transistor, has been proposed conceptually by Mehr et al.[70] and later demonstrated in experiments.[71,72] Here, a graphene sheet is sandwiched between two insulators, with metals or doped semiconductors on both sides (**Figure 4**a). Carrier transport is vertical and happens by way of quantum mechanical tunneling. In such a device, the base contact is made up of graphene, hence the name graphene base transistor or GBT. The combination of high electrical conductivity and extreme thinness of the graphene leads to high transmission of charge carriers. When a voltage is applied to the graphene base, the current can be modulated by several orders of magnitude (Figure 4b). This happens because the graphene base potential modulates the tunneling barrier between the emitter and the base. Above a certain threshold, charge carriers may tunnel via the Fowler Nordheim mechanism and reach the collector by ballistic transport (Figure 4c). Other vertical 2D devices under consideration include resonant tunneling structures[73] and devices utilizing

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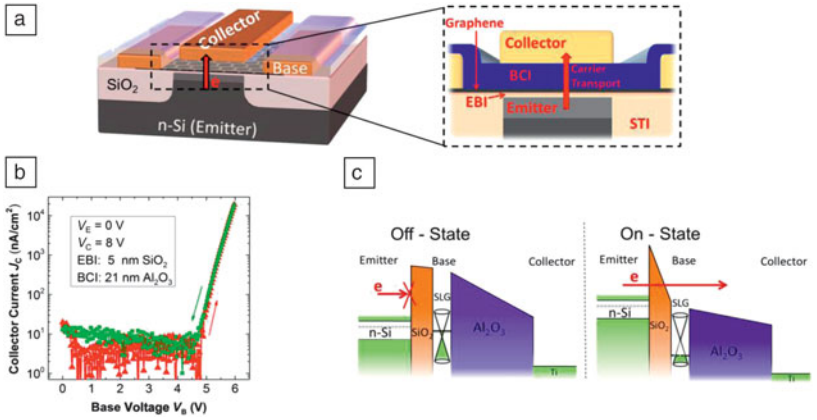


Figure 4. (a) Schematic of a graphene base hot electron transistor. (b) Measured transfer characteristics with an on/off current ration of over 10^4. (c) Schematic of the band structure of a graphene base transistor. Vertical tunneling based transistors with a graphene base achieve high on-off current ratios and can therefore be used as electronic switches. In addition, graphene base transistors have the potential for high operating speeds.[70,71] Note: EBI, emitter base insulator; STI, shallow trench isolation; V_E, emitter voltage; V_C, collector voltage; SLG, single layer graphene. Adapted from Reference 71.

the intrinsic symmetry in the graphene band structure and are hence named SymFET.[74]

BiSFETs

One of the most striking—but not yet experimentally verified—device concepts based on 2D materials is the bilayer pseudospin FET (BiSFET). Pioneering theoretical work by MacDonald and Banerjee has predicted that electron–hole pair condensation in two closely spaced graphene layers may occur at room temperature,[75] which could be utilized as a new low power switching device.[76] The basic BiSFET structure consists of two graphene layers separated by an interlayer dielectric that is thin in the region where condensation ought to occur and thicker in the rest of the device (**Figure 5**). By applying two opposite gate voltages V_{Gp} and V_{Gn}, *p*-type conduction is achieved in one layer, and *n*-type conduction is achieved in the other layer. Due to their opposite charges, the holes in the *p*-type layer interact with the electrons in the *n*-type layer due to Coulomb forces across the thin interlayer dielectric. If this interaction is strong enough, holes and electrons will bind into excitons, and if this happens to a large extent, an exciton condensate forms,[75,77] which does not require precise alignment of the two graphene layers. If a low voltage V_{pn} is applied across the contacts of the graphene layers, a collective tunneling process sets in and results in a tunneling current I_{pn}. Note that this collective tunneling is different from the conventional single-particle tunneling. At slightly higher V_{pn}—but still below the thermal voltage V_T (25 mV at room temperature)—the condensate is predicted to collapse, and the collective tunneling current drops to zero.[76] Thus, within a very small voltage range, the BiSFET is expected to show clearly distinguishable on- and off-states. This is a requirement for a switch in digital logic, and BiSFET-based logic gates such as inverters, NAND, and NOR could operate at much smaller voltage levels compared to CMOS logic, enabling ultralow power consumption.[76,78] For this reason, the BiSFET has been included in the "International Technology Roadmap for Semiconductors."[44]

One concern with the BiSFET is the critical temperature up to which exciton condensation occurs. So far, condensation has been observed only in III–V semiconductor structures at very low temperatures. In graphene, theoretical studies estimate a range for the critical temperature from a few mK to above 300 K, depending on structures and assumptions made during simulations,[79–82] even though a slightly different structure from Figure 5 may be required for room-temperature operation.[83] Another open question is whether the switching occurs at voltage levels around V_T, as stated in References 76 and 78 or if higher voltages are needed.[84,85]

Two recent theoretical studies compare the performance of BiSFETs to that of 15-nm silicon CMOS logic.[86,87] Due to different assumptions, the outcomes of these studies are quite different. In one study, sub-V_T switching and the initial BISFET design have been assumed, and a clear advantage of BiSFET logic in terms of the energy consumption × delay time product has been obtained, while CMOS showed a slight edge with regard to chip area.[86] In the other study, on the other hand, a supply voltage of 0.6 V (i.e., much higher than in Reference 86 but still lower compared to 15-nm CMOS) and a modified BiSFET design have been assumed, resulting in a BiSFET performance

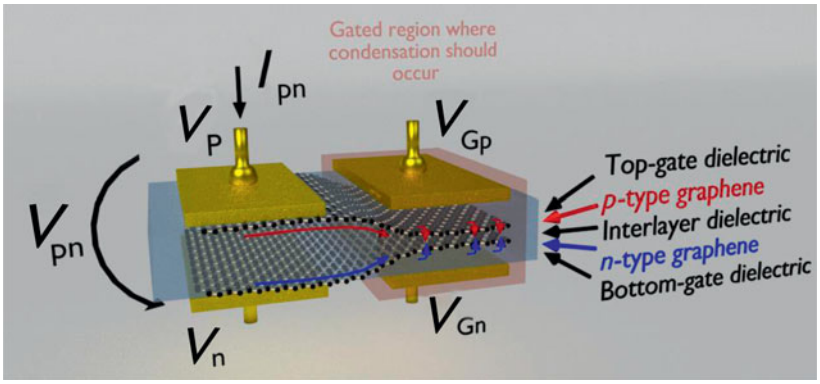


Figure 5. Schematic of a bilayer pseudospin field-effect transistor as described in Reference 76. Condensation and collective tunneling are expected to occur on the right side of the device. Note: V_{pn}, voltage across the two graphene layers; V_p, potential of *p*-type graphene layer; V_n, potential of *n*-type graphene layer; I_{pn}, tunneling current; V_{Gp}, gate voltage for *p*-type graphene layer; V_{Gn}, gate voltage for *n*-type graphene layer.

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that is worse compared to Si CMOS in terms of energy consumption, delay time, and chip area.[87]

In conclusion, the BiSFET is a very attractive device concept in theory, but so far, its operation has not been confirmed experimentally. Other 2D materials may also be of interest for BiSFETs, including silicene and germanene, the silicon- and germanium-based counterparts of graphene, and the semiconducting single-layer TMDs. Experimental data will be required to obtain reliable information on the merits and drawbacks of BiSFETs and to optimize materials and designs for this device.

Semiconducting 2D FETs

In spite of graphene's unique properties and the promising device results described earlier in this article, many electronic applications, such as digital CMOS circuits, require the use of semiconductors with a sizeable bandgap. Thus, the identification and characterization of suitable semiconducting 2D layers from the vast material pool is urgent and a great challenge. Following the Scotch tape method of exfoliating graphene monolayers,[1] high-quality 2D monolayers have been mechanically exfoliated,[88] which are ideal for the demonstration of low-dimensional physics and high-performance devices.

Molybdenum disulfide (MoS_2) monolayers, a TMD with a direct bandgap of 1.8 eV, have been demonstrated as the channel material in *n*-type FETs with fairly high electron mobility (~200 cm^2/Vs), excellent I_{on}/I_{off} ratio (~10^8), and low subthreshold swing (~74 mV/dec).[89] Proof-of-concept MoS_2-integrated circuits such as inverters, NAND gates, static random access memory (RAM), and a five-stage ring oscillator have also been demonstrated.[90] Addressing the issue of scalability, high-performance MoS_2 circuits on large-area chemical vapor deposited MoS_2 were demonstrated.[91] Although MoS_2 normally shows *n*-doped characteristics likely caused by the presence of S-vacancies in the structure, both enhancement-mode and depletion-mode transistors can be fabricated by the use of gate metals with different work functions.[90] Ideally, *p*-type TMD monolayers would complement MoS_2 for digital logic applications. One option is *p*-channel FETs based on monolayer tungsten diselenide (WSe_2), which exhibit a fairly high effective hole mobility of ~250 cm^2/Vs, a perfect subthreshold swing of ~60 mV/dec, and an I_{on}/I_{off} ratio of >10^6 at room temperature.[92]

The carrier mobility demonstrated in TMDs is not higher than that of silicon. Nevertheless, there may be substantial merit, because thin channel materials typically improve the scale length of FETs,[93] leading to better gate length scalability. In ultrathin silicon below 5 nm thickness, the carrier mobility is greatly reduced compared to conventional silicon FETs, most likely well below that of TMDs.[94,95] Furthermore, some of the first applications being pursued for TMD FETs are in the field of large-area, flexible electronics. Some examples include the back-plane electronics of large displays, and chemical and biological sensors. Again, the mobility is larger than in other competing materials in these applications, such as organic semiconductors and amorphous silicon. Transparent electronics is another research direction in the TMD devices field. For this, TMD channel materials are combined with graphene electrodes and BN dielectrics for all-transparent systems that take advantage of the limited optical absorption of few-atom-thick materials.[96,97]

Summary

Graphene and other 2D materials have a number of intrinsic material properties that make them attractive candidates for micro- and nanoelectronic devices. In this review, we have focused on applications such as electronic switches for logic and transistors for radio frequency applications. However, in order to fully exploit their exceptional properties, several challenges need to be overcome first. Reliable, industry scale material growth methods compatible with existing semiconductor technology have to become available, along with suitable transfer methods to the desired substrates, if needed. Furthermore, the 2D layers have to be adequately connected to the surrounding (complementary metal oxide semiconductor) technology, in particular with respect to ohmic contacts and dielectric interfaces. These challenges are currently being addressed by a large number of device engineers and physicists worldwide, and progress is rapid and substantial. Moreover, there is great potential for applications in optoelectronics,[4,98–101] nanoelectromechanical systems,[5,102,103] or chemical- and biosensors[104,105] that are beyond the scope of this review. It will be exciting to witness the future development of 2D materials, technology, devices, and circuits.

Acknowledgments

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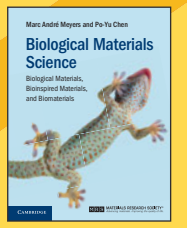
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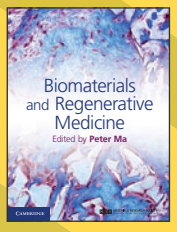
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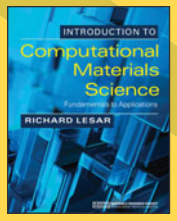
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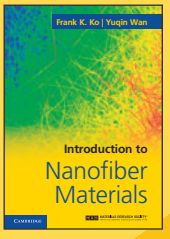
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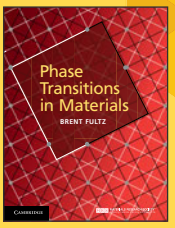
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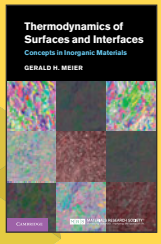
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