A METHOD INTEGRATING OPTIMAL ALGORITHM AND FEM ON CMOS RESIDUAL STRESS

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ABSTRACT

Residual stress in MEMS is of inherent importance in various respects. This study proposes a specific method using ANSYS including the birth and death method and combined with the optimal method (SCGM) to reduce the residual stresses during the CMOS fabrication process. The suitable cooling temperature for decreasing the residual stress is proposed and available. It demonstrates that the suitable parameter on the fabrication can reduce the residual stress in MEMS devices without any extra manufacturing process or external apparatus. The proposed method can expand to simulate the realistic MEMS model effectively.

Keywords: Optimization, Residual stress, CMOS fabrication, SCGM.

1. INTRODUCTION

The residual stress essentially reduces the structural integrity and longevity of MEMS devices. During the CMOS fabrication process, residual stress is generated from the thermal mismatch resulted from the thin film deposited process. Many studies propose that the residual stress of the thin films is an important key on the reliability of film/substrate systems [1,2].

The finite element analysis (FEA) has to be utilized in order to consider the nonlinear deformations and evaluate the layer deposition on deformed substrates. The stress of the deformed multilayer has to be simulated with the birth and death method in ANSYS. It can be used to simulate in manufacturing process [3], welding process [4]. The numerical design approach uses a direct problem solver, ANSYS code, combined with an optimization method (the simplified conjugate gradient method, SCGM [5]) to minimize the residual stress of the thin film generated from the CMOS fabrication process.

2. RESIDUAL STRESS IN CMOS FABRICATION

Residual stress includes the quenching stress and thermal stress. The quenching stress is due to the rapid contraction of the deposited layer cooled from

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operating temperature to substrate temperature. The magnitude of quenching stress can be estimated [6]:

$$\sigma_q = \alpha_c (T_m - T_s) E_c \quad (1)$$

where α_c, E_c, T_m, and T_s are coefficient of thermal expansion (CTE), elastic modulus, melting point of the deposited material and substrate temperature, respectively.

The thermal stress induces by the mismatch in CTE of the substrate and deposited materials. Thermal stress at the interface can be estimated:

$$\sigma_{tc} \approx E_c \, \Delta\alpha \Delta T \frac{1+\nu}{1-\nu^2} \quad (2)$$

where $\Delta\alpha$, ΔT and v are the CTE mismatch between the substrate and deposition layers, the temperature drop in the cooling and the Poisson's ratio, respectively

The overall magnitude of residual stress in CMOS fabrication is the summation of quenching stress and thermal stress.

$$\sigma_{\text{residual}} = \sigma_q + \sigma_{tc} \quad (3)$$

3. NUMERICAL ANALYSIS AND MODELING

The CMOS cross-section schematic diagram is presented in Fig. 1. Thin film deposition in micro — system technology occurs normally on thicker substrates (typically: 400μm to 675μm).

To evaluate the residual stress distribution within CMOS fabrication, a finite element model, PLANE13 for ANSYS, is used and combined the coupled heat transfer and elastic — plastic finite element stress analyses. The detail material characteristics of each layer in CMOS process are given in Tables 1 and 2 [7].

Stressless layers deposited on already deformed multilayer have to be simulated with the so called "birth and death" method. Birth and death method is special method in ANSYS. It can be used to simulate in manufacturing process, welding process and especially in coating. Specifically for the thin film deposition, the death and birth method causes the free and reactionless (death) entrainment of layers deposited later on. The free and reactionless movement of layer — elements can be switched into a mechanically active status (birth) at the simulation step where the layer should be deposited. Actually, the multilayer film of CMOS is modeled in the initialization. The death and birth method is used to active each layer as the manufacturing process. For "death" elements: Initial properties are the same as the substrate material, *e.g.* switched to low Young's modulus, E = 0+ and density ρ, but high yield strength, σ_y at the end of the predicted time for etching. And for "birth" elements: The assigned material properties, *e.g.* the Young's modulus, density and yield strength are switched in the reverse order as in the case of "death" elements at the end of the deposition process.

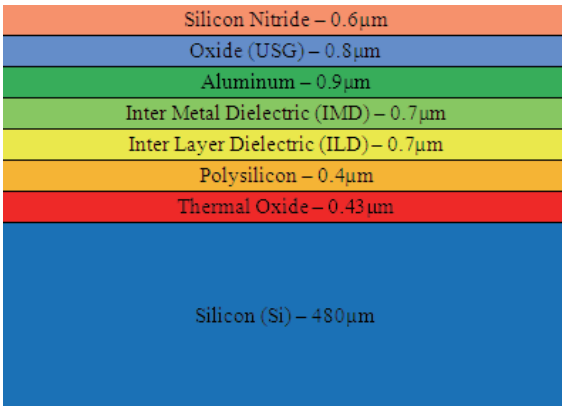


Fig. 1 Simplified cross-section of CMOS

Table 1 Physical properties [7]

Material	Young's modulus (MPa)	Poison ratio	CTE (K^{-1})	Free — stress temperature (K)
Silicon	129E3	0.28	2.62E–6	298
Thermal oxide (FOX)	72E3	0.2	0.5E–6	1253
Polysilicon (P2)	169E3	0.22	2.3E–6	893
ILD	80E3	0.2	1.1E–6	1123
IMD	60E3	0.25	1.37E–6	673
Al (M2)	*Non - linear*	0.33	26E–6	773
Oxide (OX)	60E3	0.25	1.37E–6	673
S_iN	210E3	0.27	2E–6	673

Table 2 Thermal properties [7]

Material	Density kg/m^3	Specific heat capacity J/(kg · K)	Thermal conductivity W/(m · K)
Silicon	2329	700	130
Thermal oxide (FOX)	2200	730	1.4
Polysilicon (P2)	2320	678	34
ILD	2320	678	34
IMD	3965	730	35
Al (M2)	2700	904	237
Oxide (OX)	3965	730	35
S_iN	3100	700	20

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A symmetric model is employed, and the displacement $U_x = 0$ along the line of the symmetry, $U_x = 0$, $U_y = 0$ at the bottom nodes to prevent a rigid body motion. Figure 2 shows the deposition parameters about the simplified CMOS fabrication. Convection to the surrounding environment is used as thermal boundary condition.

4. VALIDATED MODEL

In this study, we use the experimental results and previous COMSOL numerical study to validate our numerical methodology in ANSYS. First, a 2P2M bridge structure with length of bridge $L = 130\mu m$ [8] is built for the validation. The test structure is fabricated by Macronix International Co. (MXIC) standard 0.5μm 2P2M process. We use the scanning electron microscope (SEM) system to measure the pre-deformation after the 2P2M bridge structure released residual stress. The deformation curve of the bridge structure is obtained from the SEM picture analysis. The image analysis method is described in Fig. a with x — location follows the length of the bridge structure and y — height of gap g in detail.

The experiment measures the deformation at 9 specific positions by using the SEM picture analysis method (Fig. 3). The deformation's curvature of the 2P2M bridge structure ($L = 130\mu m$) in experiment and numerical ANSYS simulation are shown in Fig. 4. Through this figure, the 2P2M bridge structure is bending down and the maximum deformation value is 0.136μm in experiment. In the simulation, the bridge is also bending down and the maximum deformation value is 0.111μm at the same position in experiment. The shape of curvature is a parabolic. It finds that the simulation result agree well with experimental data. The deviation is also calculated. The average deviation is 3.58%.

Next, a validated case compared with the previous study [9] is designed to explore the correctness of the proposed method of this study. The coating process is simulated by COMSOL in the previous study [9]. This device consists of two layers (SiO_2 and Aluminum) deposited on the silicon substrate with different temperature deposition. The thickness is 20μm (substrate), 1μm (SiO_2), and 1μm (Al), separately. At first, the silicon plate is heated up to 900°C as the thermally grown of silicon oxide (SiO2) occurs. Afterwards the two layers are cooled to room temperature. Second, the temperature adjusts to 400°C, the deposition of 1 μm aluminum (Al, third step) occurs on the curved surface. Finally, the three layered stack is cooled down to room temperature.

In the previous paper [9], the free and reactionless movement of death layer elements is done by applying a very low YOUNG's modulus in COMSOL package and the activation of the elements is realized by switching the YOUNG's modulus back to the original physical material value. The difference of this study is the birth and death method in ANSYS.

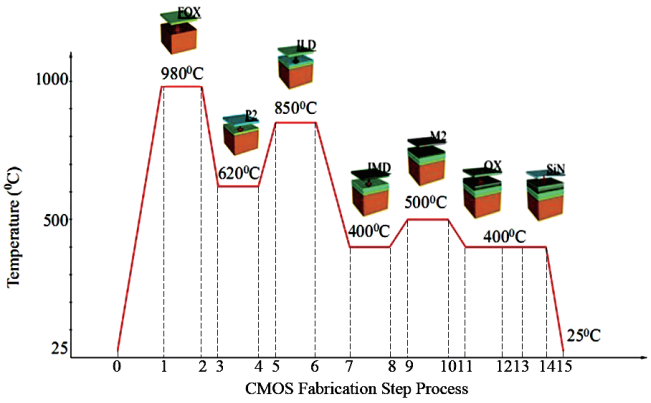


Fig. 2 The schematic diagram of CMOS fabrication step process

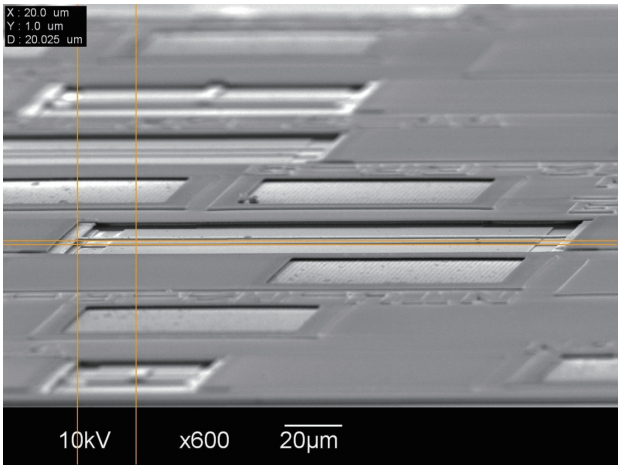


Fig. 3 The measurement of the deformation by using SEM image analysis [8]

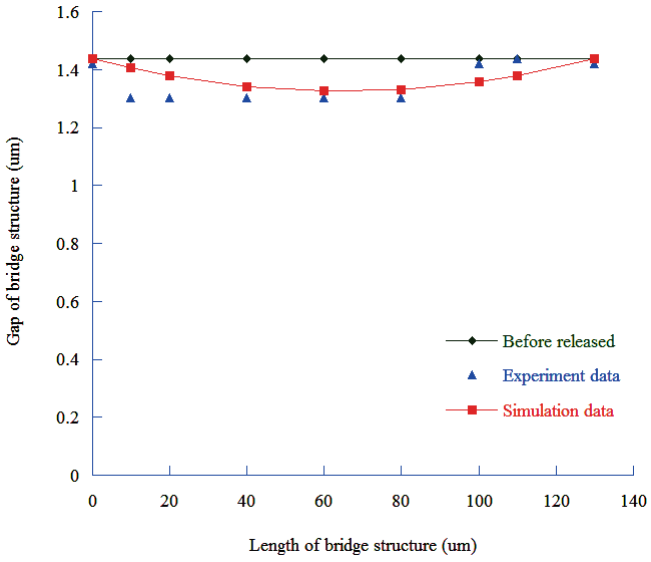


Fig. 4 The comparison between experimental data and simulation result of the 2P2M bridge structure with $L = 130\mu m$

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Figures 5 and 6 show the comparison of the final deformation and y — displacement between COMSOL [9] and this study by ANSYS. Through these figures, the maximum deformation by using ANSYS and COMSOL package can be observed is 0.806μm and 0.8μm, respectively. It finds that the simulation result in ANSYS package agree well with the previous paper. The average deviation is 0.66%.

5. OPTIMIZATION METHOD

In this study, the objective function is to find the minimum Von Mises stress in the CMOS fabrication through the optimal process. The Von Mises stress (as known as equivalent stress, σ_{eqv}) is given by:

$$J = \sigma_{eqv} = \sqrt{\frac{(\sigma_1 - \sigma_2)^2 + (\sigma_2 - \sigma_3)^2 + (\sigma_3 - \sigma_1)^2}{2}} \qquad (4)$$

Assume that, a set of undetermined coefficients to be optimized in the iterative process. Different combinations of these coefficients can derive the minimum Von Mises stress from the finite element package, ANSYS. The minimum objective function is accomplished by using the SCGM method. The method evaluates the gradient functions of the objective function and sets up a new conjugate direction for the updated undetermined coefficients with the help of a direct numerical sensitivity analysis. The detailed process of this proposed optimal method is illustrated in our previous paper related to the LED design [10]. In this study, the step size of the iterative process is determined by a trial and error process, and the value is set to be 1×10^{-4} for the film sensor design.

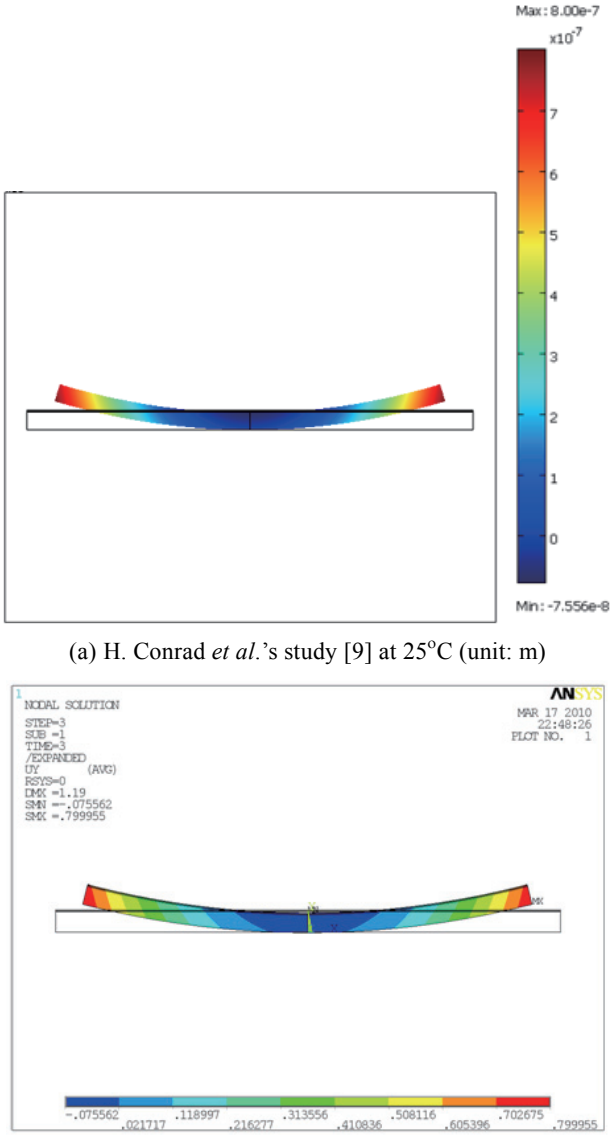
6. RESULTS AND DISCUSSIONS

6.1 CMOS Fabrication

To predict and minimize the residual stresses in the CMOS fabrication process is the purpose of this study. Here, each layer of the CMOS follows the corresponding deposition temperature during the fabrication process as shown in Fig. 2. After the top layer (S_iN) deposited, all layers will be cooled by natural cooling. Figure 7 shows the profiles of the residual stress, S_x, with different layers in the fabrication process.

S_x of 1st ~ 7th layer is −146.7MPa, −43.5MPa, −115.4MPa, −216.1MPa, 257.5MPa, −200MPa and −101.6MPa, respectively. It is clearly that the residual stress not only depends on the CTE of the deposited material but also the deposited temperature. In addition, the maximum S_x is 257.5MPa happened on the 5th layer of Al at x is 748μm (the free edge of this model) at the last step.

CMOS failure mechanisms are mainly controlled by the magnitude and distribution of S_x, S_y, and shear stress S_{xy}. The maximum tensile and compress stress of the residual stress S_y is 111.1MPa and −123.8MPa and



(a) H. Conrad *et al.*'s study [9] at 25°C (unit: m)

(b) Present study at 25 °C (unit: μm)

Fig. 5 The final deformation of this fabrication: (a) H. Conrad *et al.*'s study [9]; (b) present study

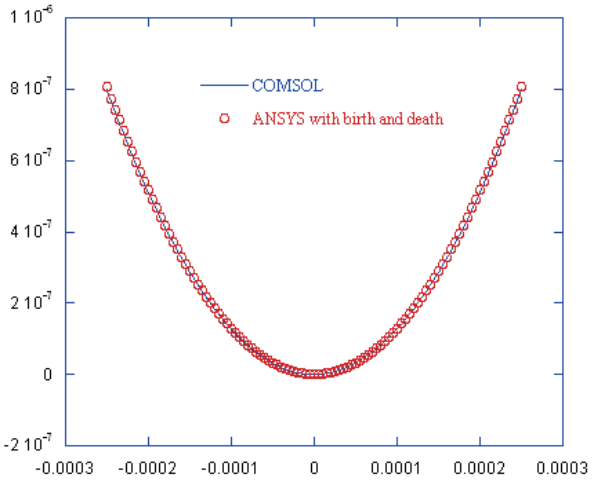


Fig. 6 The comparison of the y-deformation (m) between H. Conrad *et al.*'s study (COMSOL) [9] and present study at 25°C (ANSYS)

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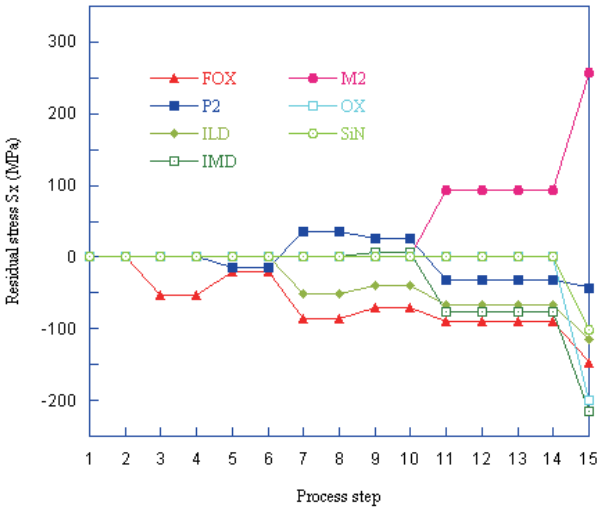


Fig. 7 Stress variation during fabrication process steps in different layer

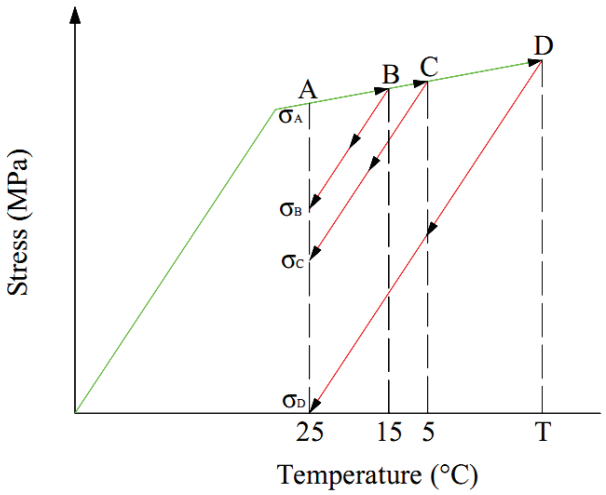


Fig. 8 Schematic constitutive model for cases A, B, C

concentrates at the free edge of this model. Similarity, the maximum tensile and compress stress of the shear stress S_{xy} is 70.9MPa and 96MPa and happens on the free end, too. The details are shown in Table 3. Therefore, the cracks could originate at the free edge due to the high concentration of S_y and shear stresses S_{xy}.

The above discussion about the generation of the residual stresses is happened on the standard CMOS fabrication process. The different cooling at the last step is proposed to reduce the residual stress. Therefore, Case A, B, C is the final temperature of the fabrication decreased to 25°C, 15°C and 5°C subsequently returned to room temperature by natural convection, separately. It shows that the tensile and compress residual stress of S_x is –216.1MPa, 257.5MPa in case A, –211.1MPa, 246MPa in case B, and –205.9MPa, 234.5MPa in case C, respectively. The other components residual stress are also reduced and illustrated in Table 3.

According to these cases, a qualitative explanation for the stress reduction shows as Fig. 8 schematically. The recovery of cooling process will benefit the decreasing of the residual stress. Here, point A denotes the stress σ_A of case at room temperature. In addition, point B is the stress of case B and the stress will decrease from point B to σ_B as the temperature is from 15°C to the room temperature following the natural recover process. A lower cooling temperature will result in further stress reduction to σ_C (Case C). Possibly, case D can be assumed if the temperature cools to temperature T, the residual stress would be released at room temperature.

6.2 Optimal Residual Stress in the CMOS Fabrication

The aim of this study is to achieve the minimum Von Mises stress in the CMOS fabrication process through SCGM combined with ANSYS. Depending on the characteristic of the fabrication process, the optimization includes two variables that are heat transfer coefficient ($x1$) and cooling temperature ($x2$) at the last step.

Table 3 Comparison of the residual stress in three cases

Case	S_x		S_y		Shear stress S_{xy}	
	Compress	Tensile	Compress	Tensile	Compress	Tensile
A	–216.1	257.5	–123.8	111.1	–96	70.9
B	–211.1	246	–116.8	110	–92.4	67.8
C	–205.9	234.5	–109.9	108.9	–88.8	64.7

The different heat convection coefficient for the cooling speed to the cooling temperature is proposed at the last step when deposition of last layer completes. The cooling temperature is chosen lower than room temperature and the CMOS-MEMS microphone will back to the room temperature following the natural recovery process. The range of the variable $x1$ is $35\text{W/m}^2\text{K} < x1 < 50\text{W/m}^2\text{K}$ and variable $x2$ is $5°\text{C} < x2 < 25°\text{C}$.

The residual stress profiles of the Aluminum layer in the initial and optimal CMOS fabrication are described in Fig. 9. It requires approximately 155 iterations to reach the optimal design. The Von Mises stress after finishing the CMOS fabrication process at room temperature is reduced from 248.5MPa to 226.1MPa. As the result, the residual stress in this layer is reduced clearly. Here, the initial value of $x1$ and $x2$ is $50\text{W/m}^2\text{K}$ and 20°C, separately. In addition, the optimal value of these variables is $35\text{W/m}^2\text{K}$ and 5°C, separately. After the optimal procedure, the difference is 22.4MPa and the residual stress is reduced about 9%.

The residual stress distributions of the initial and optimal CMOS design are shown in Fig. 10. Through this figure, the residual stress distribution is similar between the initial and optimal CMOS device but the stress of each layer decreasing obviously in the optimal device. It proves that the residual stress in CMOS fabrication process can minimum with suitable fabrication parameter.

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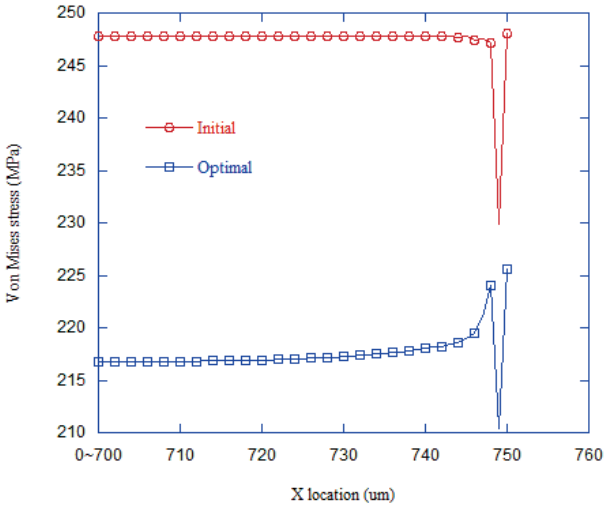
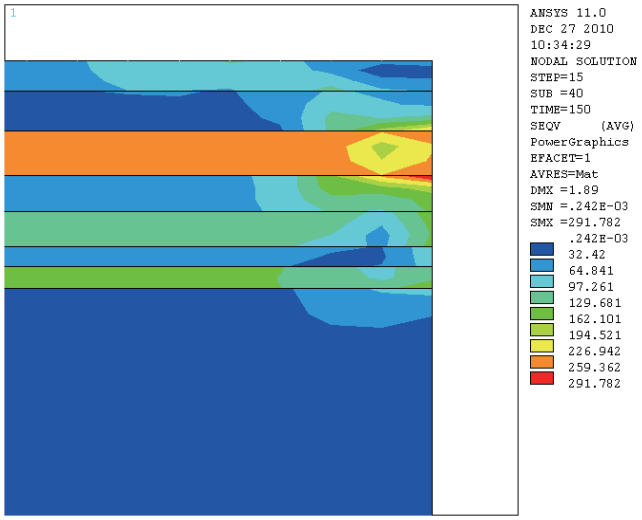
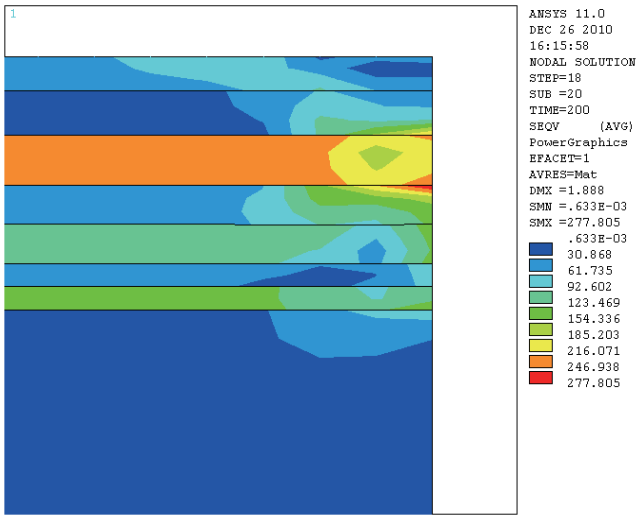


Fig. 9 The residual stress profiles of the Aluminum layer in the initial and optimal CMOS fabrication



(a) Initial design



(b) Optimal design

Fig. 10 The residual stress distribution of the (a) initial and (b) optimal design

7. CONCLUSIONS

The general purpose of the present study uses the ANSYS combined with SCGM to minimize the residual stresses in the CMOS fabrication process. The coupled heat transfer and elastic – plastic model and the birth and death method are used on the analysis and validation. The cooling speed and cooling temperature of the last step are chosen as the design variable to reduce the residual stress.

After the optimal process, the residual stress is reduced about 22.4MPa and 9%. It demonstrates that the suitable parameter on the fabrication can reduce the residual stress in MEMS devices without any extra manufacturing process or external apparatus.

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