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SICL based Ka-band series SPDT switch for duplexer application

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Research Paper

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Abstract

This paper presents a Ka-band series single-pole double-throw (SPDT) switch circuit realized in substrate-integrated coaxial line (SICL) environment for time division duplex operation. It is designed with a low-cost printed circuit board (PCB) technique. The size of the proposed circuit is $3.1\lambda_g \times 5.9\lambda_g$, where λ_g is the guided wavelength at the center frequency of 27.75 GHz. In this circuit, a SICL-based SPDT switching circuit is proposed with radio frequency (RF) isolation network where the shunt connection of butterfly stubs is in an asymmetric stripline environment. The proposed circuit exhibits less than 2 dB insertion loss at 27–27.9 GHz and less than 2.5 dB insertion loss at 27–28.5 GHz. The design offers good impedance matching in the Transmit (Tx) and Receive (Rx) channels from the common Tx/Rx input channel, along with more than 24 dB isolation between ON and OFF state output channels. The proposed circuit is suitable for millimeter-wave communication systems.

Introduction

A duplexer circuit plays an important role in the RF transceiver, which helps to direct a common input signal into two individual output streams at different time instant. Now a days, time division duplex (TDD) is highly demanding scheme for the duplexer circuit. Generally, a single-pole double-throw (SPDT) switch is dominantly used for TDD operation, where the SPDT switch is followed by a duplexer as shown in Fig. 1(a), where the series SPDT switch configuration is operated at 2.4 GHz [1]. Many circuit designer have adopted conventional PCB design process for the implementation of SPDT switch at L, S, X, and Ka bands [2–8]. However, the conventional PCB fabrication approach is rarely employed in millimeter-wave applications due to the significant radiation loss and undesirable surface wave loss produced by the varied dimensions of a microstrip line. With the development of the modern 5G wireless communication system, the designated millimeter wave frequency bands should support the TDD scheme, and hence a new millimeter wave SPDT switch circuit is needed. The main challenge of designing such a circuit involves maintaining good isolation between two output ports while maintaining low insertion loss and good impedance matching in the desired path. Designing millimeter wave SPDT switch circuit at high frequencies require additional considerations about PCB material and transmission line theory. Recently, a novel planar configuration of the conventional coaxial line, named the substrate integrated coaxial line (SICL), has been proposed. It is used to compensate for all of these issues in millimeter wave frequency applications [9].

The SICL acts as a printed version of a typical coaxial line created by encircling a conducting strip with metallic plates and laterally confining it with plated through holes (PTHs) on both sides. The coaxial nature of SICL is improved by a conducting strip imposed through the PTHs. Due to the similar nature of a coaxial line, SICL allows single-mode TEM wave propagation across a wide frequency range, and the self-shielding configuration helps to implement low-loss lines in millimeter wave frequencies [10–13]. In this paper, the proposed SICL based SPDT switch circuit adopts a low-cost PCB design technique at 27–28.5 GHz as shown in Fig. 2. The proposed network comprises of SPDT switching circuit using a series of butterfly stubs and mounting pads for the integration of diodes and capacitors which was introduced in [14]. However, the placement of the butterfly stubs at the middle layer eliminates the possibility of spurious radiation as it is shielded by the top and bottom copper plates in asymmetric stripline environment and increases the isolation between RF and DC paths. The sidewall ensures good shielding of the main RF line channels, which helps to improve the impedance matching between Tx to Tx/Rx and Rx to Tx/Rx channel. A single-layer ceramic capacitors (DC blocks) are mounted on the top layer of the SICL in the path of Tx to Tx/Rx and Rx to Tx/Rx. The main contributions of our research work are summarized as follows:

- The proposed design adopts SICL technology to implement a SPDT switch in a low-profile planar configuration which performs TDD operation. To the best of author's knowledge, this is the first time to realize a planar SPDT switch circuit for duplexer application using SICL technology in 27–28.5 GHz.

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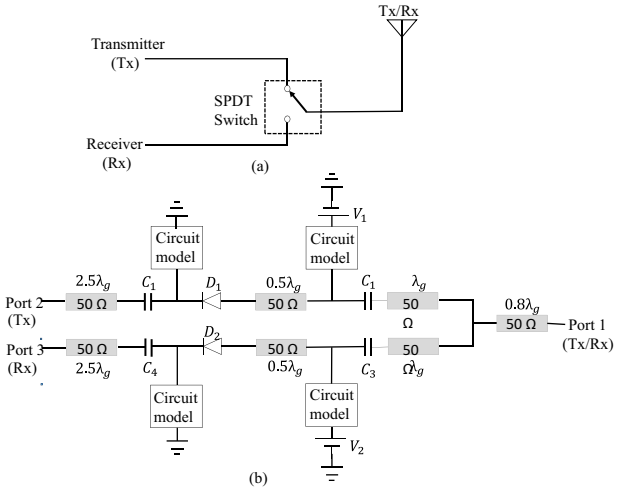


Figure 1. (a) Conventional SPDT switch in RF transceiver system. (b) Proposed equivalent circuit of SPDT switch.

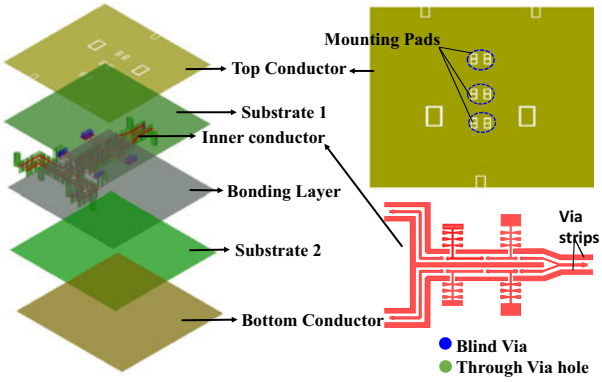


Figure 2. 3-D view of the proposed duplexer.

- The self-shielded structure of SICL helps the proposed circuit to operate at millimeter wave frequencies with satisfactory performance.
- The proposed design provides a mechanism to connect SMD components with SICL technology which is an important stepping stone for realizing SICL based systems [14].
- The RF isolation network is introduced in an asymmetric stripline environment where the placement of the butterfly stub at the middle layer eliminate the possible chance of spurious radiation as it is shielded by the top and bottom copper plates and increases the RF isolation between RF and DC path which helps to supply better transmission at the two output streams in millimeter-wave communication systems.

The explanation of design procedure for the proposed duplexer is shown in section "Design procedure of proposed SPDT switch". The results and discussion of the circuit are presented in section "Experimental results and discussion."

Design procedure of proposed SPDT switch

In this paper, two 0.25-mm thick Taconic TLY-5 ($\epsilon_r = 2.2$, $\tan\delta = 0.0009$) based substrate along with bond layer Taconic FR-28 prepreg ($\epsilon_r = 2.8$, $\tan\delta = 0.0014$) is used to realize the proposed design. The proposed circuit introduces an RF isolation network

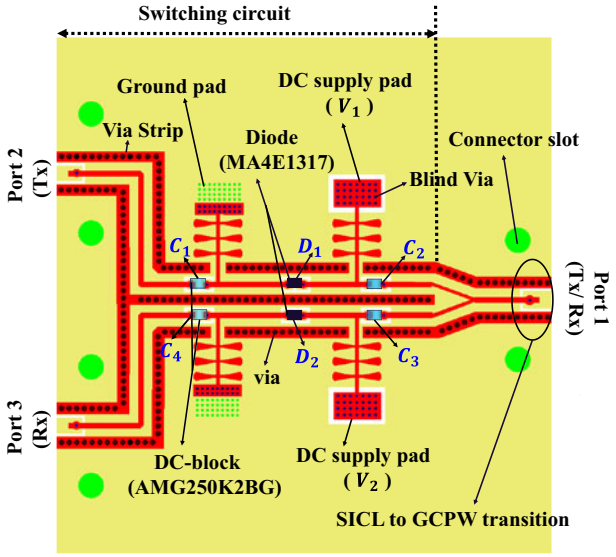


Figure 3. Physical structure of the proposed duplexer circuit.

which are used to activate the RF switches in the corresponding channels (Tx and Rx) by the DC supply. The equivalent circuit and physical layout of the proposed circuit are shown in Figs. 1(b) and 3, respectively.

Design of RF isolation network for DC supply

Figure 4(a) and (b) show the physical layout and stack up of the substrate for the proposed isolation circuit where a series of three butterfly stubs are used for the high isolation in the middle layer of the substrate, which is separated from the top and bottom ground plate as an asymmetric stripline structure [14]. The characteristic impedance of the asymmetric stripline ($Z_{0,AS}$) depends on the ratio of the conductor width and distance between the signal and ground planes. The characteristics impedance ($Z_{0,AS}$) can be calculated as follows [15]:

$$Z_{0,AS} = \frac{1}{\sqrt{\epsilon_r}}\left[Z_{0,SS}\left(\epsilon_r = 1, H = h_1 + h_2 + t\right) - \Delta Z_{0,air}\right], \quad (1)$$

where $Z_{0,SS}(\epsilon_r = 1, H = h_1 + h_2 + t)$ is the characteristics impedance of symmetric stripline. The value of $Z_{0,SS}$ is derived from (2)–(4), with air as the dielectric and having total thickness ($H = h_1 + h_2 + t$):

$$Z_{0,SS} = \frac{\eta_0}{2\pi\sqrt{\epsilon_r}} \ln\left\{1 + \frac{4H}{\pi w'}\left[\frac{8H}{\pi w'} + \sqrt{\left(\frac{8H}{\pi w'}\right)^2 + 6.27}\right]\right\}, \quad (2)$$

where

$$w' = w + \frac{t}{\pi}\ln\left\{\frac{e}{\sqrt{\left(\frac{t}{2H+t}\right)^2 + \left(\frac{\pi t}{4(w+1.1t)}\right)^m}}\right\}, \quad (3)$$

$$m = \frac{6H}{3H + 2t}, \quad (4)$$

and

$$\Delta Z_{0,air} = 0.0325\pi Z_{0,air}^2\left(0.5 - \frac{1}{2}\frac{2h_1 + t}{h_1 + h_2 + t}\right)^{2.2} \times n \quad (5)$$

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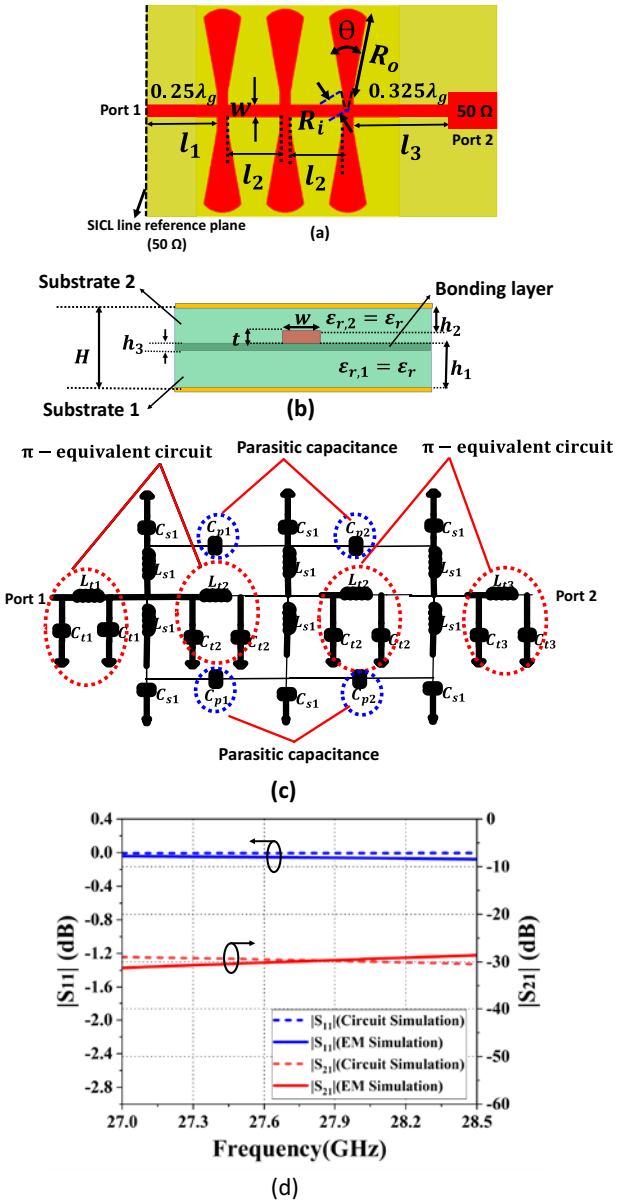


Figure 4. Physical layout of a series butterfly stubs with the dimension $R_i = 0.16$ mm, $R_o = 1.9$ mm, $\theta = 23^o$, $w = 0.24$ mm. (a) Top view. (b) Substrate stackup of the proposed design where $h_1 = 0.354$ mm, $h_2 = 0.254$ mm, and $h_3 = 0.1$ mm. (c) The proposed equivalent circuit model of the series butterfly stubs with lossless central transmission lines. (d) Response of EM and circuit simulation of the series butterfly stubs with lossless central transmission lines from optimized values of $L_{t1} = 0.38$ nH, $C_{t1} = 0.0856$ pF, $L_{t2} = 0.289$ nH, $C_{t2} = 0.0373$ pF, $C_{s1} = 0.064$ pF, $L_{s1} = 0.54$ nH, $C_{t3} = 0.14$ $L_{t3} = 0.5$ nH, $C_{p1} = 0.0133$ pF, $C_{p2} = 0.0133$ pF.

$$n = \left(\frac{t+w}{h_1+h_2+t}\right)^{2.9}, \tag{6}$$

where h_1 is the distance between the signal line and the lower reference plane, h_2 is the distance between the signal line and the upper reference plane, and $Z_{0,air}$ is represented by Equation (7):

$$Z_{0,air} = 2\left[\frac{Z_{0,SS}(\epsilon_r = 1, H = h_1)\, Z_{0,SS}(\epsilon_r = 1, H = h_2)}{Z_{0,SS}(\epsilon_r = 1, H = h_1) + Z_{0,SS}(\epsilon_r = 1, H = h_2)}\right], \tag{7}$$

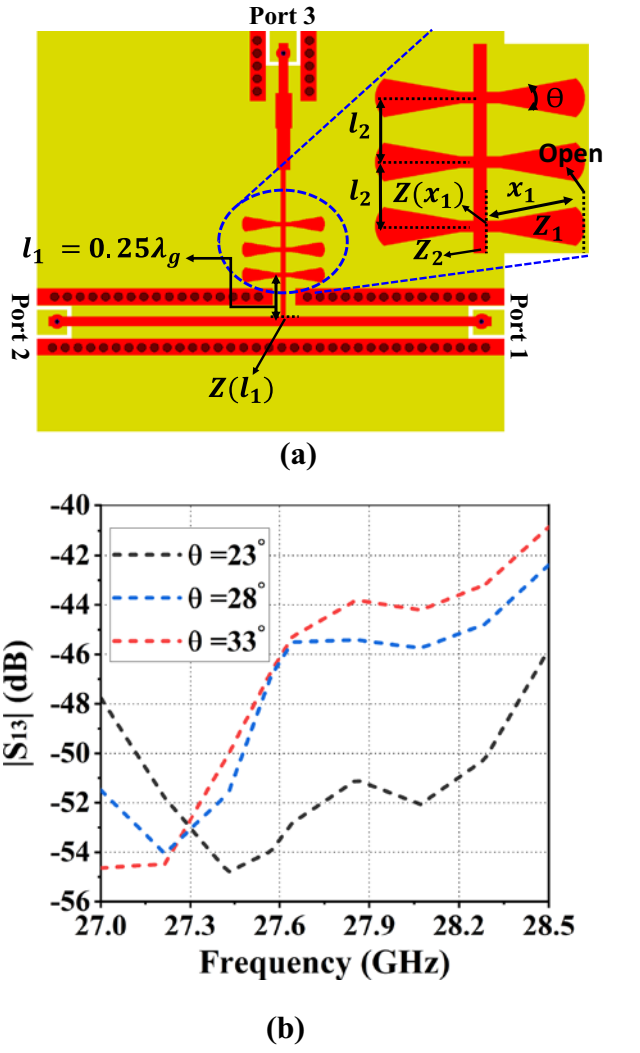


Figure 5. (a) Physical layout of the proposed RF isolation network (including three butterfly stubs) with SICL line. (b) Response of isolation between Ports 1 and 3 with the variation of spanning angle (θ).

where $Z_{0,SS}(\epsilon_r = 1, H = h_1)$ is the characteristic impedance of symmetric stripline as shown in (2) with air as the dielectric and having total thickness of the line equal to h_1; and $Z_{0,SS}(\epsilon_r = 1, H = h_2)$ is the characteristic impedance of symmetric stripline with air as the dielectric and total thickness of the line equal to h_2.

The series of butterfly stubs is connected with a lossless central transmission line sections. The equivalent circuit parameters of the bias line are obtained with the help of the telegrapher's equation parameters as described in [16]. A high-impedance lossless line terminated at both ends by relatively low-impedance lines can be presented by a π-equivalent circuit, as shown in Fig. 4(c). Also, the small section of high impedance line with radial stub at both ends introduces discontinuity at the junction which is represented by another π circuit. The values of L_t and C_t can be obtained from (8) and (9):

$$L_t = \frac{1}{2\pi f_1} \times Z_{0,AS} \times \sin\left(\frac{2\pi l}{\lambda_g}\right), \tag{8}$$

$$C_t = \frac{1}{2\pi f_1} \times \frac{1}{Z_{0,AS}} \tan\left(\frac{\pi l}{\lambda_g}\right), \tag{9}$$

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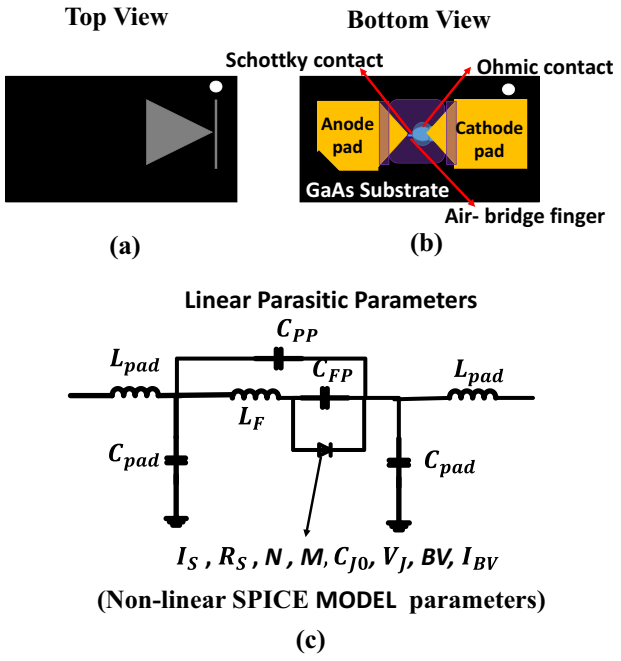


Figure 6. (a) Top view of physical layout of MA4E1317. (b) Bottom View physical layout of MA4E1317. (c) Large signal equivalent circuit model of MA4E1317 (Schottky diode) with the parameters of $L_{pad} = 4.3$ pH, $C_{pad} = 4$ fF, $L_f = 0.28$ nH, $C_{PP} = 0.017$ pF, $C_{FP} = 0.016$ pF, $I_s = 0.12$ pA, $R_s = 3.15\Omega$, $N = 1.22$, $C_{jo} = 0.02$ pF, $M = 0.48$, $I_{BV} = 10\,\mu$A, $V_j = 0.67$ V, $BV = 10$ V.

$$L_s = \frac{120\pi H(2.8 - 10\frac{R_i}{R_o})}{c\theta}, \tag{10}$$

$$C_s = \frac{\theta R_o^2 \epsilon_r}{240\pi H c}. \tag{11}$$

The next equations of (10) and (11) are obtained from [17], where f_1 is the center frequency of the operating band, H is the total substrate height in mm, R_i is the inner radius, and R_o is the outer radius of the butterfly stub, c is the speed of light, θ is the spanning angle in radian. Using the design equations of (8)–(11) with considering the parasitic capacitance effects (C_{p1}, C_{p2}) between the radial stubs, the equivalent circuit is proposed in the operating frequency of 27–28.5 GHz. With the help of known parameters such as R_o, R_i, and spanning angle θ, the initial values of L_s and C_s can be calculated. Further, the circuit is tuned slightly to have better agreement between EM and circuit simulation as shown in Fig. 4(d). Next, the first butterfly stub is considered which is directly connected to the main RF line at the distance of l_1 and it is radial stub is an open circuit at the distance of R_0. The l_1 and R_0 are maintained to approximately odd multiple of $\lambda_g/4$, so that it behaves as open circuit for the main RF line [18, 19]. Moreover, we added the other two butterfly stubs while maintaining the small gap of $l_2 = 1$ mm using the lossless line. Now, the series butterfly stubs are combined with the SICL line and the performance is shown in Fig. 5(a). The isolation graph is observed ($|S_{13}|$), which varies with the spanning angle as shown in Fig. 5(b). The optimized spanning angle is chosen, 23° for the proposed duplexer circuit.

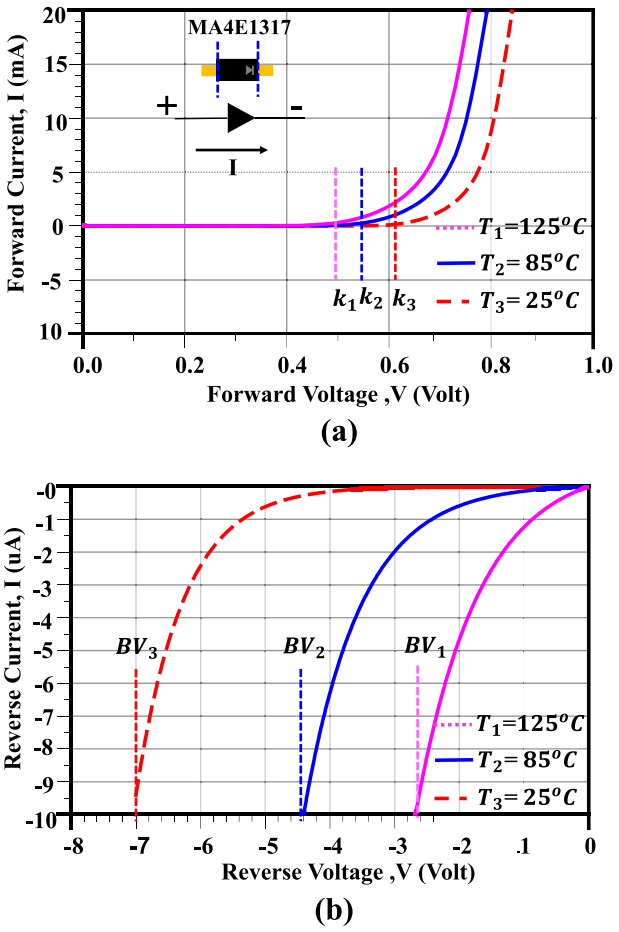


Figure 7. (a) *I–V* characteristics of the diode (MA4E1317) in forward bias condition with different temperatures where $k_1 = 0.44$ V, $k_2 = 0.5$ V, $k_3 = 0.6$ V. (b) *I–V* characteristics of the diode in reverse bias condition with different temperatures where $BV_1 = 2.7$ V, $BV_2 = 4.4$ V, $BV_3 = 7$ V.

I–V characteristics and S-parameter behavior of the diode model (MA4E1317)

Figure 6(a)–(c) shows diode model and its large signal model. The diode model of MA4E1317 is selected for the proposed SPDT switch. Figure 7(a) and (b) shows the I–V characteristics of diode model MA4E1317 with the temperature variation at forward and reverse bias, respectively. The physical model is composed of Schottky contact, Ohmic contact, Airbridge finger, cathode and anode contact pads and GaAs substrate. The large signal equivalent circuit model is created by the fringing field between both pads, which is modeled as a pad-to-pad capacitance, C_{PP}. Next, Finger pad coupling is modeled as C_{FP}, self-inductance of Airbridge finger modeled as L_F, the contact pads are denoted as C_{pad} and L_{pad}. The diode Spice Model represents the Schottky junction, non-linear junction capacitance, and resistance [20]. The effects of full parasitic with spice model are analyzed from the I–V characteristics in Keysight ADS software.

Working principle of SPDT switch as duplexer circuit

The SPDT switch as duplexer circuit consists of three port network device. It is operated with a diode ON and OFF state. In the

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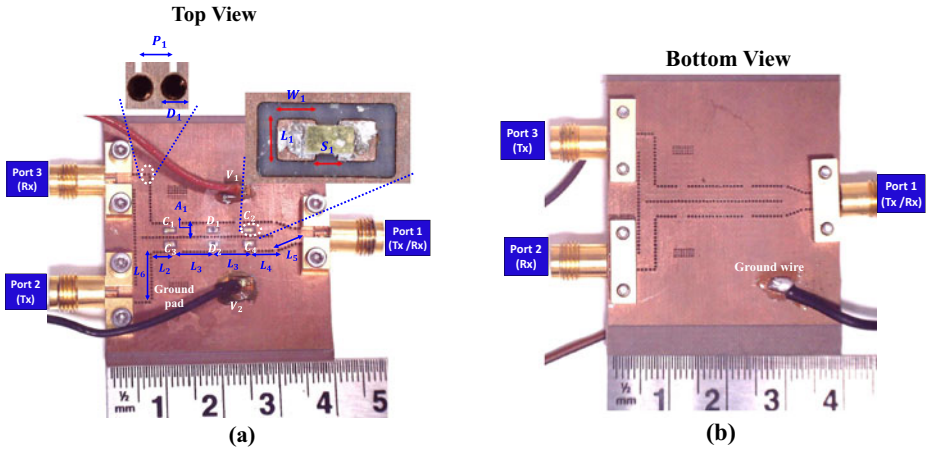


Figure 8. Fabricated prototype of the proposed SPDT switch as duplexer circuit with important dimensions, $L_1 = 0.85$ mm, $L_2 = 2.7$ mm, $L_3 = 5.2$ mm, $L_4 = 3.9$ mm, $L_5 = 3.4$ mm, $L_6 = 8.4$ mm, $P_1 = 0.62$ mm, $D_1 = 0.42$ mm, $S_1 = 0.28$ mm, $A_1 = 1.7$ mm, $W_1 = 0.82$ mm. (a) Top view. (b) Bottom view.

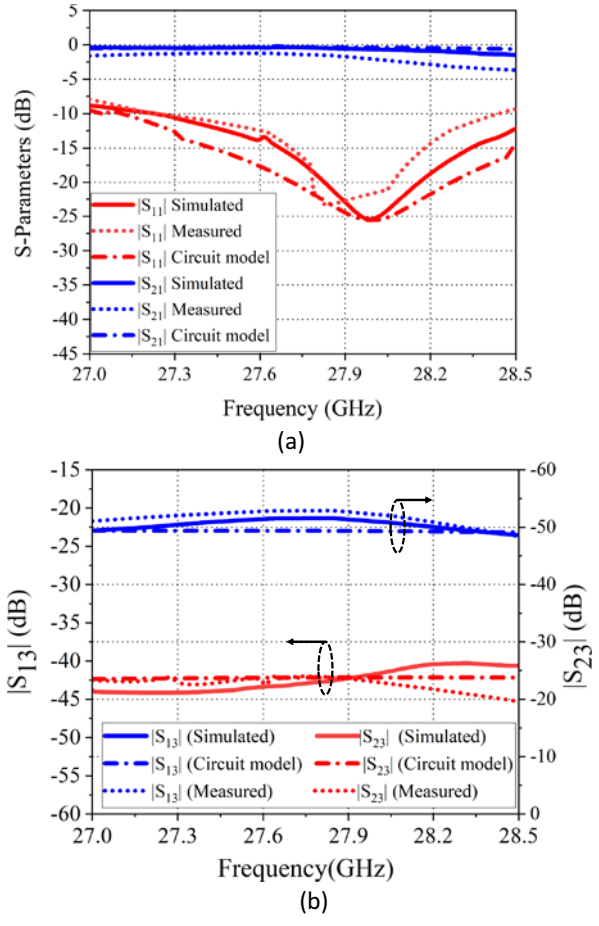


Figure 9. (a) Performance of the duplexer circuit results in reflection coefficient ($|S_{11}|$) and insertion loss ($|S_{21}|$) from Tx/Rx to Tx channel. (b) Results of isolations ($|S_{13}|$) and ($|S_{23}|$) between Port 2 (Tx)–3 (Rx) and Port 1 (Tx/Rx)–3 (Rx) where $V_1 = 0.9$ V and $V_2 = -4$ V.

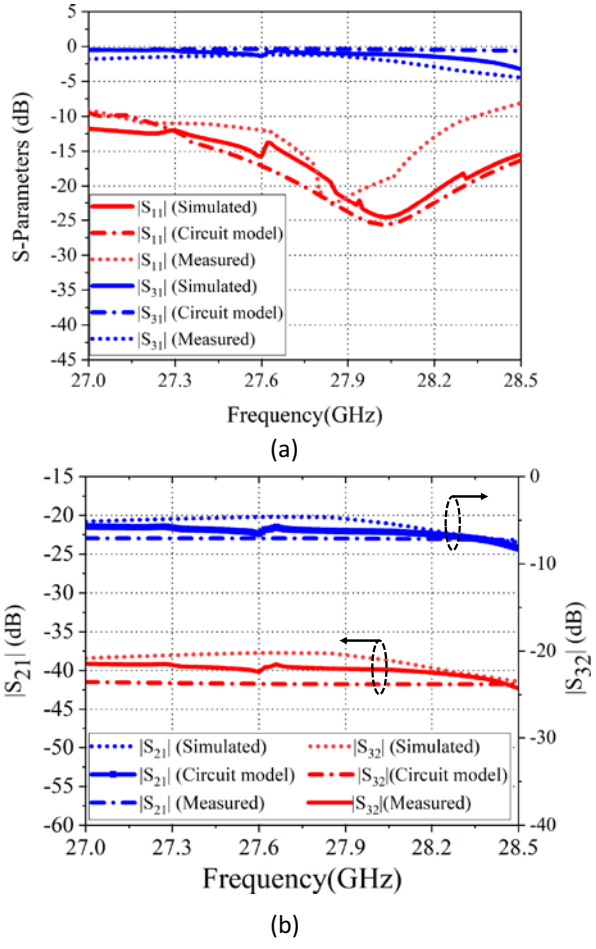


Figure 10. (a) Performance of the duplexer circuit results in reflection coefficient ($|S_{11}|$) and insertion loss ($|S_{31}|$) from Tx/Rx to Tx channel. (b) Isolations ($|S_{12}|$) and ($|S_{32}|$) between Port 1 (Tx/Rx)–2 (Tx) and Port 2 (Tx)–3 (Rx) where $V_1 = -4$ V and $V_2 = 0.9$ V.

duplexer circuit, when applying the DC bias condition such as forward voltage, $V_1 = 0.9$ V to diode D_1 and reverse voltage, $V_2 = -4$ V to diode D_2. The diode D_1 is ON state and D_2 is OFF state, respectively. The diode D_2 is placed at a distance of $2\lambda_g$ from the junction. As a result, the impedance seen from the junction toward Port 3 becomes infinity and the RF signal only passes from Port 1 to Port 2. Similarly, when the DC bias condition is reversed ($V_2 = 0.9$ V, $V_1 = -4$ V), the diode D_2 is ON, and D_1 is OFF state, respectively.

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Table 1. Comparisons of the proposed SPDT switch with the previous SPDT switch's

Ref.	Tech.	Tx/Rx Center Freq (GHz)	Tx to Rx Iso. (dB)	RL (dB)	IL (dB)	Electrical Size (λ_g^2)	No of layers	Fabrication complexity	Structure
1.	ML	2.4/2.4	13.8	16.8	0.58	Not Fabricated	N. A	N. A	Semi-open
2.	ML	2.3/2.3* 9.4/9.4*	15.39	15.27	1.89	2.1 35.22	2	Easy#1	Semi-open
3.	ML	9.4/9.4*	30	16	2.4	2.2	2	Easy#1	Semi-open
4.	ML	1.75/1.75*	25	N.M	1.8	N.M	2	Easy#1	Semi-open
5.	ML with DGS	2.4/2.4*	13.7	N.M	0.91	N.M	2	Easy#1	Semi-open
6.	HMSIW	5/5*	28.5	15	1.78	2.9	2	Medium#1	Semi-open
7.	SIW	10/10*	18	25	1.6	18.94	2	Medium#1	Semi-open
8.	65 nm CMOS	28/28 (mmWave frequency)	24	14	1.8	N.M	N. A	Difficult#2	Semi-open
TW	**SICL**	**27.75/27.75** (mmWave frequency)	**26**	**20**	**1.7**	**17.26**	**3**	**Medium#1**	**Shielded**

Tech: Technology, ML: Microstrip line, DGS: Defective ground structure, N.M: Not Mentioned, N.A: Not Applicable, RL: Return Loss, IL: Insertion Loss, #1Low-cost PCB technology, #2High-cost RFIC fabrication technology, *Microwave frequency.

In the reverse bias condition, Port 2 behaves as an open circuit which allows the transmission of RF signal from Port 1 to Port 3.

Experimental results and discussion

Figure 8(a) and (b) shows the fabricated prototypes and responses of the SPDT circuit with the diodes (D_1 and D_1) model MA4E1317 [20] and capacitors (C_1, C_2, C_3, and C_4). The proposed duplexer circuit has been developed with a SICL to GCPW transition, which is applied on all ports for edge mount connector interfaces. Figure 9(a) and (b) present the simulated and measured results of the reflection coefficients, which is below −10 dB at the band, and insertion losses vary from 0.2 to 2.5 dB between Port 1 (Tx/Rx) and Port 2 (Tx) while maintaining the isolation's 22–26 dB between Port 2 (Tx) and Port 3 (Rx) when D_1 is ON and D_2 is OFF state, respectively at 27–28.5 GHz. Similarly, Figure 10(a) and (b) presents the simulated and measured results for the reflection coefficients and insertion losses with the isolations maintained around 21–26 dB between Port 3 (Rx) and 2 (Tx) when D_1 is OFF state and D_2 is ON state, respectively at 27–28.5 GHz. The simulated results are validated with measured results in the frequency range of 27–28.5 GHz from Agilent N5234A Network Analyzer with DC supply HMP4030, where the measured results followed the simulated results with a slight deviation due to fabrication tolerance and connector loss.

Table 1 shows the comparisons of the proposed SPDT switch with the previous SPDT switches.

Conclusion

The design and development of the SPDT switch circuit for duplexer application are presented in this paper. The results obtained from simulation and measurement are in good agreement. The results of the SPDT switch exhibit less than 2 dB insertion loss in 27–27.9 GHz and less than 2.5 dB insertion loss in 27.9–28.5 GHz with better impedance matching in the transmit (Tx) and receive (Rx) channel from Tx/Rx channel. The proposed design is realized with a low-cost PCB design technique. It is suitable for millimeter wave active circuits and communication systems application.

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Competing interests. The authors report no conflict of interest.

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