International Journal of Microwave and Wireless Technologies, 2011, 3(1), 1–9. © Cambridge University Press and the European Microwave Association, 2011
doi:10.1017/S1759078710000814

Division by current: a new approach to FET capacitance modeling

STEPHEN MAAS

This paper introduces a new approach to the modeling of capacitance in field-effect transistor (FET) devices, which we call division by current. *It is compared with existing formulations, which we call* division by capacitance *and* division by charge. *In doing so, it is necessary to normalize the theory of nonlinear capacitances and to clarify a number of matters. These include charge conservation and determination of charge functions from capacitance measurements, which are often misstated in the literature. We find the division by current formulation to be practical and to have significant advantages in the generation of FET models and in circuit simulation.*

Keywords: FET, modeling, capacitance, nonlinear charge functions

Received 5 August 2010; Revised 14 November 2010; first published online 3 February 2011

I. INTRODUCTION

This paper introduces a new approach to field-effect transistor (FET) capacitance modeling, which we call *division by current*. Although the focus is primarily on microwave FETs, the method is relevant to other types of FET devices as well, and to any kinds of devices using capacitances with multiple control voltages. In doing this, we compare it to two existing formulations, which we call *division by capacitance* and *division by charge*. Although it is possible to create an equivalence between our new formulation and a division-by-charge formulation (but not division-by-capacitance), the new one has a number of advantages:

1) It avoids many of the endemic problems of existing modeling approaches, such as charge nonconservation and inconsistency. Since it is based on a single charge region, it avoids a situation where gate charge is conserved but individual gate-to-source and gate-to-drain charges are not.
2) It is straightforward to implement.
3) Properly implemented, it is numerically efficient and stable.
4) Parameter extraction for models using the division-by-current approach is straightforward and well conditioned.

Early nonlinear FET capacitance models suffered from serious errors, which by now have been well documented. One was called the *consistency problem*: small-signal models were not equivalent to large-signal models operated at weak excitations [1]. Another was charge nonconservation, in which the charge at the completion of a period of a periodic waveform was unequal to that at the beginning [2–6]. In particular, it sometimes happened that dividing the gate charge into two regions, the gate-to-drain and gate-to-source capacitances, created two nonconservative charge regions while the original gate charge was conservative [4].

Capacitance, which is, after all, a linear concept, must be carefully defined in nonlinear circuits; describing nonlinear capacitances by charge functions eliminates many of the difficulties. The consistent use of charge concepts, instead of capacitance, would do much to eliminate endemic conceptual errors in nonlinear circuit modeling. For this reason, this paper focuses primarily on charge. We use the term *capacitance* loosely, to refer to nonlinear capacitive reactances, which are defined by charge functions.

II. THEORY

All FETs experience gate charging. The gate charge is balanced by an oppositely charged region below the gate. In junction FETs, this is a depletion region, but in HEMTs and MOSFETs, that charge region is somewhat more complex. A circuit element that models this capacitance is unusual, as it has three terminals: the FET's intrinsic source, gate, and drain (Fig. 1). As such, it is controlled by (i.e., its charge is a function of) the voltages between any two pairs of terminals. Traditionally, the control voltages are chosen to be the gate-to-source and drain-to-source voltages, V_{gs} and V_{ds}, respectively, but the use of gate-to-source and gate-to-drain voltages, V_{gs} and V_{gd}, respectively, preserves the symmetry existing in most FETs. For this reason, we shall use the latter, in most cases, in the remainder of this paper.

The gate is one terminal of this capacitor. As such, the reactive gate current is easily defined as $dQ_g(t)/dt$, where $Q_g(t) = Q_g(V_{gs}(t), V_{gd}(t))$ is the gate charge. This current is divided between the drain and source terminals in a manner that is not obvious, but, clearly, it must satisfy Kirchoff's current law; thus,

$$I_g + I_s + I_d = 0 \tag{1}$$

Nonlinear Technologies, Inc., P.O. Box 7284, Long Beach, CA 90807, USA.
Corresponding author:
S. Maas
Email: s.maas@nonlintec.com

https://doi.org/10.1017/S1759078710000814 Published online by Cambridge University Press

where I_g, I_s, and I_d are the reactive components of the gate, source, and drain current, respectively.

Knowing that the gate charge balances the reactive component of the channel charge, we can determine an expression for the charge and thus the gate current. The rationale for dividing that current between the source and drain remains to be determined. Any of three approaches could conceivably be used. We call those approaches *division by charge*, *division by capacitance*, and *division by current*. They are explained below.

A) Division by charge

The most common treatment is to divide the channel charge into a pair of two-terminal charges, $Q_{gs}(V_{gs}, V_{gd})$ and $Q_{gd}(V_{gs}, V_{gd})$. This division, which seems to follow in a straightforward manner from the circuit in Fig. 1, is shown in Fig. 2.

To satisfy (1) we require that

$$Q_g(V_{gs},\ V_{gd}) = Q_{gs}(V_{gs},\ V_{gd}) + Q_{gd}(V_{gs},\ V_{gd}) \tag{2}$$

where, as before, $Q_g(V_{gs}, V_{gd})$ is the total gate charge. In a symmetrical device,

$$Q_{gs}(V_{gs},\ V_{gd}) = Q_{gd}(V_{gd},\ V_{gs}) \tag{3}$$

simplifying the formulation considerably. With this formulation, however, we must use *transcapacitances* in the small-signal, linear equivalent circuit. Specifically, for the gate-to-source current,

$$I_s = -\frac{dQ_{gs}}{dt} = -\left(\frac{dQ_{gs}}{dV_{gs}}\frac{dV_{gs}}{dt} + \frac{dQ_{gs}}{dV_{gd}}\frac{dV_{gd}}{dt}\right) \tag{4}$$

showing that a component of the gate-to-source current I_s results from changes in V_{gd}. This controlled charge source,

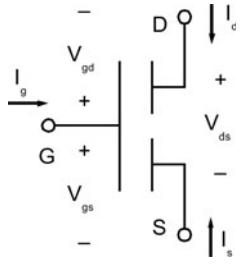


Fig. 1. An FET's intrinsic gate-to-channel capacitance can be viewed as a kind of three-terminal capacitor, where the terminals are those of the FET. Any pair of branch voltages defines the capacitor's charge.

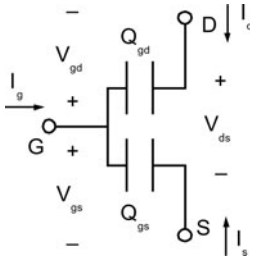


Fig. 2. Division-by-charge formulation: the three-terminal capacitor is represented by two separate nonlinear capacitors.

which depends on a remote voltage, is called a *transcapacitance* [7], analogous to a controlled voltage source or current source. Similarly,

$$I_d = -\frac{dQ_{gd}}{dt} = -\left(\frac{\partial Q_{gd}}{\partial V_{gs}}\frac{dV_{gs}}{dt} + \frac{\partial Q_{gd}}{\partial V_{gd}}\frac{dV_{gd}}{dt}\right) \tag{5}$$

and a component of the gate-to-drain current I_d results from V_{gs}. Thus, if this formulation is used, a small-signal, linear equivalent circuit must have two capacitances and two transcapacitances. Measuring all four capacitances and transcapacitances can become a difficult problem [8, 9]. It is also possible for the individual capacitances to fail to conserve charge, even if the total gate charge is conserved; thus, an additional constraint on the division exists, which is sometimes not respected [3]. Especially problematical is a charge discontinuity occurring when the drain-to-source voltage passes through zero [5]. Even if such difficulties are avoided, the conversion of a single charge region into two has the potential to overcomplicate an otherwise simple situation. We examine these problems further in later sections.

B) Division by capacitance

Given the gate charge, $Q_g(V_{gs}, V_{gd})$, the gate current is

$$I_g = \frac{dQ_g}{dt} = \frac{\partial Q_g}{\partial V_{gs}}\frac{dV_{gs}}{dt} + \frac{\partial Q_g}{\partial V_{gd}}\frac{dV_{gd}}{dt} \tag{6}$$

We hypothesize that

$$I_s = -\frac{\partial Q_g}{\partial V_{gs}}\frac{dV_{gs}}{dt} \tag{7}$$

$$I_d = -\frac{\partial Q_g}{\partial V_{gd}}\frac{dV_{gd}}{dt}$$

which defines two nonlinear capacitances:

$$C_{gs} = \frac{\partial Q_g}{\partial V_{gs}} \tag{8}$$

$$C_{gd} = \frac{\partial Q_g}{\partial V_{gd}}$$

Again, the three-terminal capacitor of Fig. 1 has been divided into two capacitors, in a manner similar to that shown in Fig. 2, but that division is defined by the incremental capacitance, not the large-signal charge. In this case, however, the capacitor currents depend *only on the time derivatives of their own terminal voltages*, and not on changes in any remote voltage. The resulting small-signal equivalent circuit consists, simply, of these capacitances, evaluated at the dc bias voltages. The small-signal circuit is completely consistent with the large signal, and it requires no transcapacitances.

This approach is not convenient for harmonic-balance analysis. In harmonic-balance analysis, it is much more convenient to calculate charge waveforms and to differentiate them in the frequency domain by multiplying by $j\omega$. The simplest way to calculate (7) is to generate the time derivatives by frequency-domain differentiators in the linear subcircuit and

https://doi.org/10.1017/S1759078710000814 Published online by Cambridge University Press

to use the voltage derivatives as the control quantities. This doubles the number of control quantities and, in a naive implementation, causes the Jacobian matrix to become ill-conditioned. To avoid this ill conditioning, and the resulting poor convergence, the voltage derivatives must be scaled smaller and the capacitances larger by a factor approximately equal to the fundamental excitation frequency.

It is important to note that there is no underlying theoretical justification for this formulation. It is largely a conjecture, justified by its intuitive reasonableness and made attractive by its simplicity. Empirical results, including those presented later, indicate that it is indeed valid for many applications. It has been employed in widely used FET models; for example, [10–12].

C) Division by current

A third possibility, introduced in this paper, is to calculate the gate charge and gate current directly, then to use appropriate functions to divide it between the source and drain. Specifically, we use the *division functions* $f_{gs}(V_{gs}, V_{gd})$ and $f_{gd}(V_{gs}, V_{gd})$ in conjunction with the gate charge, $Q_g(V_{gs}, V_{gd})$. Then,

$$I_s = -f_{gs}\frac{dQ_g}{dt} \tag{9}$$

$$I_d = -f_{gd}\frac{dQ_g}{dt}$$

To satisfy Kirchoff's current law, the division functions must have the property

$$f_{gs} + f_{gd} = 1 \tag{10}$$

for all V_{gs} and V_{gd}. In general, f_{gs} approaches unity when $V_{ds} >> 0$. In symmetrical FETs, when $V_{ds} = 0$, $f_{gs} = 0.5$ and with $V_{ds} = V_{gs} - V_{gd}$,

$$f_{gs}(V_{ds}) = f_{gd}(-V_{ds}). \tag{11}$$

An example of a set of division functions meeting these criteria, for a symmetrical FET, is

$$f_{gs}(V_{ds}) = 0.5(1 + g_{odd}(\alpha V_{ds})) \tag{12}$$

$$f_{gd}(V_{ds}) = 0.5(1 + g_{odd}(-\alpha V_{ds}))$$

where α is a constant and $g_{odd}(x)$ is an odd function whose maximum value is 1.0. A promising candidate for $g_{odd}(x)$ might be $tanh(x)$. If the FET is asymmetrical, (10) must still hold, but (11) and (12) in general do not. Although this is an added complication, this idea can be applied to asymmetrical FETs.

The equivalent circuit of this model is shown in Fig. 3.

Q_g is a charge source controlled by V_{gs} and V_{gd}. The source and drain current sources are nonlinear controlled sources, whose controlling quantity is dQ_g/dt and I/V functions are f_{gs} and f_{gd}, respectively.

The use of a single charge source should ease the avoidance of discontinuities caused by a switch in charge ownership at $V_{ds} = 0$. Additionally, with f_{gs} and f_{gd} formulated as in (12), discontinuities in those functions should be easy to avoid as well. Finally, the formulation guarantees consistency between large- and small-signal formulations, charge conservation, and good convergence in simulation, as long as the three functions f_{gs}, f_{gd}, and Q_g are smooth and continuously differentiable throughout the (V_{gs}, V_{gd}) space.

A seeming difficulty of this formulation is the need to evaluate the two-dimensional functions $Q_g(V_{gs}, V_{gd})$ and either $f_{gs}(V_{gs}, V_{gd})$ or $f_{gd}(V_{gs}, V_{gd})$. The nature of the formulation makes this simpler than it at first appears. Fig. 4(a) shows the model, excluding extrinsic elements.

The current source in the gate-to-drain branch can easily be transformed into two sources, one in parallel with the gate-to-source branch and another with the drain-to-source. This is shown in Fig. 4(b). Finally, in Fig. 4(c), the two controlled sources in the gate-to-source branch are simply replaced by the nonlinear gate-charge capacitor. This leaves a controlled source in parallel with the channel, which is easily absorbed into the channel-current function.

Since the division function now appears in only one place, the choice of the function is arbitrary. Any convenient function $f_{gd}(V_{gs}, V_{gd})$ can be used, as long as the total channel current, represented by the combination of the two current sources, is correct. It seems obvious that some forms of f_{gd} would be better than others. While f_{gd} is real, $f_{gd}\, I_g$ introduces a phase shift in the channel current that may be difficult to compensate with the channel current source I_{ch} in a manner that is amenable to use in a circuit simulator. Thus, two branches are likely to be necessary.

D) Small-signal equivalent circuit

The small-signal gate current, i_g, is simply

$$i_g = \frac{dQ_g}{dt} = \frac{\partial Q_g}{\partial V_{gs}}\frac{dv_{gs}}{dt} + \frac{\partial Q_g}{\partial V_{gd}}\frac{dv_{gd}}{dt} \tag{13}$$

where the derivatives are evaluated at the bias point, (V_{gso}, V_{gdo}). From (9), the small-signal reactive drain

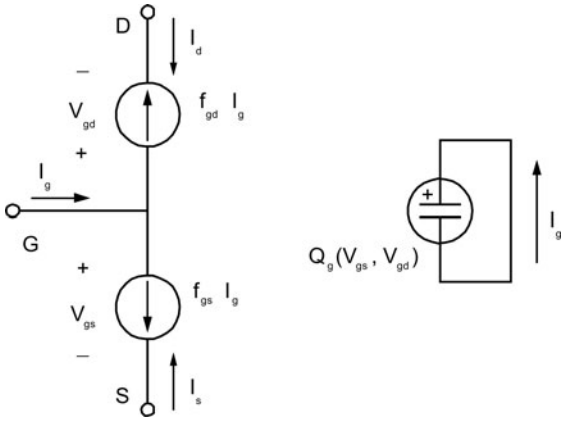


Fig. 3. Large-signal equivalent circuit of a FET's channel capacitance. Q_g is a charge source.

https://doi.org/10.1017/S1759078710000814 Published online by Cambridge University Press

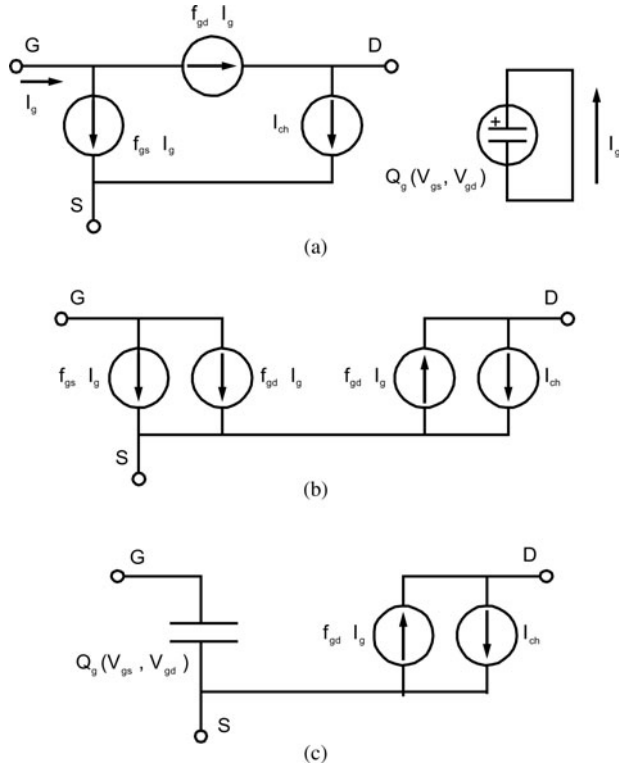


Fig. 4. Transformation of the division-by-current equivalent circuit. (a) Shows the circuit, according to the original concept. In (b), the gate-to-drain current source has been transformed to a pair of shunt sources. In (c), the pair of gate-to-source current sources has been replaced by its equivalent, the gate-charge capacitance. Then, the division function remains only in the drain-to-source branch, where it can be treated simply as part of the channel current.

current, i_d, is

$$i_d = -f_{gd}(V_{gso} + v_{gs}, V_{gdo} + v_{gd})\frac{d}{dt}Q_g(V_{gso} + v_{gs}, V_{gdo} + v_{gd}), \quad v_{gs} << V_{gso},\ v_{gd} << V_{gdo} \tag{14}$$

where v_{gs} and v_{gd} are the small-signal gate-to-source and drain-to-source voltages. Expanding f_{gd} and Q_g in Taylor series' and taking the limit as v_{gs}, v_{gd} approach zero gives the small-signal current,

$$i_d = -f_{gd}(V_{gso}, V_{gdo})\left(\frac{\partial Q_g}{\partial V_{gs}}\frac{dv_{gs}}{dt} + \frac{\partial Q_g}{\partial V_{gd}}\frac{dv_{gd}}{dt}\right) \tag{15}$$

where the derivatives are evaluated at V_{gso} and V_{gdo}.

The equivalent circuit is shown in Fig. 5; it consists of a capacitance and a transcapacitance at the gate side and a controlled source at the drain side. These elements are all easy to characterize from small-signal, Y-parameter measurements.

This circuit is entirely consistent with the large-signal circuit; both the small- and large-signal circuits give identical results as v_{gs} and v_{gd} approach zero.

E) Determination of the Q_g and f_{gd} functions

It is possible to determine the Q_g and f_{gd} functions in a manner that is straightforward and numerically well conditioned. From the small-signal equivalent circuit in Fig. 5, we note that, at low frequencies, the following approximations are valid:

$$\mathrm{Im}\{Y_{12}\} = -\omega\frac{\partial Q_g}{\partial V_{gd}} \tag{16}$$

$$\mathrm{Im}\{Y_{11}\} = \omega\left(\frac{\partial Q_g}{\partial V_{gs}} + \frac{\partial Q_g}{\partial V_{gd}}\right) \tag{17}$$

$$\mathrm{Im}\{Y_{21}\} = -\omega\left(G_m\tau + f_{gd}\left(\frac{\partial Q_g}{\partial V_{gs}} + \frac{\partial Q_g}{\partial V_{gd}}\right)\right) \tag{18}$$

where G_m is the magnitude and τ is the time delay of the transconductance; that is, we assume that the transconductance has the form

$$g_m = G_m \exp(-j\omega\tau) \tag{19}$$

For practical implementation in a nonlinear simulator, it is necessary to assume τ to be constant. From (16) and (17) both $\partial Q_g/dV_{gs}$ and $\partial Q_g/dV_{gd}$ can be determined uniquely, and Q_g can be found by path integration. Finally, f_{gd} and τ can be selected to optimize the fit in (18) to $\mathrm{Im}\{Y_{21}\}$ over the required (V_{gs}, V_{gd}) space.

From (16) to (18), we obtain

$$\frac{dQ_g}{dV_{gd}} = -\frac{\mathrm{Im}\{Y_{12}\}}{\omega} \tag{20}$$

$$\frac{dQ_g}{dV_{gs}} = \frac{1}{\omega}(\mathrm{Im}\{Y_{11}\} + \mathrm{Im}\{Y_{12}\}) \tag{21}$$

$$f_{gd} = -\left(\frac{\mathrm{Im}\{Y_{21}\} + \omega G_m\tau}{\mathrm{Im}\{Y_{11}\}}\right) \tag{22}$$

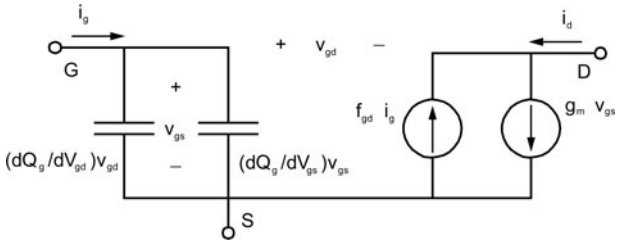


Fig. 5. Small-signal equivalent circuit derived from the large-signal equivalent circuit in Fig. 4(c).

https://doi.org/10.1017/S1759078710000814 Published online by Cambridge University Press

F) Determination of Q_g from small-signal measurements

Given a general nonlinear charge function $Q(V_1, V_2)$ we define the incremental capacitances:

$$C_1(V_1, V_2) = \frac{\partial Q}{\partial V_1} \tag{23}$$

$$C_2(V_1, V_2) = \frac{\partial Q}{\partial V_2}$$

The small-signal reactive current $i_Q(t)$ is found from small-signal voltages $v_1(t)$ and $v_2(t)$ as

$$\begin{aligned} i_Q(t) &= \frac{\partial Q}{dV_1}\frac{dv_1}{dt} + \frac{\partial Q}{dV_2}\frac{dv_2}{dt} \\ &= C_1(V_{10}, V_{20})\frac{dv_1}{dt} + C_2(V_{10}, V_{20})\frac{dv_2}{dt} \end{aligned} \tag{24}$$

where V_{10} and V_{20} are bias values. Clearly, C_1 can be found by setting $v_2 = 0$ and measuring the admittance I_1/V_1 and C_2 similarly. Then Q is found by path integration:

$$\begin{aligned} Q(V_1, V_2) = &\int_{V_{2,0}}^{V_2} C_2(V_{1,0}, v_2)\, dv_2 \\ &+ \int_{V_{1,0}}^{V_1} C_1(v_{1,0}, V_2)\, dv_1 + Q(V_{1,0}, V_{2,0}) \end{aligned} \tag{25}$$

$Q(V_{1,0}, V_{2,0})$ can be set to any convenient value, usually zero, as constant charge does not affect the current in the capacitor. The path of integration is shown in Fig. 6.

In the case of FETs, V_1 represents the V_{gs} axis and V_2 the V_{gd}. In theory, at least one integration in the V_{gd} direction is necessary; however, if the initial point V_{gs},0 is chosen well below pinch-off, there may be little charge variation with V_{gd}, so the integration in that direction can be eliminated.

This process is applicable to all capacitance formulations. In division by charge, the two capacitances are treated separately. For the gate-to-source capacitance, $C_1 \equiv \partial Q_{gs}/dV_{gs}$ and $C_2 \equiv \partial Q_{gs}/dV_{gd}$; the gate-to-drain capacitance, Q_{gd}, is treated similarly. In division by current or capacitance, the gate charge is determined directly, so $C_1 \equiv \partial Q_g/dV_{gs}$ and $C_1 \equiv \partial Q_g/dV_{gd}$.

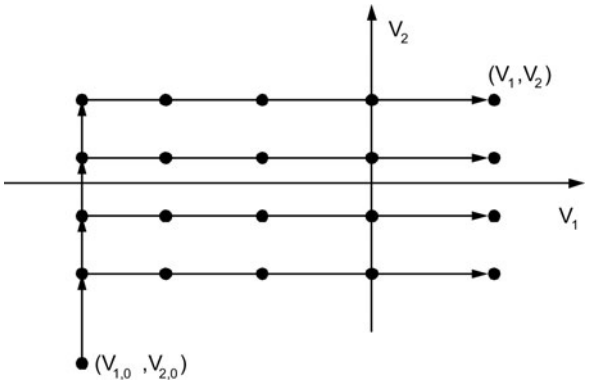


Fig. 6. Values of charge are found by path integration of the capacitance in the (V_1, V_2) plane as indicated. As long as the model is charge conservative, any path may be used, although for practical reasons integrating along the axes is preferred.

G) Definition of the (V_{gs}, V_{gd}) space

It is worthwhile to note that a large range of the (V_{gs}, V_{gd}) space need not be mapped. In Fig. 7, we have plotted the FET's I/V plane in a somewhat different form from the usual; that is, we plot V_{gs} versus V_{gd}. This results in lines of constant V_{ds}. The figure indicates the (V_{gs}, V_{gd}) space that must be considered. It is clear that a large area is not accessible, as it is limited by turn-on of the gate Schottky junction. Conversely, at voltages well below pinch-off, the gate charge varies only weakly, and linear, intermetallic capacitances dominate. Voltages above some power-dissipation limit need not be mapped, as continued operation in that region damages the device. Finally, if the device is symmetrical, only half of the accessible space (the region below the $V_{ds} = 0$ contour) need be mapped.

For this reason, it is generally not possible to perform the contour integration as simply as is implied in Fig. 7. Invariably, multiple integration steps are necessary. Fortunately, this exercise is necessary only for determining the form of the Q_g and f_{gd} equations; once those are determined, parameters can be found by fitting to the capacitance functions, obtained by differentiating Q_g, rather than the charge function.

III. CHARGE CONSERVATION

Much has been written about charge conservation in FETs, and a great deal of that material has been misleading. The requirement is often stated as

$$\frac{\partial C_{gs}}{dV_{gd}} = \frac{\partial C_{gd}}{dV_{gs}} \tag{26}$$

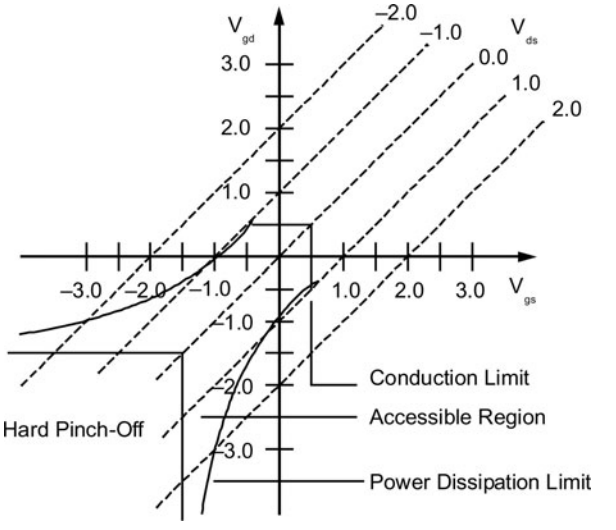


Fig. 7. This figure illustrates the area of the (V_{gs}, V_{gd}) space that must be mapped, for a hypothetical device having approximately −1.0 V pinch-off. This is called the *accessible region*. Contours of constant V_{ds} are shown as well. The accessible region is within the limits established by power dissipation, gate-to-channel conduction, and hard pinch-off. Furthermore, if the device is symmetrical, only the accessible region below the $V_{ds} = 0$ contour must be mapped; the rest can be determined by symmetry.

https://doi.org/10.1017/S1759078710000814 Published online by Cambridge University Press

without a clear indication of the definitions of C_{gs} and C_{gd}. Frequently, it is assumed that these are the primary capacitances from a division-by-charge formulation; that is,

$$C_{gs} = \frac{\partial Q_{gs}}{\partial V_{gs}}, \quad C_{gd} = \frac{\partial Q_{gd}}{\partial V_{gd}} \tag{27}$$

This criterion guarantees charge conservation for the total gate charge when $C_{gs} = \partial Q_g / dV_{gs}$ and $C_{gd} = \partial Q_g / dV_{gd}$ but not for the individual charges Q_{gs} and Q_{gd}. As such, this could be called a *weak criterion* for charge conservation. Conservation of the individual charges is also necessary. The criterion for charge conservation in both formulations, which we shall call the *strong criterion*, is given below.

A) Division by charge

The conditions for charge conservation apply to a *single* charge source controlled by two (or more) voltages. It simply states that any change in charge is completely defined by the initial and final values of the control voltages, independent of the path taken by those voltages. For this to be the case, it is necessary and sufficient that its derivatives be continuous throughout the (V_{gs}, V_{gd}) space. Functions that are continuous and infinitely differentiable throughout a specified space are called *analytic* within that space. The charge functions we consider here need not be strictly analytic; continuity through the second derivative is sufficient. Thus, in the case of division by charge, the requirement for charge continuity, similar to (26), should be stated as

$$\frac{\partial C_{gs}}{dV_{gd}} = \frac{\partial C_{gsm}}{dV_{gs}} \tag{28}$$

where

$$C_{gs} = \frac{\partial Q_{gs}}{\partial V_{gs}}, \quad C_{gsm} = \frac{\partial Q_{gs}}{\partial V_{gd}} \tag{29}$$

and similarly for Q_{gd}. Then, both sides of (28) become

$$\frac{\partial^2 Q_{gs}}{\partial V_{gs} \partial V_{gd}} \tag{30}$$

We shall call this the *strong criterion* for charge conservation. Any ordinary algebraic expression satisfies this property.

It should be obvious that charge conservation in the individual gate-to-source and gate-to-drain charge elements guarantees charge conservation for the total gate charge $Q_{gs} + Q_{gd}$. Thus, this strong criterion satisfies the weak criterion in all cases. The weak criterion simply states, for the total gate charge,

$$\frac{\partial C_{gs}}{\partial V_{gd}} + \frac{\partial C_{gdm}}{\partial V_{gd}} = \frac{\partial C_{gsm}}{\partial V_{gs}} + \frac{\partial C_{gd}}{\partial V_{gs}} \tag{31}$$

This has little practical value, however, and does not guarantee charge conservation for the individual Q_{gs} and Q_{gd} charge functions.

Charge nonconservation is strong evidence of model invalidity, as real capacitors always conserve charge. Additionally, it creates practical difficulties in circuit simulation. Time-domain simulators sometimes carry capacitor charge as a variable, and if a capacitor does not conserve charge, numerical overflow quickly occurs. In harmonic-balance simulation, the existence of a finite charge difference between the beginning and end of a waveform period results in the appearance of dc current in the capacitor. If the weak criterion, but not the strong, is satisfied, no dc gate current is created, but dc currents in the individual gate-to-source and gate-to-drain capacitances are possible. Satisfying the strong criterion prevents this.

B) Division by current

The division-by-current formulation is based on a single charge function, so charge conservation requires only that the function satisfies the fundamental requirement,

$$\frac{\partial}{\partial V_{gs}}\left(\frac{\partial Q_g}{\partial V_{gd}}\right) = \frac{\partial}{\partial V_{gd}}\left(\frac{\partial Q_g}{\partial V_{gs}}\right) \tag{32}$$

throughout the entire (V_{gs}, V_{gd}) region.

For a number of mostly obvious reasons, f_{gs} and f_{gd} should also have continuous derivatives throughout this region as well. As long as Kirchoff's current law is satisfied, however, discontinuities in the f_{gs} and f_{gd} functions do not affect charge conservation.

C) Division by capacitance

Since this formulation does not generate transcapacitances, (32) applies directly to division by capacitance. Satisfying (32) prevents charge nonconservation in division-by-capacitance models.

IV. THE "CHARGE OWNERSHIP" PROBLEM

Charge nonconservation is likely to occur in division-by-charge models when V_{ds}(t) passes through zero. In most model formulations, the Q_{gd} and Q_{gs} charge functions are interchanged, as are their control voltages, when V_{ds} changes its sign.

The case is made in [4] that, as the $V_{ds}(t)$ passes through zero, Q_{gs} and Q_{gd} are interchanged. The change in "charge ownership" by the gate-to-source and gate-to-drain capacitances results in nonconservation of the individual charges. This point is illustrated by tracing the FET charge through a closed path in the (V_{gs}, V_{gd}) plane, including the $V_{ds} = 0$ point. The example shows that, while total gate charge is conserved, the individual charges are not.

If the charge functions are individually conservative (i.e., in the strong sense) and the device is symmetrical, $Q_{gs} = Q_{gd}$ at $V_{ds} = 0$ of necessity. Then, a change in charge ownership does not affect the drain or source currents. Discontinuities in the derivatives of these functions at $V_{ds} = 0$ are still possible, however, and may be subtle. Such difficulties still may lead to convergence failure in harmonic-balance analysis.

A lack of appreciation of this point has resulted in model behavior that is not physically correct. An example is the widely used BSIM3 model for MOSFETs [5]. This model treats the gate charge as a single element, but then employs

https://doi.org/10.1017/S1759078710000814 Published online by Cambridge University Press

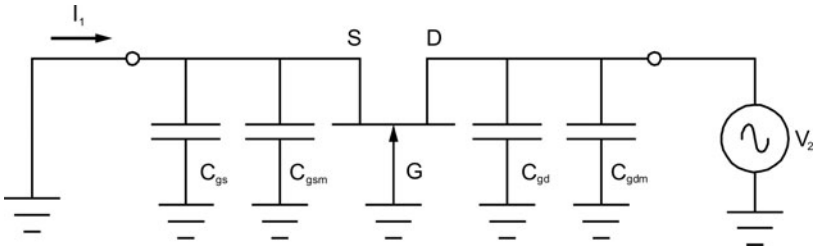


Fig. 8. Dependence of i_s on v_{gd} or i_d on v_{gs} can be determined from Y-parameter measurements of the device in common-gate configuration.

a clumsy technique for partitioning it between the drain and source. Documentation for the model frankly admits that some of the partitioning methods result in nonphysical drain- and source-current impulses occurring as $V_{ds}(t)$ passes through zero. This is a strong indication of a charge-ownership problem.

V. VALIDITY OF DIVISION BY CAPACITANCE

We noted that the division by capacitance approach is based on the hypothesis in (7). It seems likely to be valid when the device is in current saturation, as C_{gd} is dominated by intermetallic capacitances and shows little variation with V_{gd}. In the device's linear region, however, it is not at all clear that this hypothesis is valid; thus, measurements on the device in that region should clarify the matter.

Consider the device in a common-gate configuration, as shown in Fig. 8, with C_{ds} and all terminal parasitics removed. We evaluate the device at $V_{ds} = 0$, which is likely to be the worst case.

In this case, if the small-signal i_s varies with v_{gd}, indicated by a nonzero value of Y_{12}, a transcapacitance, C_{gsm} in the figure, must exist.

Figure 9 shows measured values of Y parameters of a small-signal HEMT, a Triquint foundry device, biased at $V_{ds} = 0$. At values of V_{gs} close to zero, there is a clear indication of a transcapacitive effect in Y_{12}. As V_{gs} becomes more negative, however, but still remains above the threshold voltage, the effect disappears quickly. Further measurements show that it disappears rapidly with V_{ds} as well. It appears that the division by capacitance approach may be useful for circuits in which the device remains in saturation, or dips only lightly into its linear region. If the device is operated primarily in its linear region, as is the case in switches and FET resistive mixers, this approach to modeling probably is not useful.

VI. EQUIVALENCES IN THE FORMULATIONS

All formulations are equivalent, in the sense that they derive from a single gate charge, $Q_g(V_{gs}, V_{gd})$. In division by charge, this quantity is divided into two charges, Q_{gs} and Q_{gd}, where $Q_g = Q_{gs} + Q_{gd}$, whose derivatives define the source and drain reactive currents. In division by capacitance, the partial derivatives of $Q_g(V_{gs}, V_{gd})$ define those currents, while in division by current, they are split by a pair of separate functions, $f_{gs}(V_{gs}, V_{gd})$ and $f_{gd}(V_{gs}, V_{gd})$.

A) Division by charge and division by current

Equivalence between division by charge and division by current can be shown as follows. We consider the case of the gate-to-source current; the drain current follows by analogy. The current is

$$I_s = -f_{gs}\frac{dQ_g}{dt} = -f_{gs}\left(\frac{dQ_{gs}}{dt} + \frac{dQ_{gd}}{dt}\right) \tag{33}$$

Straightforward algebraic manipulation gives

$$f_{gs} = \frac{\partial Q_{gs}/\partial V_{gs}}{\partial Q_g/\partial V_{gs}} \tag{34}$$

showing that $f_{gs}(V_{gs}, V_{gd})$ and, therefore, $f_{gd}(V_{gs}, V_{gd})$ can be derived directly from terms of the division-by-charge formulation. This implies that

$$f_{gs}\frac{\partial Q_g}{\partial V_{gs}} = \frac{\partial Q_{gs}}{\partial V_{gs}} \tag{35}$$

which is the definition of the capacitance C_{gs} in both the division-by-current and division-by-charge small-signal equivalent circuits.

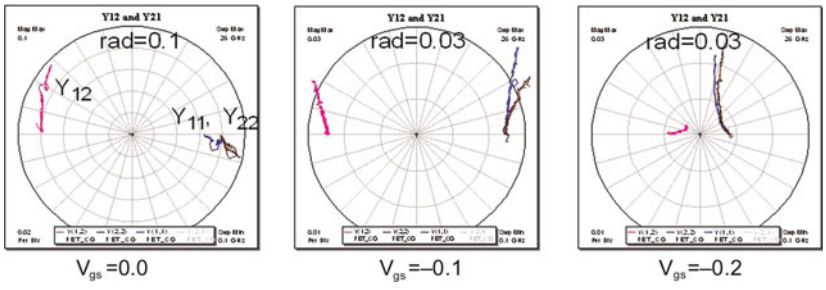


Fig. 9. Measurements of Y parameters at $V_{ds} = 0$ and various values of V_{gs}. The positive imaginary part of Y_{12} is a clear indication of a transcapacitance. Note that at $V_{ds} = 0$, $Y_{12} = Y_{21}$. The frequency range is 0.1–26 GHz.

https://doi.org/10.1017/S1759078710000814 Published online by Cambridge University Press

Since these two approaches can be equated algebraically, one can legitimately question the need for the division-by-current formulation. That formulation has the advantage of helping to avoid many of the previously described pitfalls in FET modeling. In addition, it has significant advantages in numerical conditioning in parameter extraction and in its implementation in a simulator.

B) Division by charge and division by capacitance

Again, for simplicity we consider the gate-to-source current. For the division-by-charge case, we have

$$I_s = -\frac{dQ_{gs}}{dt} = \frac{dQ_{gs}}{dV_{gs}}\frac{dV_{gs}}{dt} + \frac{dQ_{gs}}{dV_{gd}}\frac{dV_{gd}}{dt} \tag{36}$$

For the division-by-capacitance case,

$$I_s = -\frac{dQ_g}{dV_{gs}}\frac{dV_{gs}}{dt} \tag{37}$$

In (36) the current is a function of the V_{gs} and V_{gd} time derivatives, while in (37) it is a function of the V_{gs} derivative only. Since V_{gs} and V_{gd} are independent quantities, it is clearly impossible to equate the two approaches.

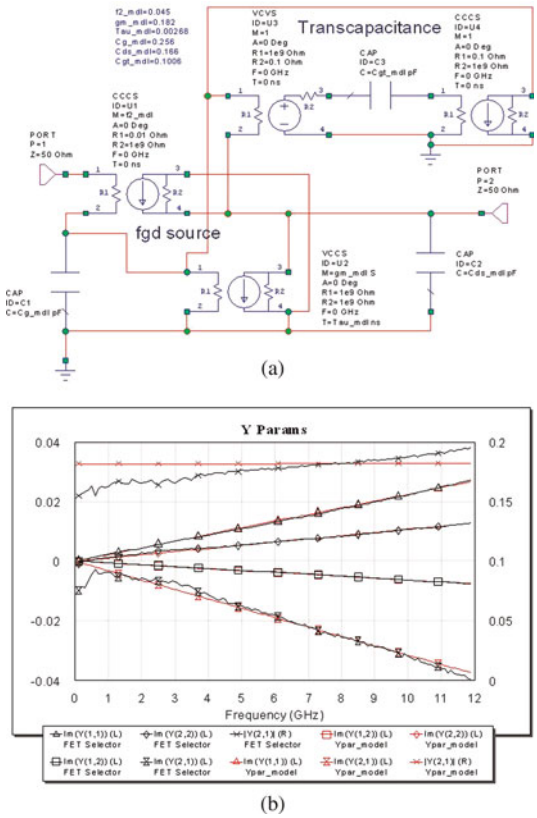


Fig. 10. Small-signal equivalent circuit (a) and *Y*-parameter fitting (b) of the model.

VII. PARAMETER EXTRACTION

From an analysis of Fig. 5 we obtain

$$\mathrm{Im}\{Y_{12}\} = -\omega\frac{dQ_g}{dV_{gd}} \tag{38}$$

$$\mathrm{Im}\{Y_{11}\} = -\omega\left(\frac{dQ_g}{dV_{gs}} + \frac{dQ_g}{dV_{gd}}\right) \tag{39}$$

$$\mathrm{Im}\{Y_{21}\} = -\omega\left(G_m\tau + f_{gd}\left(\frac{dQ_g}{dV_{gs}} + \frac{dQ_g}{dV_{gd}}\right)\right) \tag{40}$$

From these, the derivatives of the charge are determined unequivocally, and the charge function is found by path integration. An appropriate value for τ is selected and f_{gd} determined accordingly. Finally, f_{gs} is found from (10). Drain-to-source capacitance C_{ds} is found from Y_{22}. Since these quantities are determined from low-frequency measurements, parasitic inductance, and series resistance affect the extraction minimally. In any case, these can be removed by well-known means [15–18].

Figure 10(a) shows the small-signal circuit as implemented in a circuit simulator, and Fig. 10(b) shows the results of fitting to *Y* parameters of a Triquint foundry device, at moderate frequencies. The f_{gd} function behaved as expected, and a constant value of τ fit the data accurately.

VIII. CONCLUSIONS

We have shown that existing FET capacitance formulations are based on one of two fundamental approaches, which we call *division by capacitance* and *division by charge*. We have additionally proposed a third formulation, called *division by current*, which has significant advantages compared to the former two.

One central purpose of this study was to introduce the division-by-current formulation and to compare it to the others. It was determined that this formulation is practical, and it has significant advantages in parameter extraction and, perhaps, simulation efficiency and numerical conditioning. As it can be made equivalent to the division-by-charge formulation, it has many identical properties.

We have also examined a number of matters regarding these formulations, which, in our view, either have never been clearly addressed in the literature or are frequently confused. Finally, we have evaluated the characteristics, validity, and practicality of the three formulations. We found that the division-by-charge and division-by-current formulations are quite general. The division-by-capacitance approach, however, may be invalid for resistive FET applications.

ACKNOWLEDGEMENTS

This work was supported by Ericsson AB and Chalmers University of Technology, Göteborg, Sweden.

https://doi.org/10.1017/S1759078710000814 Published online by Cambridge University Press

REFERENCES

[1] Root, D.E.: Nonlinear charge modeling for FET large-signal simulation and its importance for IP3 and ACPR in communication circuits, in Proc. 44th IEEE 2001 Midwest Symp. Circuits and Systems, vol. 2, 2001, 768.

[2] Statz, H.; Newman, P.; Smith, I.; Pucel, R.; Haus, H.: GaAs FET device and circuit simulation in SPICE. IEEE Trans. Electron Devices, **ED-34** (2) (1987), 160.

[3] Divekar, D.: Comments on GaAs FET device and circuit simulation in SPICE. IEEE Trans. Electron Devices, **ED-34** (12) (1987), 2564.

[4] Statz, H.; Newman, P.; Smith, I.; Pucel, R.; Haus, H.: On charge non-conservation in FET's. IEEE Trans. Electron Devices, **ED-34** (12) (1987), 2565.

[5] Cheng, Y.; Hu, C.: MOSFET Modeling and BSIM3 User's Guide, Kluwer, Boston, 1999.

[6] Yang, P.; Epler, B.; Chatterjee, P.: An investigation of the charge conservation problem for MOSFET circuit simulation. IEEE J. Solid-State Circuits, **SC-18** (1) (1983), 128.

[7] Snider, A.D.: Charge conservation and the transcapacitance element. IEEE Trans. Educ., **38** (1995), 376.

[8] Struble, W. et al.: A new small signal MESFET and HEMT model compatible with large signal modeling, in IEEE MTS 1994 Int. Microwave Symp. Digest, 1994, 1567.

[9] Scheinberg, N.; Chisholm, E.: A capacitance model for GaAs MESFET's. IEEE J. Solid-State Circuits, **26** (10) (1991), 1467.

[10] Parker, A.E.; Skellern, D.J.: A realistic large signal MESFET model for spice. IEEE Trans. Microw. Theory Tech., 45 (9) (1997), 1463.

[11] Wren, M.; Brazil, T.J.: Enhanced prediction of pHEMT nonlinear distortion using a novel charge conservative model, in IEEE MTS 2004 Int. Microwave Symp. Digest, 2004, 31.

[12] Hallgren, R.B.; Litzenberg, P.H.: TOM3 capacitance model: linking large- and small-signal MESFET models in SPICE. IEEE Trans. Microwave Theory Tech., **47** (5) (1999), 556.

[13] Rorsman, N.; Garcia, M.; Karlsson, C.; Zirath, H.: Accurate small-signal modeling of HFETs for millimeter-wave application. IEEE Trans. Microwave Theory Tech., **44** (4) (1996), 432.

[14] Dambrine, G.; Cappy, A.; Heliodore, F.; Playez, E.: A new method for determining the FET small- signal equivalent circuit. IEEE Trans. Microwave Theory Tech., **36** (1988), 1151.

[15] Parker, A.E.; Mahon, S.J.: Robust extraction of access elements for broadband small-signal FET models, in IEEE MTS 2007 Int. Microwave Symp. Digest, 2007, 783.

[16] Berroth, M.; Bosch, R.: Broad-band determination of the FET small-signal equivalent circuit. IEEE Trans. Microwave Theory Tech., **38** (1990), 891.

[17] Divekar, D.A.: FET Modeling for Circuit Simulation, Kluwer, Boston, 1988.

[18] Aaen, P.; Bridges, D.; Pla, J.A.; Wood, J.: Modeling and Characterization of RF and Microwave Power FETS, Cambridge University Press, Cambridge, UK, 2007.



Stephen Maas received BSEE and MSEE degrees in Electrical Engineering from the University of Pennsylvania in 1971 and 1972, respectively, and a Ph. D. in Electrical Engineering from UCLA in 1984. He has been involved in research, design, and development of low-noise and nonlinear microwave circuits and systems at the National Radio Astronomy Observatory (where he designed the receivers for the Very Large Array), Hughes Aircraft Co., TRW, the Aerospace Corp., and the UCLA Department of Electrical Engineering. Subsequently he worked as an engineering consultant and founded Nonlinear Technologies, Inc., a consulting company, in 1993. He is currently Chief Scientist of AWR, Inc.

Dr. Maas is the author of Microwave Mixers (Artech House, 1986 and 1992), Nonlinear Microwave Circuits (Artech House, 1988; second edition 2003), The RF and Microwave Circuit Design Cookbook (Artech House, 1998), and Noise in Linear and Nonlinear Circuits (Artech House, 2005). From 1990 until 1992 he was the editor of the IEEE Transactions on Microwave Theory and Techniques and from 1990–93 was an Adcom member and Publications Chairman of the IEEE MTT Society. He received the Microwave Prize in 1989 for his work on distortion in diode mixers and the MTT Application Award in 2002. He is a Fellow of the IEEE.

https://doi.org/10.1017/S1759078710000814 Published online by Cambridge University Press