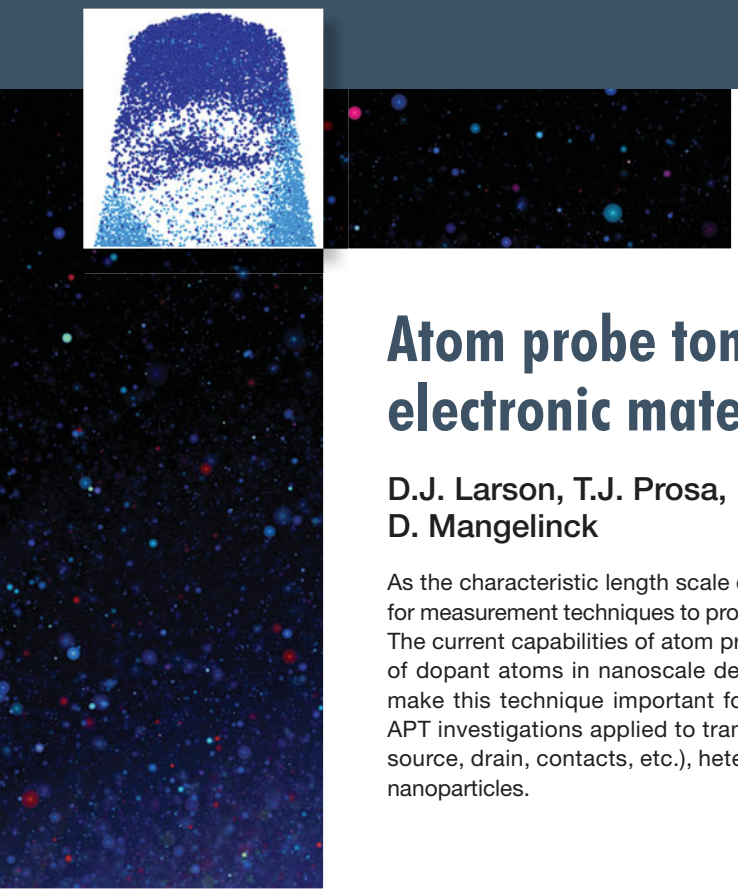


Atom probe tomography of nanoscale electronic materials

D.J. Larson, T.J. Prosa, D.E. Perea, K. Inoue, and D. Mangelinck

As the characteristic length scale of electronic devices shrinks, so does the required scale for measurement techniques to provide useful feedback during development and fabrication. The current capabilities of atom probe tomography (APT), such as detecting a low number of dopant atoms in nanoscale devices or studying diffusion effects in a nanowire (NW), make this technique important for metrology on the nanoscale. Here we review recent APT investigations applied to transistors (including regions such as gate oxide, channel, source, drain, contacts, etc.), heterogeneous dopant incorporation in NWs, and Pt-based nanoparticles.

Introduction

Over the past decade, integrated circuit and device technology has become reliant on advanced materials and complicated three-dimensional (3D) structures that continue to shrink in size and grow in complexity (a trend that is expected to continue for years).[1] Characteristic feature sizes in metal oxide semiconductor field-effect transistors (MOSFETs) commonly used in microelectronics continue to shrink in accordance with Moore's Law, and the functional properties of the MOSFETs depend on structure, elemental distribution, and interface roughness among other factors, at the nanometer or even the subnanometer scale. The distribution of just a few individual atoms, for instance, near the gate in a fin-shaped FET (finFET)[2] or adjacent to a strained SiGe layer often determines the performance of individual devices. As such, optimal metrology methods are needed to routinely measure (in three dimensions) near and at the atomic scale.[3] Lord Kelvin succinctly summarized the idea behind this characterization goal, "If you cannot measure it, you cannot improve it."[4]

Atom probe tomography (APT) is a mass spectrometry technique based on time-of-flight measurements that also concurrently yields 3D spatial information (see the introductory article in this issue).[5–9] Current capabilities of APT, such as detecting a low number of dopant atoms in nanoscale devices or measuring segregation at a nanoparticle interface, make this technique an important component of nanoscale metrology. In this article, we briefly review some applications of APT to nanoscale electronic materials, including transistors and finFETs, silicide contact microstructures, nanowires (NWs), and Pt nanoparticles.

Transistors and finFETs

One strength of APT is its ability to identify dopant distributions within single devices in 3D. Because device performance is directly influenced by dopant homogeneity, the ability to quantify and statistically evaluate dopant distributions provides an important dimension to device characterization. For example, **Figure 1**a shows cross-sectional 3D atom maps of *n*- and *p*-type MOSFET specimens from 65-nm technology.[10,11] This MOSFET was fabricated using the following sequence. After dopants were implanted into the channel region, the gate-oxide film and doped poly-Si gate were formed. The sample was then patterned and etched by conventional lithography and dry etching. After etching, As and B atoms were implanted for a source–drain extension (SDE) in *n*- and *p*-type MOSFETs, respectively.[10]

Phosphorus dopants in the *n*-MOSFET segregate to grain boundaries in the poly-Si gate (left),[12] while B dopants in the

D.J. Larson, CAMECA Instruments, Inc., USA; david.larson@ametek.com
T.J. Prosa, CAMECA Instruments, Inc., USA; ty.prosa@ametek.com
D.E. Perea, Environmental Molecular Science Laboratory, Pacific Northwest National Laboratory, USA; daniel.perea@pnnl.gov
K. Inoue, Institute for Materials Research, Tohoku University, Japan; kinoue@imr.tohoku.ac.jp
D. Mangelinck, Institute Materials Microelectronics Nanosciences of Provence, National Center for Scientific Research/Aix-Marseille University, France; dominique.mangelinck@im2np.fr
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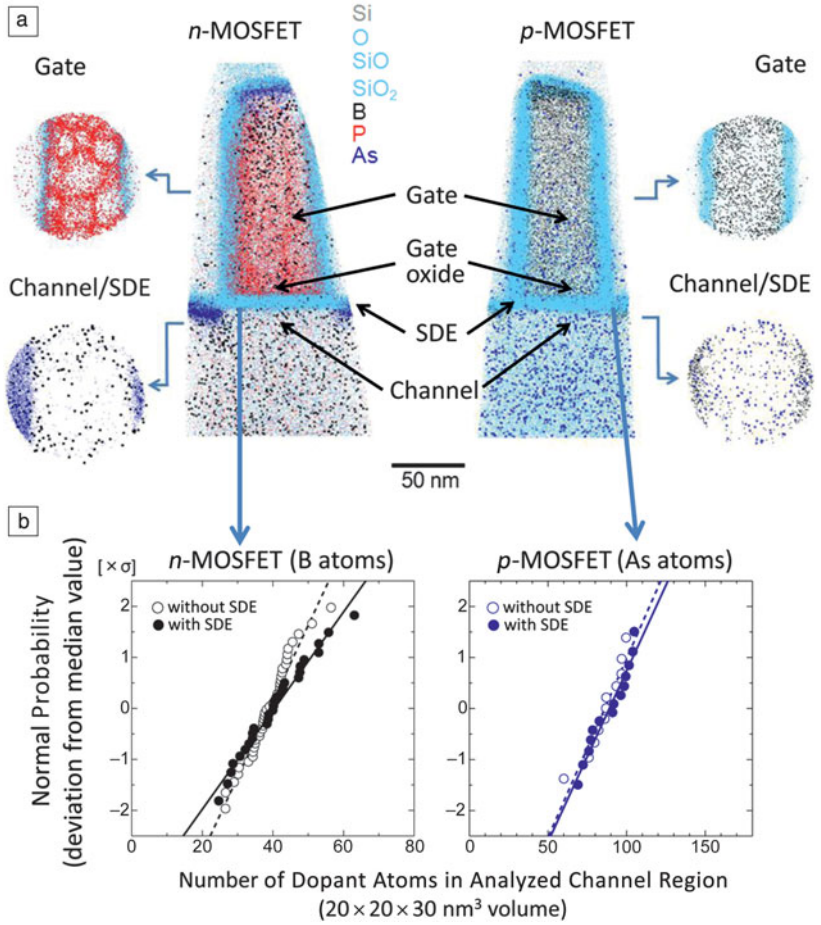


Figure 1. Atom probe tomography (APT) maps of *n*- and *p*-MOSFETs (metal oxide semiconductor field-effect transistors): (a) (Center) Three-dimensional APT atom maps are displayed as extracted two-dimensional (2D) thin cross sections, revealing the overall MOSFET structures, poly-Si gate, gate oxide, channel, and source–drain extension (SDE). Individual dopant atoms are shown: P in the poly-Si gate; As in the SDE; B in the channel, the poly-Si gate, and the SDE in the *n*-MOSFET; As is the channel in the *p*-MOSFET. (Outside) Extracted and rotated 2D atom maps of the gate and channel/SDE regions. Adapted with permission from Reference 10. © 2009 Elsevier. (b) Normal probability plots of the number of dopants in the channel region (σ is one standard deviation, solid lines with SDE, dashed lines without SDE). The slope in the probability plot is equal to the distribution width, with a steeper slope indicating a smaller dopant fluctuation. The fluctuation in B atoms in the channel region increases after the SDE formation, while the As distribution remains unchanged. Adapted with permission from Reference 13. © 2011 AIP Publishing LLC.

p-MOSFET are almost uniformly distributed (right). Dopants in the channel regions underneath the gate oxide and on both sides of the SDE can also be characterized. By comparing the dopant distribution with and without SDEs, as shown in Figure 1b, B atoms in the channel region of *n*-MOSFETs are seen to fluctuate away from a random distribution due to SDE formation by ion implantation. In contrast, the distribution of As atoms in the channel region of *p*-MOSFETs is not changed by SDE formation and is almost random.[13] These results help explain differences in variability of the device threshold voltage. To better correlate performance with dopant distribution, direct measurements of *n*-MOSFET threshold voltages and channel dopant concentrations have been made from a number of transistors extracted from a single chip, using individual transistor threshold voltages within ±4σ of the overall mean.[14] A positive correlation between threshold voltage and channel B concentration (for the 30-nm-deep region just below the gate oxide) was found. This result demonstrates that APT is a potentially powerful tool for individual device failure analysis.

Other APT application areas for electronics materials include high-κ gate dielectrics (κ is the dielectric constant) and finFETs. In high-κ gate materials, a dielectric material with higher dielectric permittivity (such as HfO_2 or ZrO_2) is used to replace the SiO_2. Atom probe tomography can reveal the chemical composition in the high-κ gate dielectrics, and thus, stoichiometry or chemical diffusion with adjacent layers can be correlated with the threshold voltage.[15] Characterization of the elemental distribution within nanoscale oxides is particularly important to manage gate leakage current.[15–18]

FinFETs represent the modern multigate device in which the channel is surrounded by a gate on multiple surfaces.[2] This complicated device morphology makes finFETs especially difficult to characterize at the nanoscale. Several APT analyses of finFET dopant distributions have been reported.[15,19–25] These analyses consider dopant distribution in depth and lateral dimensions of the fin, and reveal dependencies on ion-implantation angle[20] and doping method.[19,21]

Microstructure in silicide contacts

One of the challenges of nanoelectronics is to create contacts on the active zones of transistors. Starting with the 65-nm technology node, NiSi has been the preferred material for contacts in microelectronics due to its low resistivity, resistance to degradation with increasing temperature, and low Si consumption.[26] The addition of a small amount of Pt (typically 5–10 at.%) to a Ni film stabilizes the NiSi phase at high temperatures through an increase of the $NiSi_2$ formation temperature[27] and better resistance to morphological degradation.[28] APT enables characterization of dopant and alloying elements at the scale necessary for providing insight into formation and redistribution mechanisms for thin-film silicide contacts.

Figure 2a–b shows two 20-nm-thick slices of a 50-nm Ni-5 at.% Pt film on Si(100) annealed for 1 h at 300°C. Ni, Si, and Pt atoms are represented as green, red, and blue dots, respectively.[29] From the APT composition measurements, three regions were identified in addition to the Si substrate: (1) the unreacted Ni(Pt) film; (2) the δ-Ni_2Si phase with a thickness of approximately 60 nm; and (3) the NiSi phase that forms

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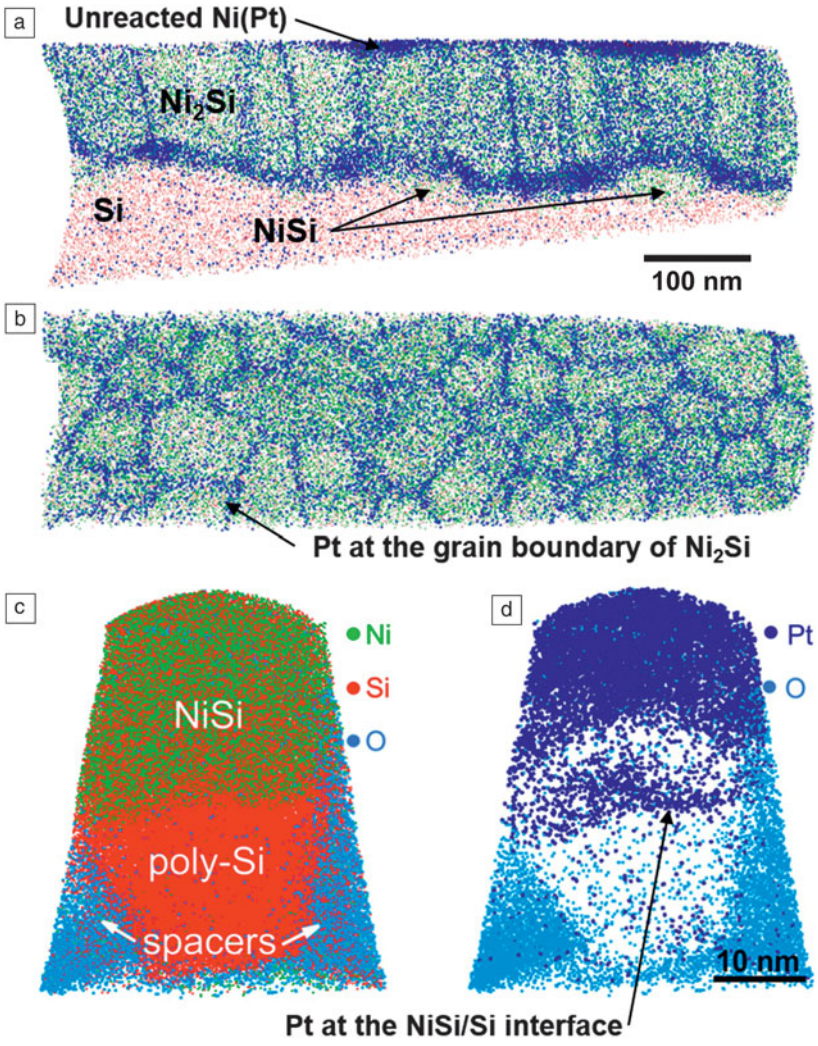


Figure 2. Atom probe tomography maps of a Ni-(5 at.% Pt)Si film (a) and (b) and *n*-MOS gate (c) and (d). (a) 20-nm-thick slice showing the different phases: Ni(Pt), δ-Ni_2Si, NiSi, and Si; (b) 20-nm slice in-depth through the δ-Ni_2Si region showing the grain-boundary enrichment of Pt; (c) *n*-MOS gate showing NiSi, poly-Si, and spacers; and (d) *n*-MOS gate with only O and Pt atoms displayed. Adapted with permission from Reference 29. © 2010 Elsevier and Reference 31. © 2011 AIP Publishing.

large islands at the δ-Ni_2Si/Si interface. As shown in Figure 2a, Pt atoms are present in all phases, but they are distributed in contrasting ways. A high concentration of Pt is found in the Ni(Pt) layer as a result of reactive diffusion.[30] In the δ-Ni_2Si phase, Pt is preferentially present at the grain boundaries, revealing the columnar structure of the δ-Ni_2Si phase, see Figure 2b. The NiSi phase is located between the δ-Ni_2Si phase and the Si substrate as large islands: Pt atoms accumulate at the δ-Ni_2Si/Si and NiSi/Si interface, but they are not incorporated into the NiSi grains. This accurate knowledge of the location and concentration of Pt atoms allows for a better understanding of the effect of this alloying element on nickel silicide formation.[30]

In microelectronic devices, the presence of stress, defects, and spatial confinement may have an effect on the silicide formation mechanism, as well as on the alloying element and dopant redistribution and segregation. Figure 2c–d shows APT analysis of a 28-nm *n*-MOS transistor gate fabricated with the standard process flow of 300-mm production wafers.[31] Nickel silicide contacts were formed from a 15-nm Ni-10 at.% Pt film by a standard Self ALIgned siliCIDE (SALICIDE) process[32] with two rapid thermal steps—annealing at 280°C and 390°C—separated by selective etching.

Four distinct regions (Ni[Pt]Si, poly-Si, and the two Si oxide spacers) can be observed in Figure 2c. Platinum (Figure 2d) and As (not shown) accumulate at the NiSi/Si interface (not shown), and neither is homogeneously distributed in the NiSi contact. Pt is mainly present in the upper part of the silicide, and there is a Pt concentration gradient within the NiSi phase (decreasing from the surface to the poly-Si gate).[31] The Pt distribution in the final Ni[Pt]Si is different from that previously reported in the literature.[27] Complementary analysis performed on model layers and for other heat treatments have shown that the specific redistribution of Pt was due to the SALICIDE process itself and especially due to the unusual phase sequence that takes place in the presence of the Ni-10 at.% Pt alloy.[33] These results reveal that monitoring the silicide microstructural formation is a key parameter for understanding and controlling device performance.

Nanowires

The operating principles and performance of NW devices are strongly correlated with the morphology and abruptness of functional interfaces. The application of APT to vapor–liquid–solid (VLS)-grown NWs continues to provide a direct measure of dopant composition and distribution, as well as the composition and morphology of buried interfaces. Ultimately, this information is leading toward a better fundamental understanding of the relationship between solution thermodynamics and growth kinetics that govern solute incorporation in VLS-grown NWs. For example, APT has shown dramatic differences in the P-dopant incorporation rate through the liquid catalyst (VLS) into the NW core, versus incorporation via surface deposition (vapor–solid; VS), which leads to a core–shell-like dopant distribution (**Figure 3**a).[34] However, convolution of the dopant distribution presented a challenge to distinguish the contribution via VLS versus the contribution via VS.

Further studies, which isolate VLS dopant incorporation, confirmed radially nonuniform dopant incorporation into the NW core through the liquid catalyst (Figure 3b), leading to a 100-fold enhancement in dopant concentration near the

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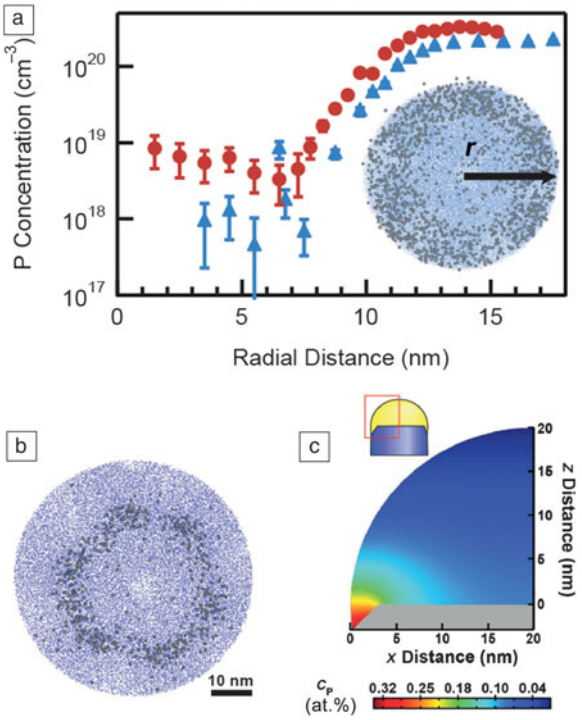


Figure 3. (a) P radial concentration profile within a Ge nanowire (NW) grown at a gas-phase P:Ge ratio of 1:500 (circles) and 1:1000 (triangles). Inset shows the path along which the profile was taken (P = gray spheres; Ge = blue dots). Note: *r* is the radial distance. Adapted with permission from Reference 34. © 2009 Macmillan Publishers. (b) Cross-sectional view through the first 20 nm of the dopant decay region of a P-doped Ge NW (P = gray spheres; Ge = blue dots). The region of enhanced P concentration is contained within the catalyst-defined diameter of the NW (i.e., the trijunction or vapor–liquid–solid interface), as illustrated by the inset schematic in (c). (c) Two-dimensional simulation of P concentration (c_P) in the liquid droplet during steady-state growth with the presence of a side facet. Inset shows a schematic of a growing vapor–liquid–solid NW with corner facets near the trijunction; the red box represents the area simulated in the plot. Note: *x* is the radial distance, and *z* is the axial distance. (b–c) Adapted with permission from Reference 35. © 2013 American Chemical Society.

VLS trijunction in B-doped Si and P-doped Ge NWs.[35] A 2D finite element model was developed to quantitatively explain this enhancement in dopant incorporation at the VLS trijunction region as occurring due to a faceted liquid–solid interface (Figure 3c).

In a similar analysis of Si NWs grown from an Al catalyst, APT revealed a radially and axially homogenous incorporation of individual Al atoms with a concentration that far exceeds the solid solubility.[36] A kinetic model of step-flow growth was used to explain the colossal injection of Al impurity atoms and identify the key thermodynamic growth parameters that influence impurity incorporation. The results from these studies provide some rational experimental handles that can be used to control solute incorporation and ultimately create NWs with outstanding control of properties.

Particles and other 3D structures

Very small nanoparticles (and other 3D structures) have a wide variety of applications, including biomedical, optical, chemical, and electronics,[37] but characterizing next-generation materials and device structures at the nanoscale can pose challenges for most characterization techniques. While the individual NWs presented previously possess a geometry that generally satisfies the requirements for APT specimens (needle shape), many devices/materials cannot be shaped—and key regions properly positioned—into void-free needles with sufficient structural integrity to survive the analysis procedure. Nanowire devices, nanoparticles, quantum dots, and even some current device structures often fail as prospective APT specimens for this reason. One strategy for overcoming these specimen preparation limitations is to encapsulate specimens to fill voids and improve structural integrity.[38–42]

Atomic layer deposition (ALD)[43] has been used for encapsulating complex topologies, including nanoparticles, to enable APT analysis.[40,41] As an example, Pt nanoparticles within a Zn(Al)O matrix created by ALD and analyzed using APT[41] are shown in **Figure 4**. This method used ALD to encase the nanoparticles within an ideally void-free matrix, as shown schematically in Figure 4b. APT analysis of the particles is shown in Figure 4c, where the nanoparticles are illustrated using a 40 at.% Pt isoconcentration surface. This type of capping/encapsulation strategy, coupled with focused ion beam specimen preparation techniques, shows promise to extend the analysis capability of APT to meet the necessary specimen requirements for analyzing the complex 3D topology of next-generation device structures.

Conclusions

The characteristic lengths in microelectronic structures have continuously decreased over the past 10–20 years in accordance

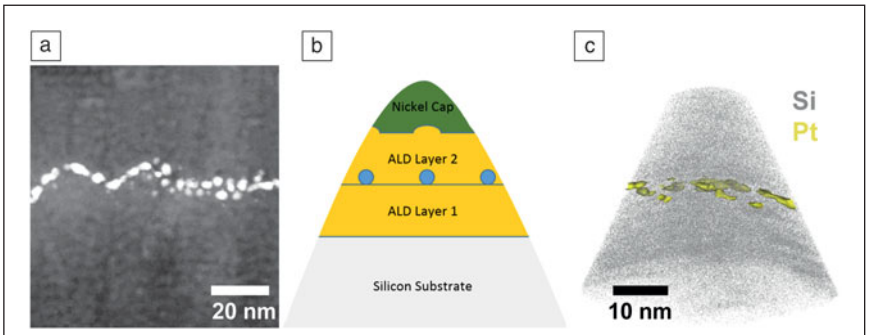


Figure 4. (a) Transmission electron microscope image of Pt nanoparticles surrounded by ZnO layers deposited by atomic layer deposition (ALD). (b) Illustration depicting general strategy for encapsulating Pt nanoparticles (light blue) within an atom probe tomography (APT) specimen. (c) APT atom map showing Pt-rich regions (yellow isoconcentration surface Pt/(Zn+O+Al+Pt) = 40 at.%) surrounded by ZnO (gray points).[41]

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with Moore's Law. At the same time, the overall capabilities of APT have improved such that many new applications are now possible. We reviewed the application of APT to various nanoscale microstructures in elements of electronic devices, NWs, and nanoparticles. These applications include (1) dopant distributions within single devices transistors and finFETs; (2) formation and redistribution mechanisms in Ni(Pt)Si thin-film silicide contacts; (3) direct measure of dopant compositions and distributions, as well as the composition and morphology of buried interfaces in silicon NWs; and (4) Pt nanoparticles encapsulated within a matrix created by ALD.

APT results are providing a link that assists in understanding the relationship between synthesis schemes and the resultant structure and properties. As the capabilities of APT continue to improve, we expect the applications to continue to grow and to be applied to more advanced structures along the semiconductor technology roadmap.

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